

# 74VHC244; 74VHCT244

Octal buffer/line driver; 3-state

Rev. 01 — 17 August 2009

Product data sheet

## 1. General description

The 74VHC244; 74VHCT244 are a high-speed Si-gate CMOS devices.

The 74VHC244; 74VHCT244 have octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs ( $\overline{\text{nOE}}$ ). A HIGH on  $\overline{\text{nOE}}$  causes the outputs to assume a high-impedance OFF-state.

## 2. Features

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than  $V_{CC}$
- Input levels:
  - ◆ The 74VHC244 operates with CMOS input level
  - ◆ The 74VHCT244 operates with TTL input level
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74VHC244D 74VHCT244D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74VHC244PW 74VHCT244PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74VHC244BQ 74VHCT244BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85\text{ mm}$	SOT764-1

## 4. Functional diagram

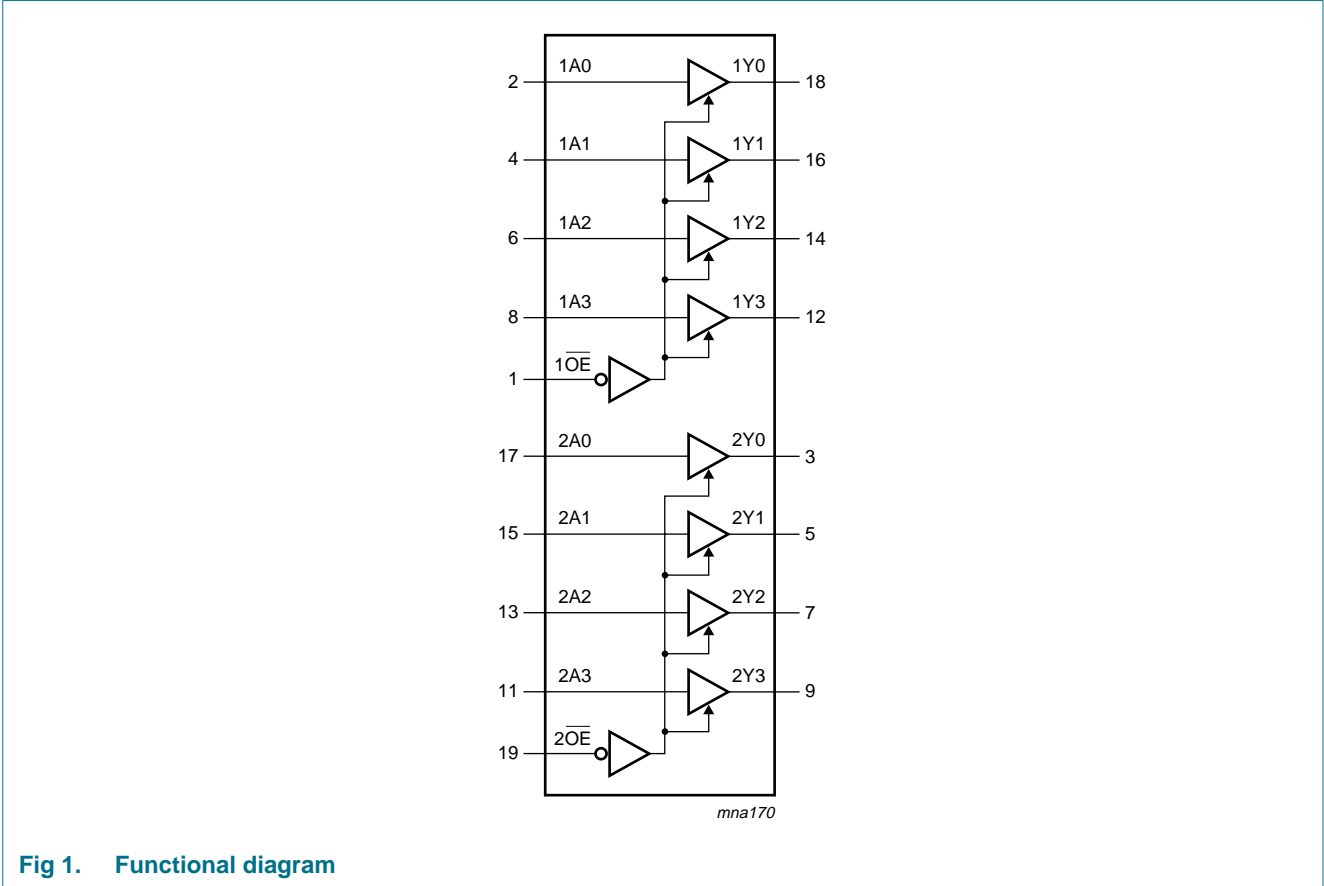


Fig 1. Functional diagram

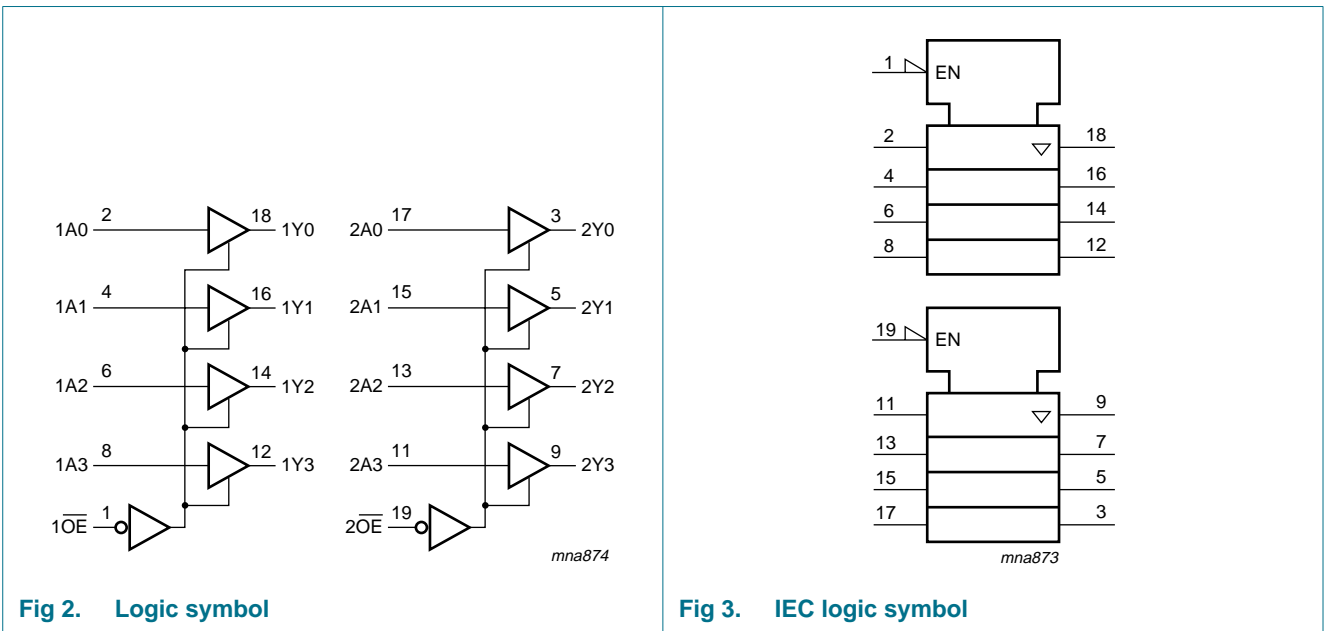
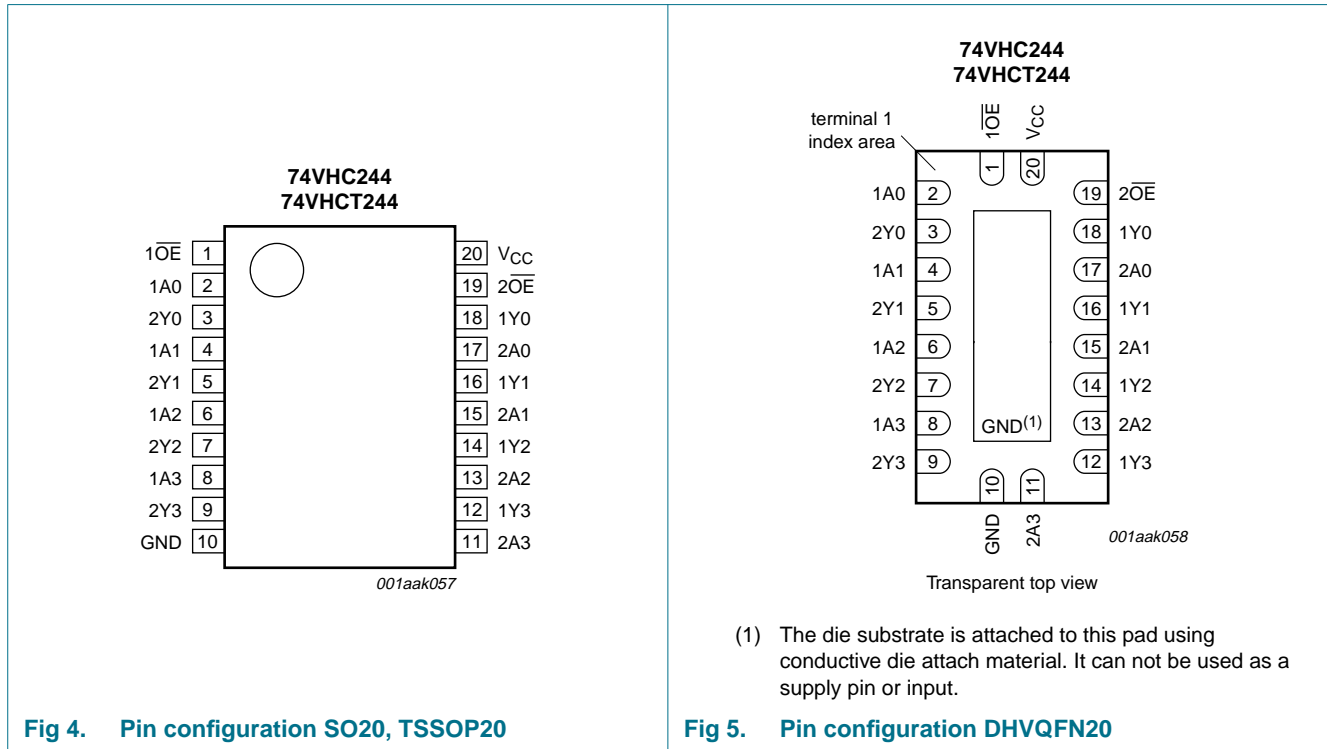


Fig 2. Logic symbol

Fig 3. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input (active LOW)
1A[0:3]	2, 4, 6, 8	data input
2A[0:3]	17, 15, 13, 11	data input
1Y[0:3]	18, 16, 14, 12	data output
2Y[0:3]	3, 5, 7, 9	data output
GND	10	ground (0 V)
$2\overline{OE}$	19	output enable input (active LOW)
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Control	Input	Output
$\overline{\text{nOE}}$	nAn	nYn
L	L	L
	H	H
H	X	Z

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	[1] -20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	$\pm 25$	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
	SO20 package		[2] -	500	mW
	TSSOP20 package		[3] -	500	mW
	DHVQFN20 package		[4] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2]  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 [3]  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
 [4]  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74VHC244			74VHCT244			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>For type 74VHC244</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0 \text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5 \text{ V}$	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0 \text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5 \text{ V}$	-	-	1.65	-	1.65	-	1.65	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$								
		$I_O = -50 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu\text{A}; V_{CC} = 3.0 \text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
	$I_O = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.8	-	3.70	-	V	
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$								
		$I_O = 50 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu\text{A}; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
	$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V	
$I_{OZ}$	OFF-state output current	$V_I = V_{IH} \text{ or } V_{IL};$ $V_O = V_{CC} \text{ or } \text{GND};$ $V_{CC} = 5.5 \text{ V}$	-	-	$\pm 0.25$	-	$\pm 2.5$	-	$\pm 10.0$	$\mu\text{A}$
$I_I$	input leakage current	$V_I = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC} \text{ or } \text{GND}; I_O = 0 \text{ A};$ $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	$\mu\text{A}$

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4.0	-	-	-	-	-	pF
<b>For type 74VHCT244</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = –50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = –8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	per input pin; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0 A V <sub>O</sub> = V <sub>CC</sub> or GND; other pins at V <sub>CC</sub> or GND	-	-	±0.25	-	±2.5	-	±10.0	μA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; I <sub>O</sub> = 0 A; other pins at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	3	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4.0	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
*GND = 0 V. For test circuit see Figure 8.*

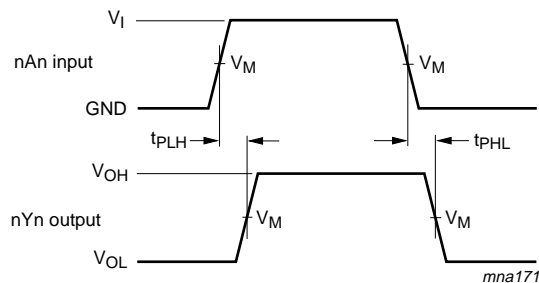
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>For type 74VHC244</b>										
$t_{pd}$	propagation delay	nAn to nYn; see <a href="#">Figure 6</a> <sup>[2]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	5.0	8.4	1.0	10.0	1.0	10.5	ns
		$C_L = 50\text{ pF}$	-	7.0	11.9	1.0	13.5	1.0	15.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
$t_{en}$	enable time	nOE to nYn; see <a href="#">Figure 7</a> <sup>[2]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	6.5	10.6	1.0	12.5	1.0	13.5	ns
		$C_L = 50\text{ pF}$	-	7.5	14.1	1.0	16.0	1.0	18.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	4.0	7.3	1.0	8.5	1.0	9.5	ns
$t_{dis}$	disable time	nOE to nYn; see <a href="#">Figure 7</a> <sup>[2]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	5.5	9.7	1.0	11.0	1.0	12.5	ns
		$C_L = 50\text{ pF}$	-	10.0	14.0	1.0	16.0	1.0	17.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	4.8	7.2	1.0	8.5	1.0	9.0	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50\text{ pF}; f_i = 1\text{ MHz}; V_i = \text{GND to }V_{CC}$ <sup>[3]</sup>	-	10	-	-	-	-	-	pF

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V. For test circuit see Figure 8.*

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>For type 74VHCT244</b>										
$t_{pd}$	propagation delay	nAn to nYn; see Figure 6 <sup>[2]</sup> $V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	3.5	7.4	1.0	8.5	1.0	9.5	ns
		$C_L = 50\text{ pF}$	-	5.0	8.4	1.0	9.5	1.0	10.5	ns
$t_{en}$	enable time	nOE to nYn; see Figure 7 $V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	3.5	10.4	1.0	12.0	1.0	13.0	ns
		$C_L = 50\text{ pF}$	-	5.5	11.4	1.0	13.0	1.0	14.5	ns
$t_{dis}$	disable time	nOE to nYn; see Figure 7 <sup>[2]</sup> $V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	5.0	9.4	1.0	10.0	1.0	12.0	ns
		$C_L = 50\text{ pF}$	-	7.0	11.4	1.0	13.0	1.0	14.5	ns
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}; f = 1\text{ MHz};$ $V_I = \text{GND to }V_{CC}$	<sup>[3]</sup>	12	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 5.0\text{ V}$ ).
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in Volts.

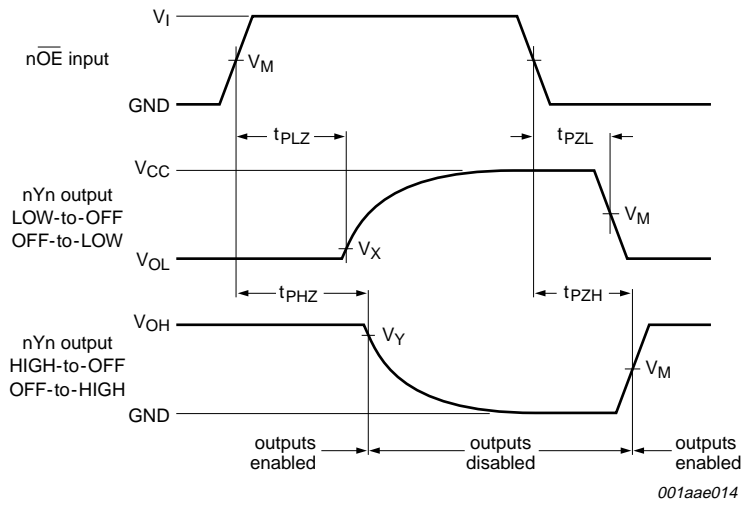
## 11. Waveforms



Measurement points are given in Table 8.  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Propagation delay input (nAn) to output (nYn)**





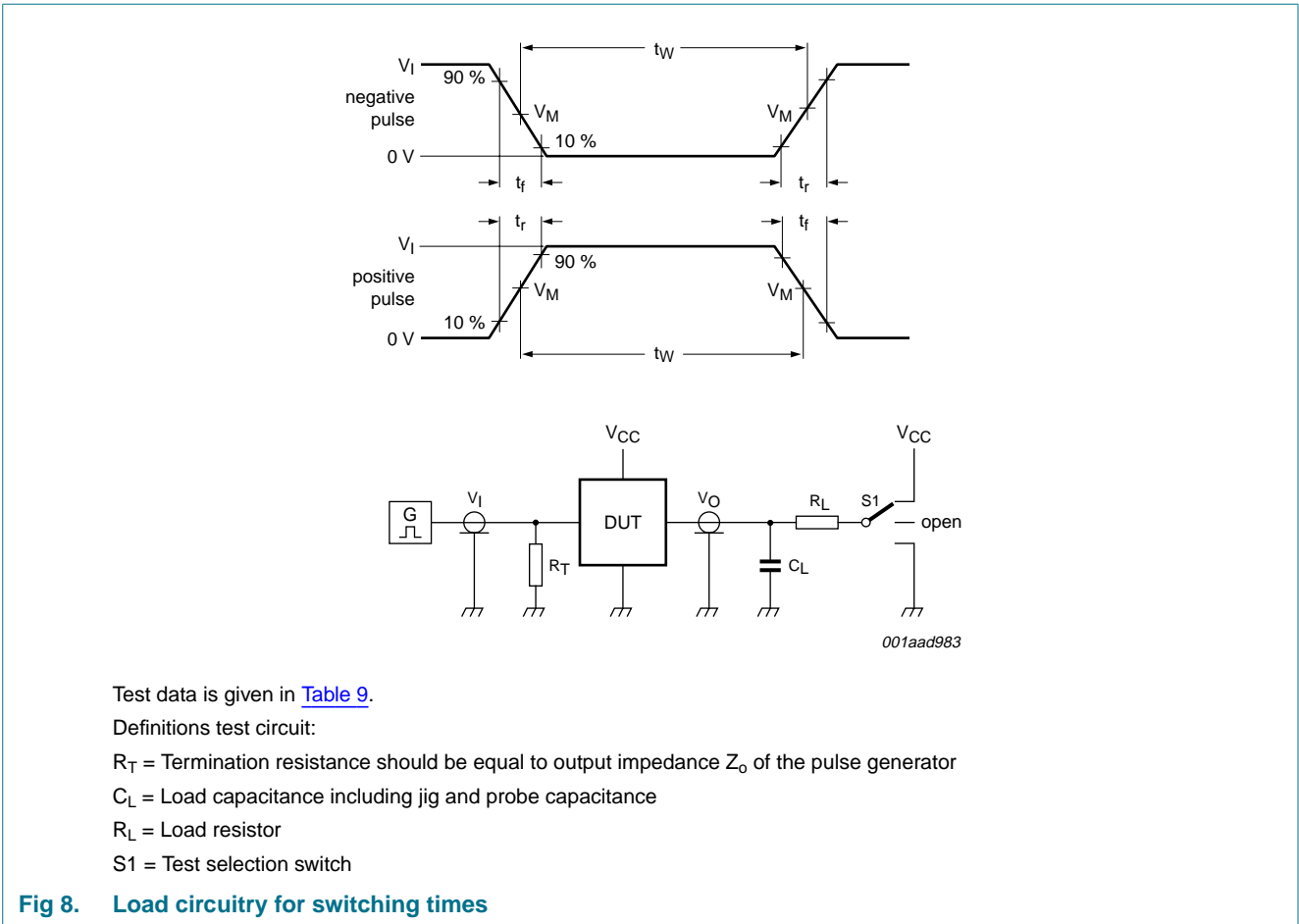
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. enable and disable times**

**Table 8. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74VHC244	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
74VHCT244	1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74VHC244	$V_{CC}$	3.0 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74VHCT244	3.0 V	3.0 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

## 12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

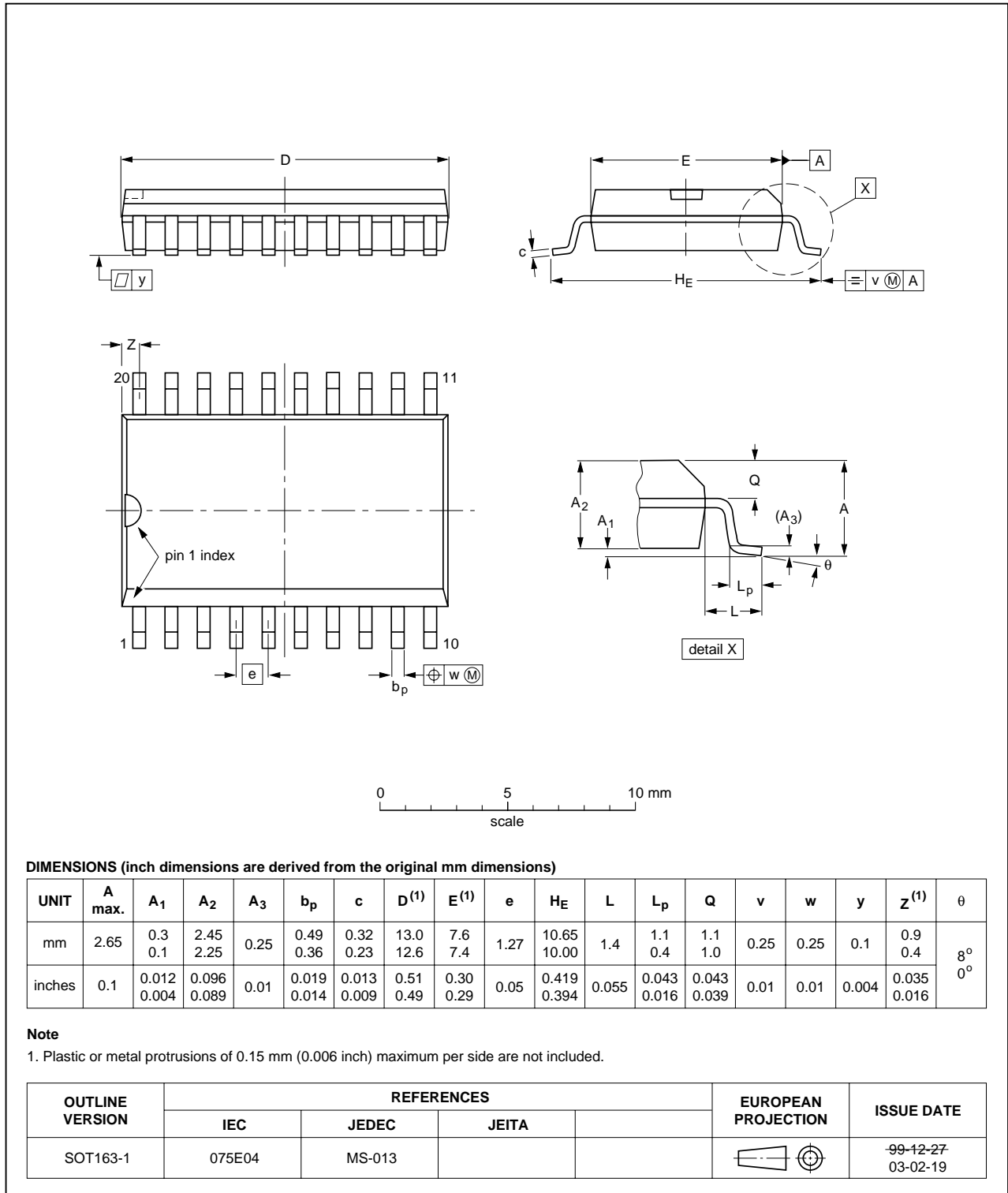


Fig 9. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

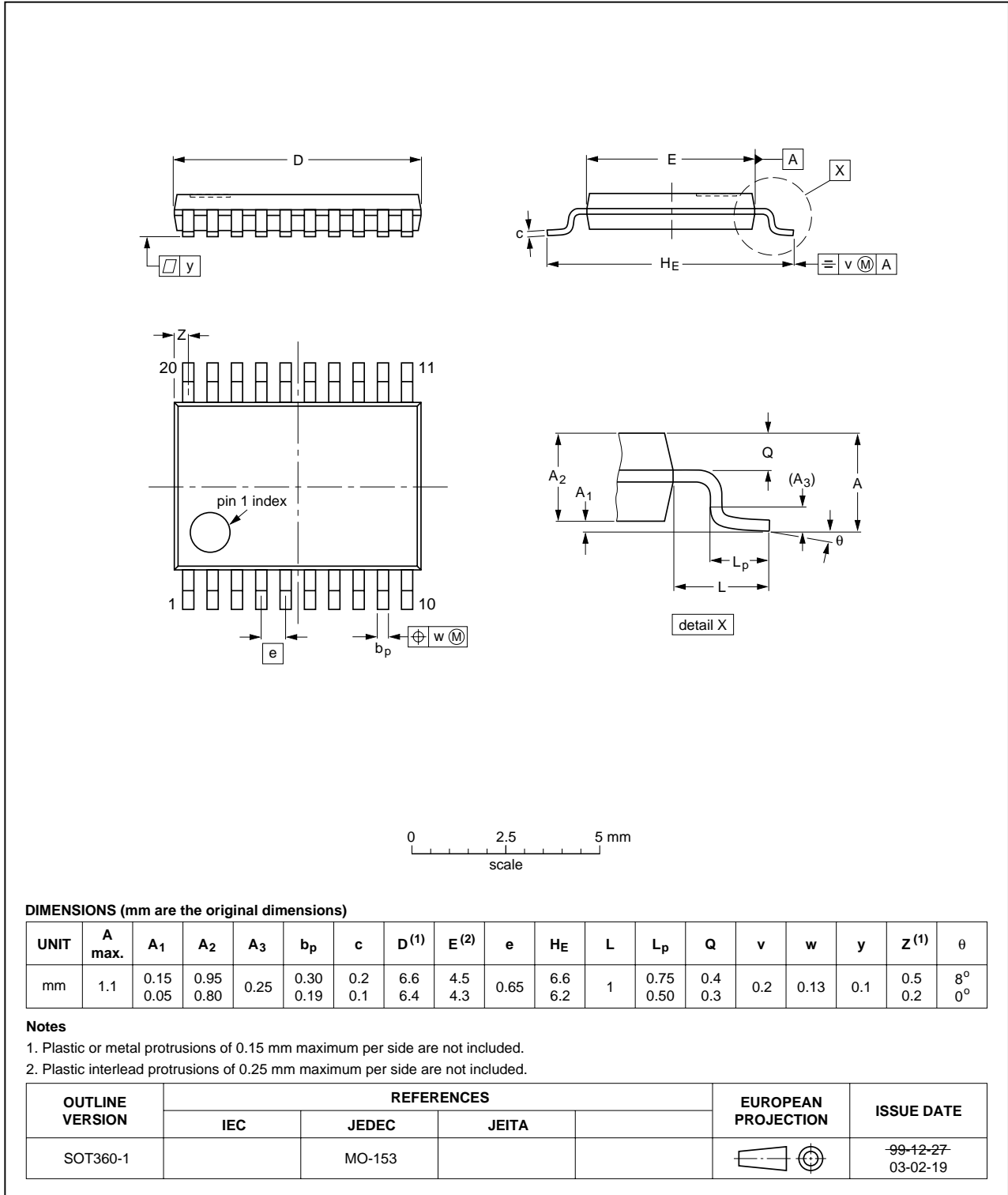
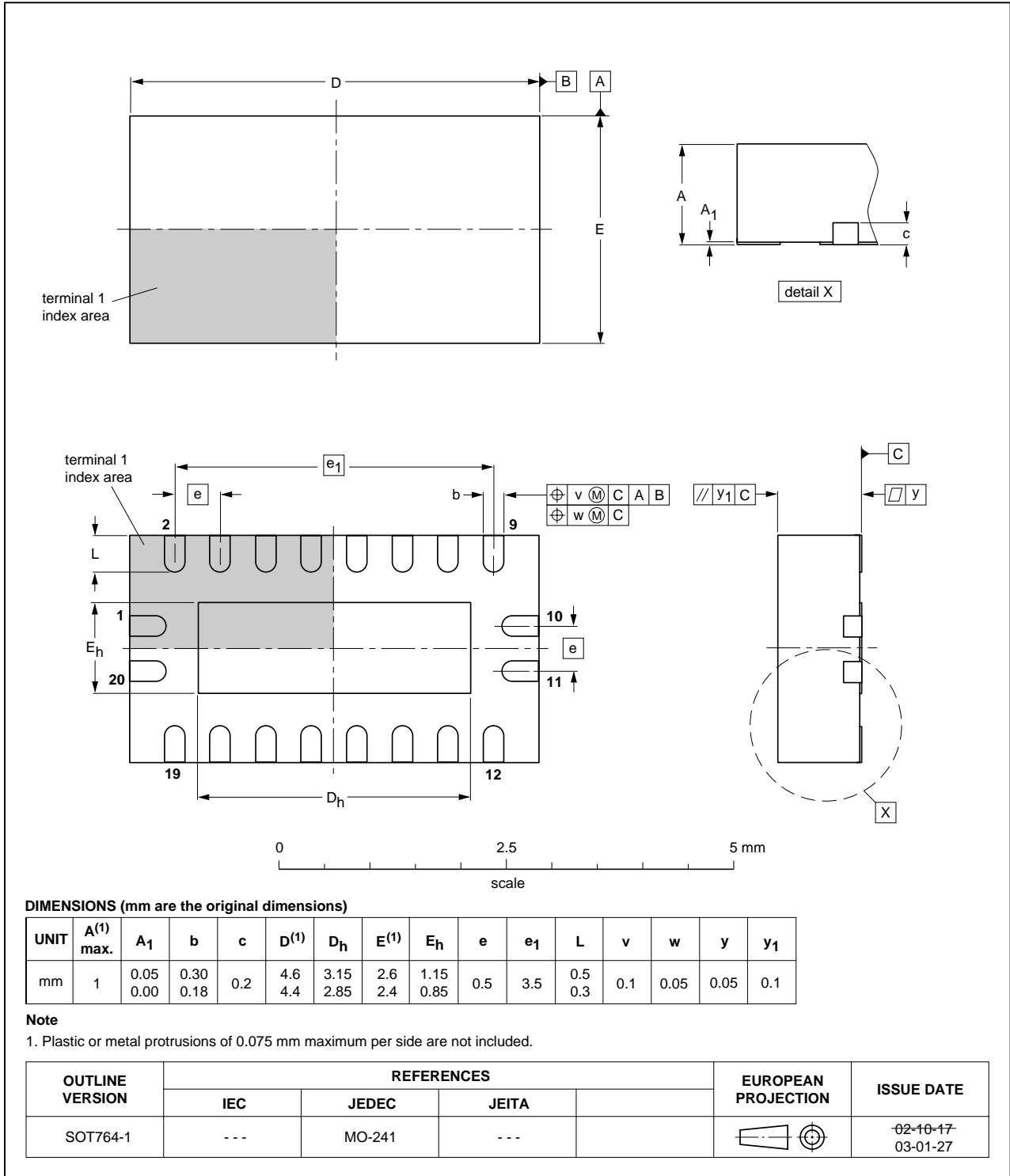


Fig 10. Package outline SOT360-1 (TSSOP20)

**DHVQFN20:** plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

**SOT764-1**



**Fig 11. Package outline SOT764-1 (DHVQFN20)**

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74VHC_VHCT244_1	20090817	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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## 16. Contact information

For more information, please visit: <http://www.nexperia.com>

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