2x20W Stereo / 1x40W Mono Digital Audio Amplifier With 30 bands EQ and DRC Functions

Features

- Supply voltage
  3.3V for digital circuit
  8V~26V for loudspeaker driver
- Supports 2.0CH/Mono configuration
- Loudspeaker output power@12V for stereo
  7W x 2CH into 8Ω <1% THD+N
  10W x 2CH into 4Ω <1% THD+N
- Loudspeaker output power@18V for stereo
  15W x 2CH into 8Ω <1% THD+N
- Loudspeaker output power@24V for stereo
  20W x 2CH into 8Ω <1% THD+N
- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  MCLK system:
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
  BCLK system:
  64xFs for 32kHz / 44.1kHz / 48kHz
  64xFs for 64kHz / 88.2kHz / 96kHz
  64xFs for 128kHz / 176.4kHz / 192kHz
- Sound processing including：
  30 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Three Band plus post Dynamic range control
  Power Clipping
  Programmed 3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  DC-blocking high-pass filter
  Pre-scale/post-scale
- Supports I^2C control without clock
- I^2C control interface with selectable device address
- I^2S output with selectable Audio DSP point
- Support hardware and software reset
- Internal PLL
- Anti-pop design
- Level meter and power meter
- LV Under-voltage shutdown and HV Under-voltage detection
- Over voltage protection
- Short circuit and over-temperature protection

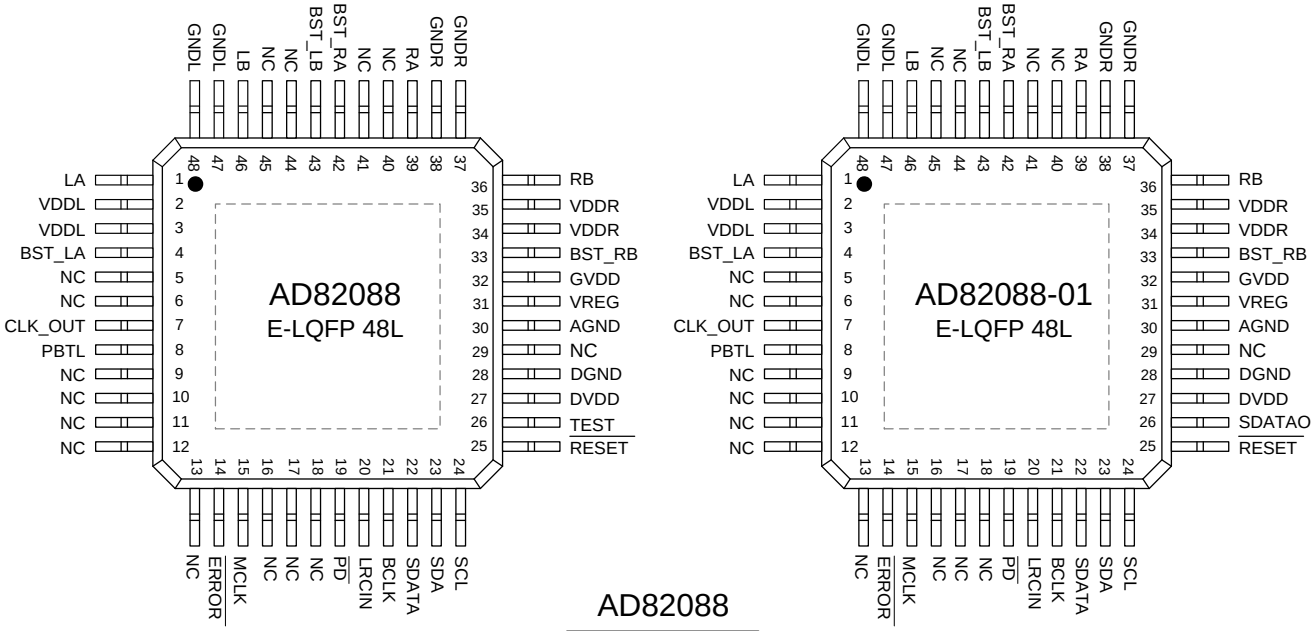
Applications

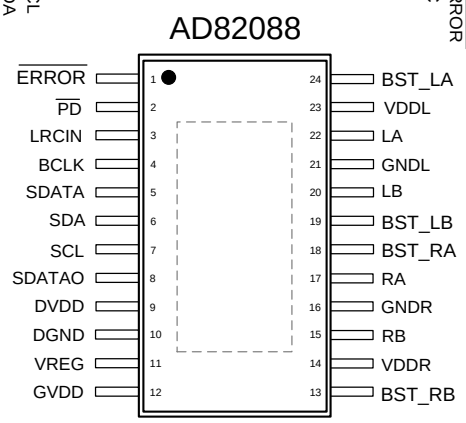
- TV audio

Description

AD82088 is a digital audio amplifier capable of driving 20W (BTL) each to a pair of 8Ω load speaker and 40W (PBTL) to a 4Ω load speaker operating at 24V supply without external heat-sink or fan requirement with play music. AD82088 provides advanced audio processing functions, such as volume control, 30 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD82088 from damage due to accidental erroneous operating condition. The full digital circuit design of AD82088 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD82088 is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment





E-TSSOP-24L

Pin Description (E-LQFP 48L)

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	LA	O	Left channel output A.	
2	VDDL	P	Left channel supply.	
3	VDDL	P	Left channel supply.	
4	BST_LA	P	Bootstrap supply for left channel output A.	
5	NC		Not connected.	
6	NC		Not connected.	
7	CLK_OUT	I/O	PLL ratio setting pin during power up, this pin is monitored on the rising edge of reset. PMF register will be default set at 1 or 16 times PLL ratio.	TTL output buffer, internal pull Low with a 100Kohm resistor.

			High: PMF [3:0] = [0000], 1 time of PLL ratio to avoid system BCLK over flow. Low: PMF [3:0] = [0001], 16 times of PLL ratio. This pin could be clock output pin also during normal operating if EN_CLK_OUT register bit is enabled.	
8	PBTL	I	Stereo/Mono configuration pin. (Low: Stereo ; High: Mono)	TTL output buffer, internal pull Low with a 100Kohm resistor.
9	NC		Not connected.	
10	NC		Not connected.	
11	NC		Not connected.	
12	NC		Not connected.	
13	NC		Not connected.	
14	$\overline{\text{ERROR}}$	I/O	$\overline{\text{ERROR}}$ pin is a dual function pin. One is I^2C address setting during power up. The other one is error status report (low active), It sets by register of A_SEL_FAULT at address 0x1C B[6] to enable it.	This pin is monitored on the rising edge of reset. A value of Low (15-kΩ pull down) sets the I^2C device address to 0x30 and a value of High (15-kΩ pull up) sets it to 0x31.
15	MCLK	I	Master clock input.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
16	NC		Not connected.	
17	NC		Not connected.	
18	NC		Not connected.	
19	$\overline{\text{PD}}$	I	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
20	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
21	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
22	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
23	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
24	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer

25	$\overline{\text{RESET}}$	I	Reset, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
26	TEST	I	This pin must connect to GND.	
27	DVDD	P	Digital Power.	
28	DGND	P	Digital Ground.	
29	NC		Not connected.	
30	AGND	P	Analog Ground.	
31	VREG	O	1.8V Regulator voltage output.	
32	GVDD	O	5V Regulator voltage output. This pin must not be used to drive external devices.	
33	BST_RB	P	Bootstrap supply for right channel output B.	
34	VDDR	P	Right channel supply.	
35	VDDR	P	Right channel supply.	
36	RB	O	Right channel output B.	
37	GNDR	P	Right channel ground.	
38	GNDR	P	Right channel ground.	
39	RA	O	Right channel output A.	
40	NC		Not connected.	
41	NC		Not connected.	
42	BST_RA	P	Bootstrap supply for right channel output A.	
43	BST_LB	P	Bootstrap supply for left channel output B.	
44	NC		Not connected.	
45	NC		Not connected.	
46	LB	O	Left channel output B.	
47	GNDL	P	Left channel ground.	
48	GNDL	P	Left channel ground.	

Pin Description (01-E-LQFP 48L)

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	LA	O	Left channel output A.	
2	VDDL	P	Left channel supply.	
3	VDDL	P	Left channel supply.	
4	BST_LA	P	Bootstrap supply for left channel output A.	
5	NC		Not connected.	
6	NC		Not connected.	

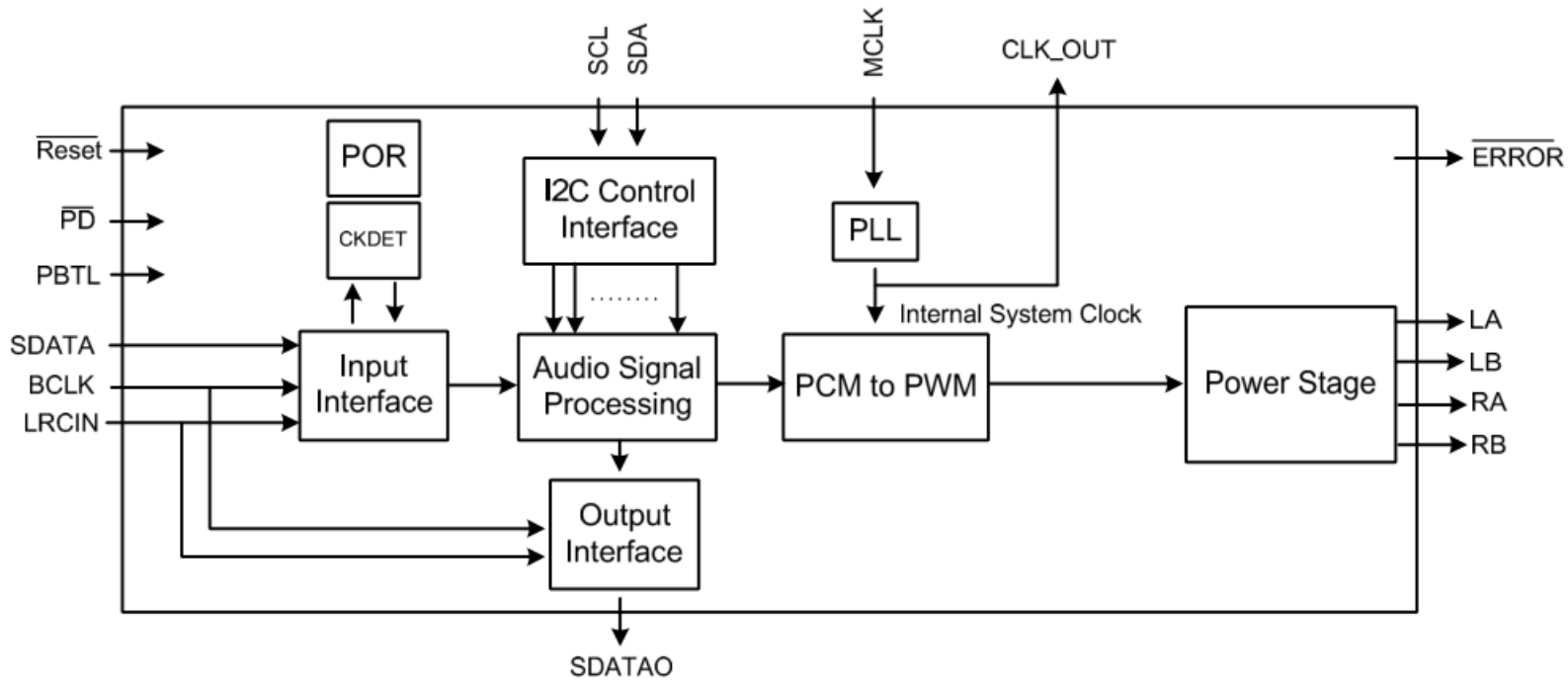
7	CLK_OUT	I/O	PLL ratio setting pin during power up, this pin is monitored on the rising edge of reset. PMF register will be default set at 1 or 16 times PLL ratio. High: PMF [3:0] = [0000], 1 time of PLL ratio to avoid system BCLK over flow. Low: PMF [3:0] = [0001], 16 times of PLL ratio. This pin could be clock output pin also during normal operating if EN_CLK_OUT register bit is enabled.	TTL output buffer, internal pull Low with a 100Kohm resistor.
8	PBTL	I	Stereo/Mono configuration pin. (Low: Stereo ; High: Mono)	TTL output buffer, internal pull Low with a 100Kohm resistor.
9	NC		Not connected.	
10	NC		Not connected.	
11	NC		Not connected.	
12	NC		Not connected.	
13	NC		Not connected.	
14	$\overline{\text{ERROR}}$	I/O	$\overline{\text{ERROR}}$ pin is a dual function pin. One is I^2C address setting during power up. The other one is error status report (low active), It sets by register of A_SEL_FAULT at address 0x1C B[6] to enable it.	This pin is monitored on the rising edge of reset. A value of Low (15-kΩ pull down) sets the I^2C device address to 0x30 and a value of High (15-kΩ pull up) sets it to 0x31.
15	MCLK	I	Master clock input.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
16	NC		Not connected.	
17	NC		Not connected.	
18	NC		Not connected.	
19	$\overline{\text{PD}}$	I	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
20	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
21	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm

				resistor.
22	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
23	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
24	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer
25	$\overline{\text{RESET}}$	I	Reset, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
26	SDATAO	O	Serial audio data output.	Schmitt trigger TTL input buffer
27	DVDD	P	Digital Power.	
28	DGND	P	Digital Ground.	
29	NC		Not connected.	
30	AGND	P	Analog Ground.	
31	VREG	O	1.8V Regulator voltage output.	
32	GVDD	O	5V Regulator voltage output. This pin must not be used to drive external devices.	
33	BST_RB	P	Bootstrap supply for right channel output B.	
34	VDDR	P	Right channel supply.	
35	VDDR	P	Right channel supply.	
36	RB	O	Right channel output B.	
37	GNDR	P	Right channel ground.	
38	GNDR	P	Right channel ground.	
39	RA	O	Right channel output A.	
40	NC		Not connected.	
41	NC		Not connected.	
42	BST_RA	P	Bootstrap supply for right channel output A.	
43	BST_LB	P	Bootstrap supply for left channel output B.	
44	NC		Not connected.	
45	NC		Not connected.	
46	LB	O	Left channel output B.	
47	GNDL	P	Left channel ground.	
48	GNDL	P	Left channel ground.	

Pin Description (E-TSSOP 24L)

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{\text{ERROR}}$	I/O	$\overline{\text{ERROR}}$ pin is a dual function pin. One is I^2C address setting during power up. The other one is error status report (low active), It sets by register of A_SEL_FAULT at address 0x1C B[6] to enable it.	This pin is monitored on the rising edge of reset. A value of Low (15-kΩ pull down) sets the I^2C device address to 0x30 and a value of High (15-kΩ pull up) sets it to 0x31.
2	$\overline{\text{PD}}$	I	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
3	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
4	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
5	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
6	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
7	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer
8	SDATAO	O	Serial audio data output.	Schmitt trigger TTL input buffer
9	DVDD	P	Digital Power.	
10	DGND	P	Digital Ground.	
11	VREG	O	1.8V Regulator voltage output.	
12	GVDD	O	5V Regulator voltage output. This pin must not be used to drive external devices.	
13	BST_RB	P	Bootstrap supply for right channel output B.	
14	VDDR	P	Right channel supply.	
15	RB	O	Right channel output B.	
16	GNDR	P	Right channel ground.	
17	RA	O	Right channel output A.	
18	BST_RA	P	Bootstrap supply for right channel output A.	
19	BST_LB	P	Bootstrap supply for left channel output B.	
20	LB	O	Left channel output B.	
21	GNDL	P	Left channel ground.	
22	LA	O	Left channel output A.	
23	VDDL	P	Left channel supply.	
24	BST_LA	P	Bootstrap supply for left channel output A.	

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD82088-LG48NRY	E-LQFP 48L (7mmx7mm)	250 Units / Tray 2.5K Units / Box (10 Tray)	Green
AD82088-QG24NRT	E-TSSOP 24L	62 Units / Tube 100 Units / Small box	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jt}(℃/W)	Exposed Thermal Pad
E-LQFP 48L	AD82088	22.9	1.64	34.9	Yes (Note1)
E-TSSOP 24L		26.8	1.83	27.1	

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja}, the junction-to-ambient thermal resistance is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The simulation is tested using the JESD51-5 thermal measurement standard.

Note 1.3: Ψ_{jt} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtaining θ_{ja}, using a procedure described in JESD51-2.

Note 1.4: θ_{jt} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

Marking Information

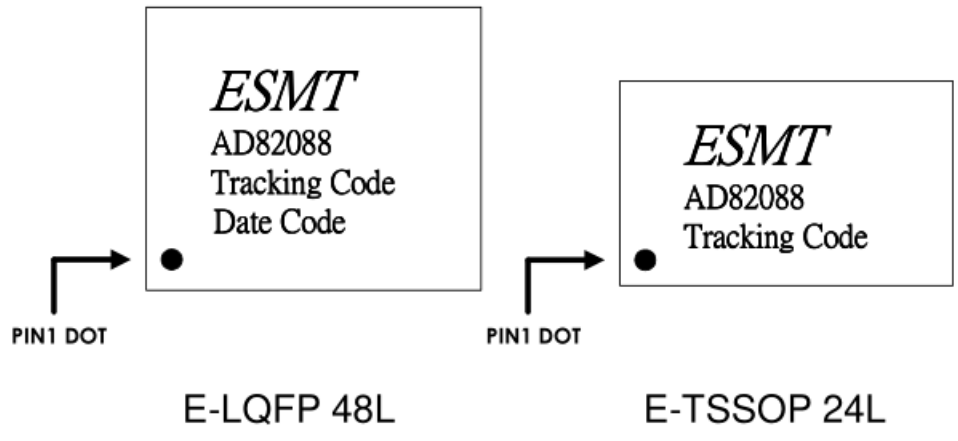
AD82088

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code

Line 4 : Date Code



E-LQFP 48L E-TSSOP 24L

Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	8~26	V
T_J	Junction Operating Temperature	-40~125	°C
T_A	Ambient Operating Temperature	-40~85	°C

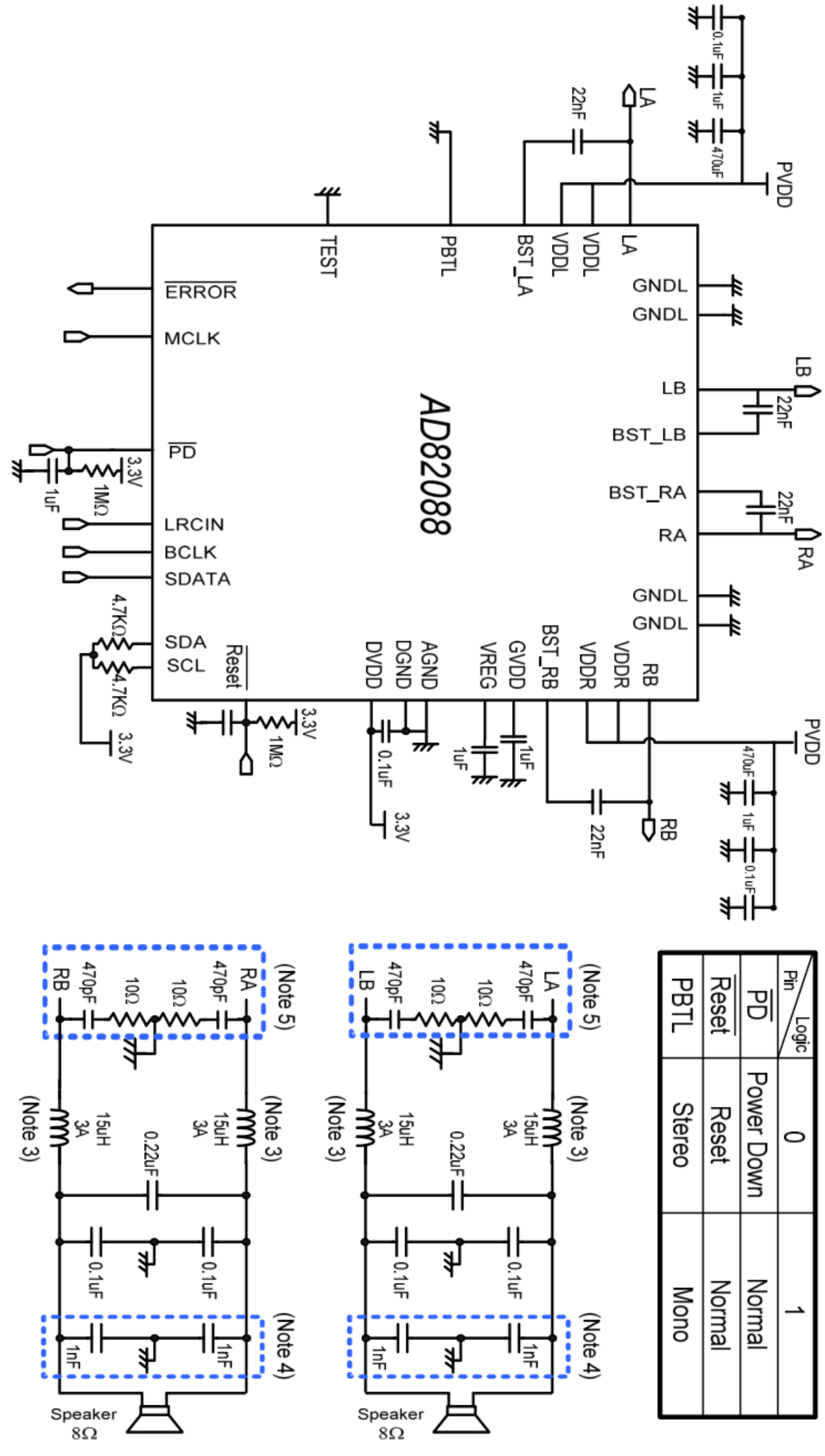
General Electrical Characteristics

Condition: T_A=25 °C (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}(HV)	PVDD Supply Current during Power Down	PVDD=24V		20	40	uA
I_Q(HV)	Quiescent current for PVDD (50%/50% PWM duty)	PVDD=24V		15		mA
I_Q(LV)	Quiescent current for DVDD (Un-mute)	DVDD=3.3V, PBTL=Low		31		mA
T_{SENSOR}	Junction Temperature for Driver Shutdown			165		°C
	Temperature Hysteresis for Recovery from Shutdown			35		°C
UV_{DVDDH}	DVDD Under Voltage Release			2.99		V
UV_{DVDDL}	DVDD Under Voltage Active			2.89		V
UV_{PVDDH}	VDDL/R Under Voltage Release			7.7		V
UV_{PVDDL}	VDDL/R Under Voltage Active			7.1		V
OV_H	VDDL/R Over Voltage Active			29.2		V
OV_L	VDDL/R Under Voltage Release			28.5		V
	Static Drain-to-Source On-state Resistor, NMOS	PVDD=24V, Id=500mA		180		mΩ
I_{SC}	L(R) Channel Over-Current Protection (Note 2)	PVDD=24V		9		A
		PVDD=12V		8.5		A
	Mono Over-Current Protection (Note 2)	PVDD=24V		18		A
		PVDD=12V		17		A
V_{IH}	High-Level Input Voltage	DVDD=3.3V	2.0			V
V_{IL}	Low-Level Input Voltage	DVDD=3.3V			0.8	V
V_{OH}	High-Level Output Voltage	DVDD=3.3V	2.4			V
V_{OL}	Low-Level Output Voltage	DVDD=3.3V			0.4	V
C_I	Input Capacitance			6.4		pF

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Application Circuit Example for Stereo



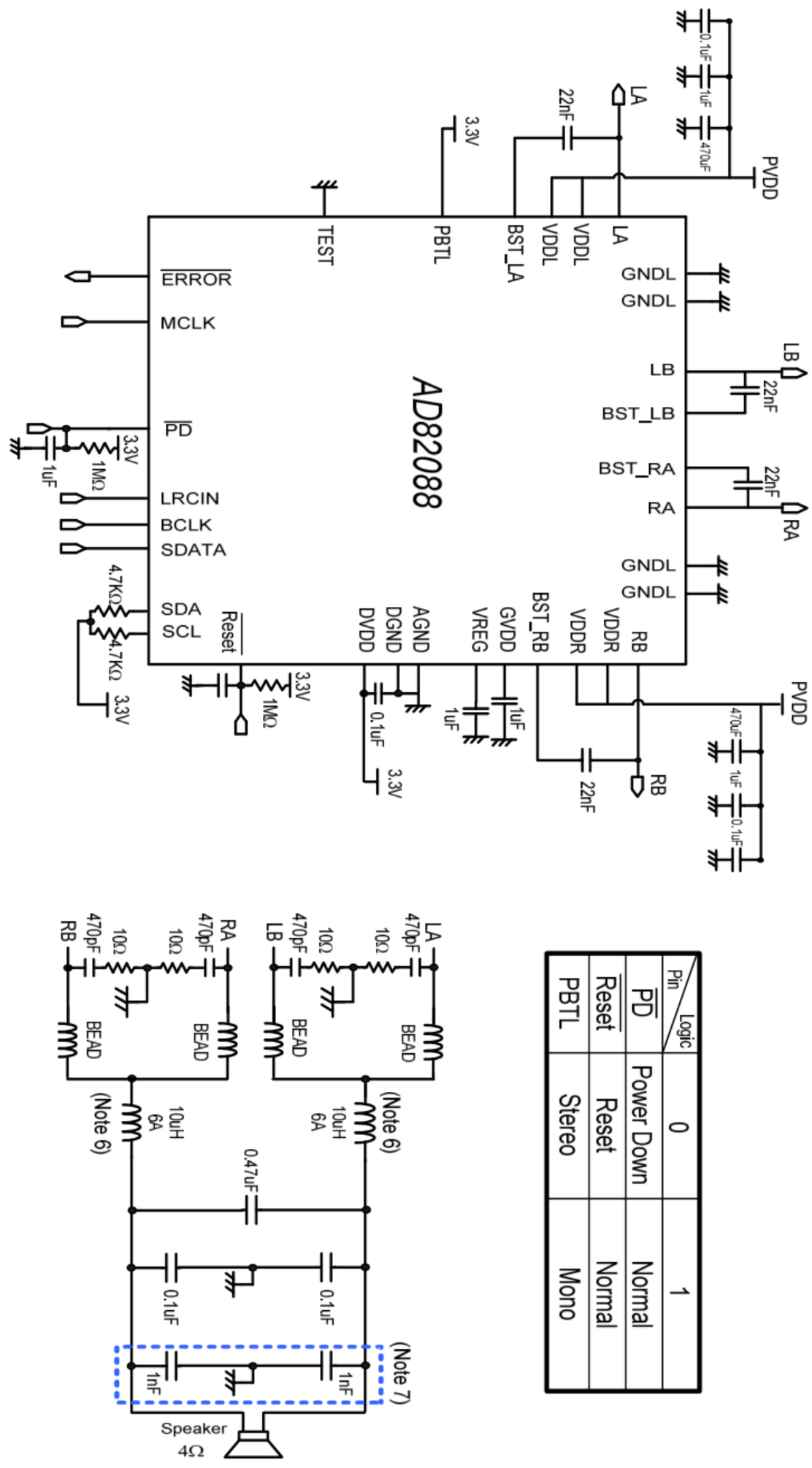
Pin / Logic	0	1
$\overline{PD}$	Power Down	Normal
$\overline{Reset}$	Reset	Normal
PBTL	Stereo	Mono

Note 3: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than I_{SC}.

Note 4: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 5: The snubber circuit can be removed while the PVDD <=20V.

Application Circuit Example for Mono



Pin / Logic	0	1
$\overline{PD}$	Power Down	Normal
$\overline{Reset}$	Reset	Normal
PBTL	Stereo	Mono

Note 6: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than I_{SC}.

Note 7: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.