ALC268 Series
(ALC268-GR, ALC268Q-GR, ALC268-VB1-GR)

2+2 CHANNEL HIGH DEFINITION AUDIO CODEC

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC268 Series Audio codecs.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2006/09/04	First release.
1.1	2007/12/12	Add ALC268-VB (Version B) information (Intermediate Release)
1.2	2008/01/07	Updated ALC268 version B part number in section 12 Ordering Information, page 72 (Intermediate Release).
1.3	2008/04/25	Updated ALC268 version B part number in section 12 Ordering Information, page 72.

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1. General Description

The ALC268 series (ALC268-VB1/ALC268/ALC268Q) 4-Channel ADC High Definition Audio Codecs with UAA (Universal Audio Architecture). Featuring two stereo DACs and two stereo ADCs, the 4 DAC channels support stereo sound playback on the rear panel and independent stereo sound output on the front panel simultaneously (multiple streaming). The two stereo ADCs integrate two stereo and independent analog sound inputs.

The ALC268-GR and ALC268Q-GR meet the current WLP3.10 (Windows® Logo Program) requirements. The ALC268-VB1-GR is the B version of the ALC268 and meets future WLP requirements that become effective from 01 June 2008, bringing PC sound quality closer to consumer electronic devices.

The ALC268 series support up to 4 digital microphone channels (microphone array) with Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technology simultaneously, significantly improving sound quality for PC VoIP applications.

The S/PDIF output offers easy connection of PCs to high quality consumer electronic products such as digital decoders and speakers.

The ALC268 series support host audio controller from the Intel ICH series and upcoming PCH chipset, and also from any other HDA compatible audio controller. With EAX/Direct Sound 3D/I3DL2/A3D compatibility, and excellent software utilities like environment sound emulation, multiple and independent software equalizer bands, dynamic range control, optional Dolby® Digital Live, Dolby® PCEE programs and SRS® TrueSurround HD, the ALC268 provides an excellent multimedia experience for PC users.

Model Differences

The ALC268-VB1 is fully pin compatible and software backward compatible with the ALC268. Board designs using the ALC268 can use the ALC268-VB1 directly without PCB (Printed Circuit Board) or software changes.

Three main functions have been added in the ALC268-VB:

- Meets future Windows® Logo Program (WLP) requirements that become effective from 01 June 2008
- Integrates a DC cancellation filter to cancel DC offset from digital microphones (becoming common in notebook and Ultra Mobile PCs)
- ADCs support 24-bit format recording

2. Features

2.1. Hardware Features

- Meets WLP (Windows Logo Program) 3.10 premium audio requirements
- ALC268-VB1 meets future WLP requirements that become effective from 01 June 2008
- 95dB Signal-to-Noise Ratio DAC performance and 90dB Signal-to-Noise Ratio ADC performance
- Two stereo DACs support independent 16/20/24-bit PCM format playback
- Two stereo ADCs support independent 16/20-bit PCM format recording
- Two stereo ADCs support independent 16/20/24-bit PCM format recording (ALC268-VB1)
- All DACs supports 44.1/48/96/192kHz sample rate
- All ADCs support 44.1/48/96kHz sample rate
- 16/20/24-bit S/PDIF-OUT supports 44.1/48/96/192kHz sample rate
- Up to four channels of microphone input are supported for AEC/BF applications
- Supports MONO line output with independent volume control
- High-quality analog differential CD input
- Supports external PCBEEP input and built-in digital BEEP generator
- Software selectable 2.5V/3.75V/4.2V VREFOUT
- Two jack detection pins, each designed to detect up to 4 jacks
- 1dB resolution of analog output volume control
- Programmable 20dB and 40dB boost for analog microphone input
- Supports hardware digital volume control for digital microphone input
- Built-in headphone amplifiers for port-A and port-D
- 4 GPIOs (GPIO0/GPIO3 are digital GPIO shared with digital MIC interface, GPIO1/GPIO2 are analog) for customized applications
- EAPD (External Amplifier Power Down) is supported

- Supports Anti-pop mode when analog power AVDD is on and digital power is off
- Power support: 3.3V digital core power; 1.5V~3.3V digital IO power for HDA link; 3.3V~5.0V analog power
- The ALC268-VB integrates a DC cancellation filter to cancel DC offset from digital microphones
- 48-pin LQFP 'Green' package (ALC268, ALC268-VB)
- 48-pin QFN 'Green' package (ALC268Q only)

2.2. Software Features

- Meets Microsoft Windows Logo Program requirements
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- HRTF 3D Positional Audio
- Emulation of 26 sound environments to enhance gaming experience
- Multi-band software equalizer and tools
- Voice Cancellation and Key Shifting effect
- Dynamic range control (expander, compressor and limiter) with adjustable parameters
- Intuitive Configuration Panel (Realtek Audio Manager) to enhance user experience
- Provides 10-foot GUI for Windows Media Center
- Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS), and Beam Forming (BF) technology for voice application
- Smart multiple streaming operation
- HDMI audio driver for AMD platform
- Dolby® PCEE program™ (optional software feature)

- SRS® TrueSurround HD (optional software feature)
- Fortemedia® SAM™ technology for voice processing (Beam Forming and Acoustic Echo Cancellation) (optional software feature)

3. System Applications

- Windows Vista premium desktop and notebook PCs
- Ultra Mobile PCs

4. Block Diagram

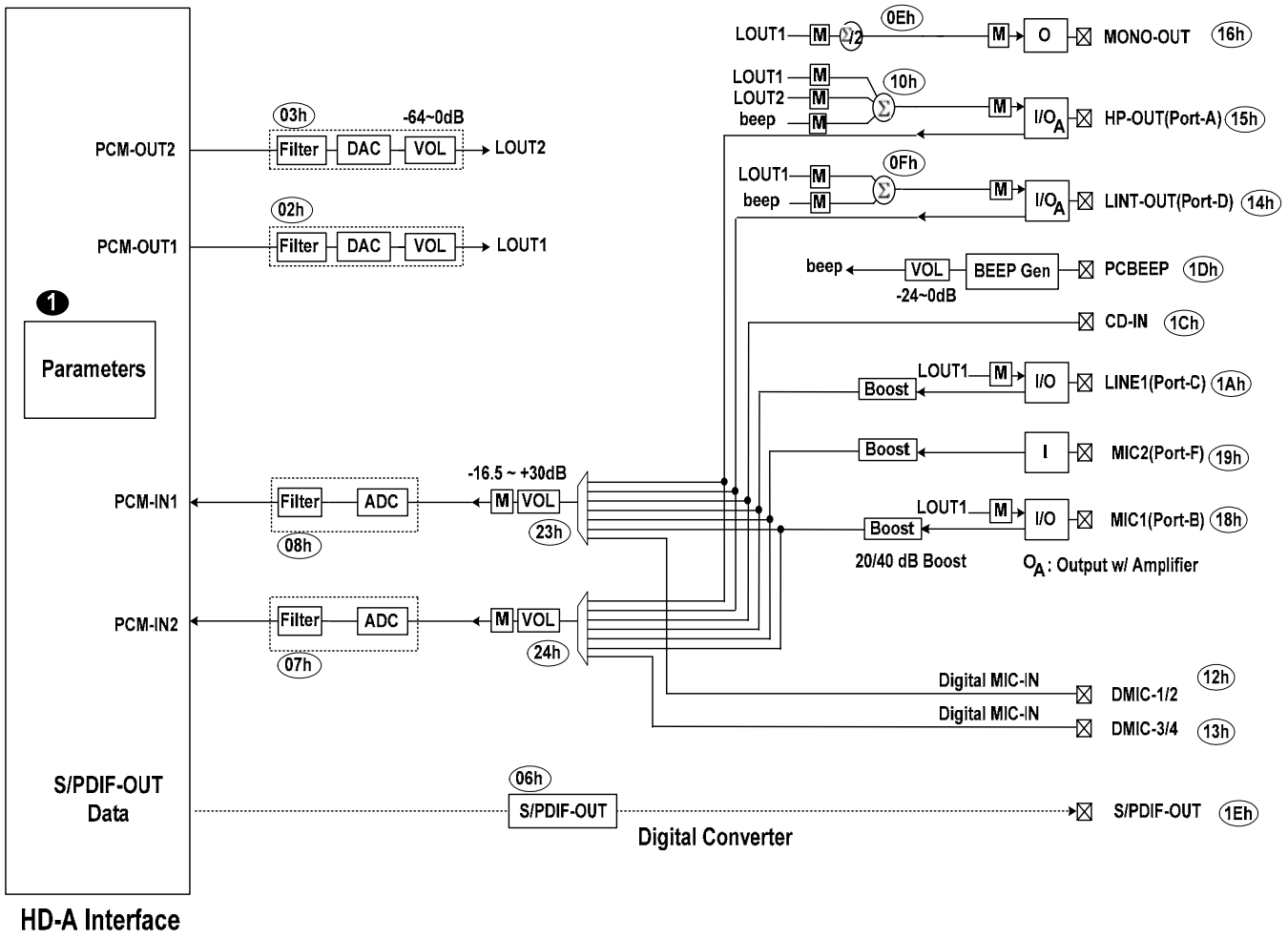


Figure 1. Block Diagram

4.1. Analog Input/Output Unit

Pin widgets NID=14h, 15h, 18h and 1Ah are re-tasking IOs supporting input units. NID=14h and 15h support an amplifier unit.

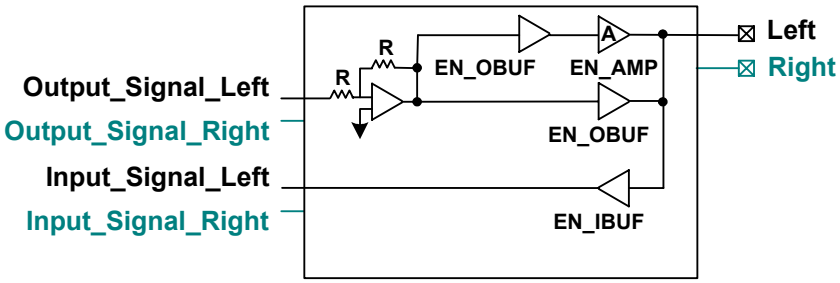


Figure 2. Analog Input/Output Unit

5. Pin Assignments

5.1. ALC268/ALC268-VB (LQFP-48)

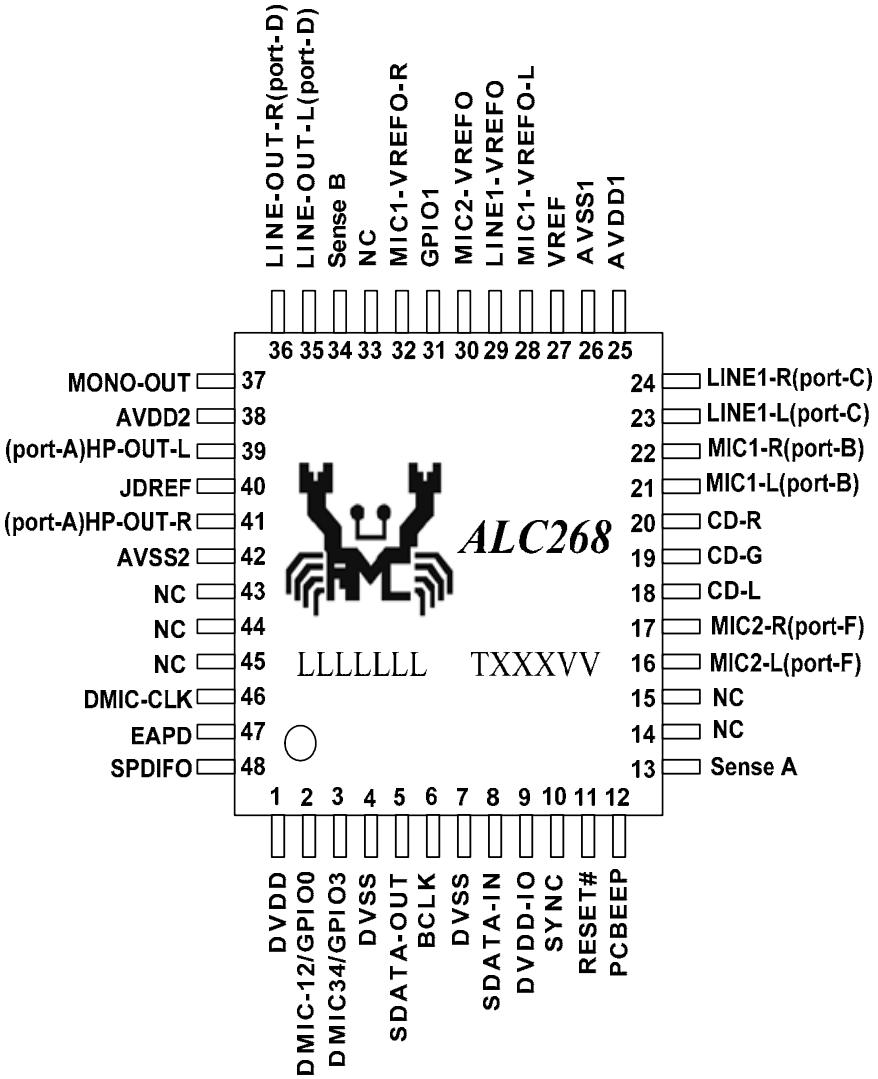


Figure 3. Pin Assignments ALC268/ALC268-VB (LQFP-48)

Note: The ALC268-VB and ALC268 are pin-to-pin compatible.

5.2. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3. The version number is shown in the location marked 'VV'. For example, 'VV=B1' indicates silicon version 'B' and stepping version '1'.

5.3. ALC268Q (QFN-48)

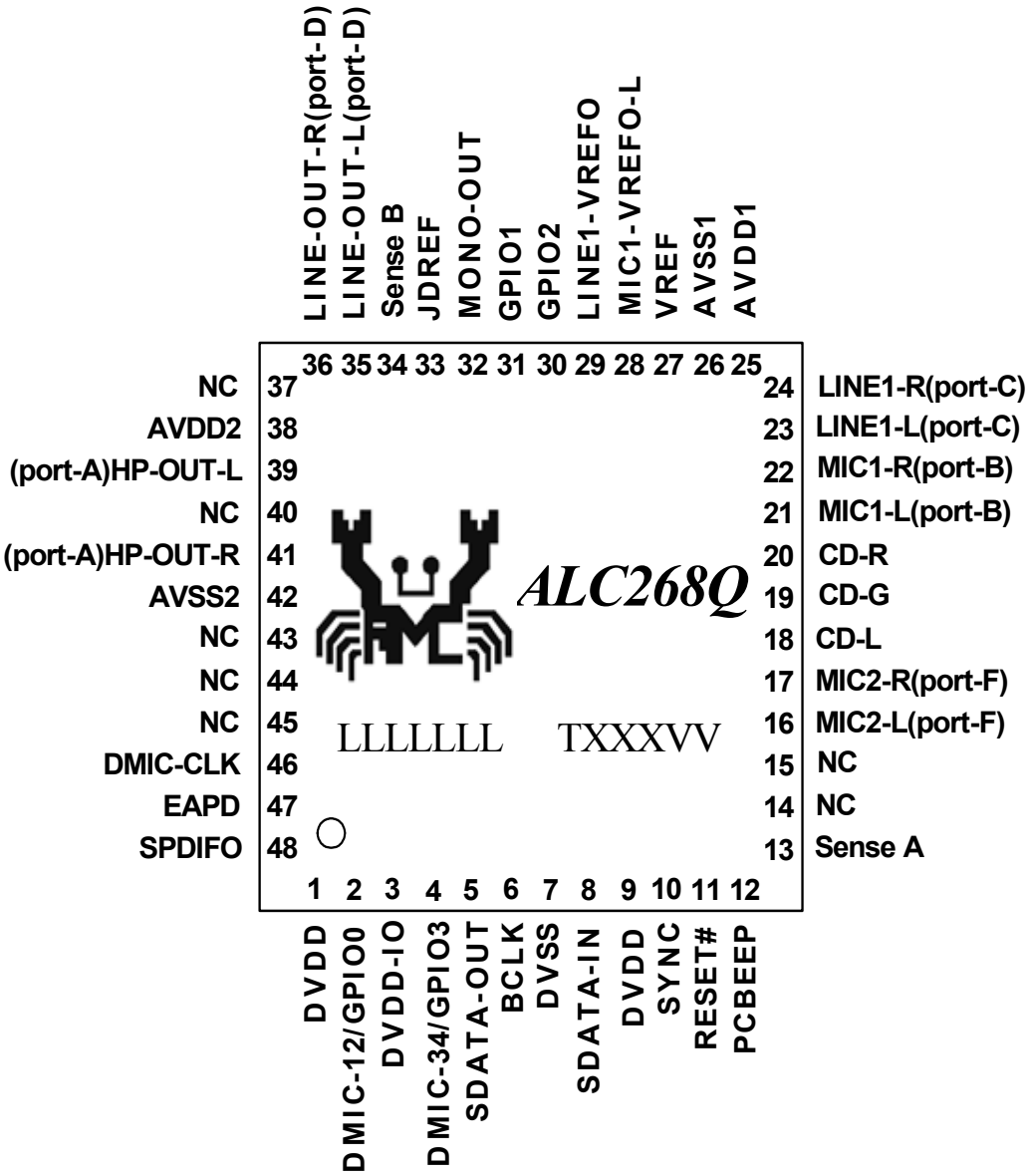


Figure 4. Pin Assignments ALC268Q (QFN-48)

Note: The ALC268Q is NOT pin compatible with the ALC268/ALC268-VB1.

5.4. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 4. The version number is shown in the location marked 'VV'. For example, 'VV=B1' indicates silicon version 'B' and stepping version '1'.

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	ALC268/-VB1 (LQFP-48) Pin No.	ALC268Q (QFN-48) Pin No.	Description	Characteristic Definition
RESET#	I	11	11	H/W Reset Control	V_t=0.5*DVDD
SYNC	I	10	10	Sample Sync (48kHz)	V_t=0.5*DVDD
BCLK	I	6	6	24MHz Bit Clock Input	V_t=0.5*DVDD
SDATA-OUT	I	5	5	Serial TDM Data Input	V_t=0.5*DVDD
SDATA-IN	O	8	8	Serial TDM Data Output	V_{OH}=0.9*DVDD, V_{OL}=0.1*DVDD
EAPD	O	47	47	S/PDIF Input / Signal to Power Down Ext. Amp	Output V_{OH}=DVDD, V_{OL}=DVSS
SPDIFO	O	48	48	S/PDIF Output	Output has 12mA@75Ω driving capability.
GPIO0/ DMIC-12	IO	2	2	General Purpose Input/Output 0 Data input from digital MIC 1&2	Input Vt=(2/3)*DVDD, output V_{OH}=DVDD, V_{OL}=DVSS, internal pulled up by 50KΩ
GPIO3/ DMIC-34	IO	3	4	General Purpose Input/Output 3 Data input from digital MIC 3&4	Input Vt=(2/3)*DVDD, output V_{OH}=DVDD, V_{OL}=DVSS, internal pulled up by 50KΩ
DMIC-CLK	O	46	46	Clock Output for Digital MIC	Default 2.048MHz clock output
Total	-	10 pins	10 pins	-	-

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	ALC268/-VB1 (LQFP-48) Pin No.	ALC268Q (QFN-48) Pin No.	Description	Characteristic Definition
MIC2-L	IO	16	16	2nd Stereo Microphone Input Left Channel	Analog input/output, default is input (PORT–F)
MIC2-R	IO	17	17	2nd Stereo Microphone Input Right Channel	Analog input/output, default is input (PORT–F)
CD-L	I	18	18	CD Input Left Channel	Analog input, 1.6Vrms of full-scale input
CD-G	I	19	19	CD Input Reference Ground	Analog input, 1.6Vrms of full-scale input
CD-R	I	20	20	CD Input Right Channel	Analog input, 1.6Vrms of full-scale input
MIC1-L	IO	21	21	1st Stereo Microphone Input Left Channel	Analog input/output, default is input (PORT–B)
MIC1-R	IO	22	22	1st Stereo Microphone Input Right Channel	Analog input/output, default is input (PORT–B)
LINE1-L	IO	23	23	1st Line Input Left Channel	Analog input/output, default is input (PORT–C)
LINE1-R	IO	24	24	1st Line Input Right Channel	Analog input/output, default is input (PORT–C)
PCBEEP	I	12 pin	12 pin	External PCBEEP Input	Analog input, 1.6Vrms of full-scale input
LINE-OUT-L	IO	35	35	Line Output Left Channel	Analog output (PORT–D)
LINE-OUT-R	IO	36	36	Line Output Right Channel	Analog output (PORT–D)
HP-OUT-L	IO	39	39	Headphone Out Left Channel	Analog output (PORT–A)
HP-OUT-R	IO	41	41	Headphone Out Right Channel	Analog output (PORT–A)
MONO-OUT	O	37	32	MONO Output	Analog mono output is summation of (L+R)/2
Sense A	I	13	13	Jack Detect Pin L	Resistor {5.1K, 10K, 20K, 39.2K} w/ 1% accuracy
Sense B	I	34	34	Jack Detect Pin 2	Resistor {5.1K, 10K, 20K, 39.2K} w/ 1% accuracy
GPIO1	IO	31	31	General Purpose Input/Output 1	Input Vt=(2/3)*AVDD, output V_{OH}=AVDD, V_{OL}=AVSS, internal pulled up by 50KΩ
GPIO2	IO	-	30	General Purpose Input/Output 2	Input Vt=(2/3)*AVDD, output V_{OH}=AVDD, V_{OL}=AVSS, internal pulled up by 50KΩ
Total	-	18 pins	19 pins	-	-

6.3. Filter/Reference/Not Connected

Table 3. Filter/Reference

Name	Type	ALC268/-VB1 (LQFP-48) Pin No.	ALC268Q (QFN-48) Pin No.	Description	Characteristic Definition
VREF	-	27	27	2.5V Reference Voltage	1µF capacitor to analog ground
MIC1-VREFO-L	O	28	28	Bias Voltage for MIC1 Jack	2.5V/3.2/4.2Vreference voltage
LINE1-VREFO	O	29	29	Bias Voltage for LINE1 Jack	2.5V/3.2/4.2Vreference voltage
MIC2-VREFO	O	30	-	Bias Voltage for MIC2 Jack	2.5V/3.2/4.2Vreference voltage
MIC1-VREFO-R	O	32	-	Bias Voltage for MIC1 Jack	2.5V/3.2/4.2Vreference voltage
JDREF	-	40	33	Ref. Resistor for Jack Detect	20K, 1% resistor to analog ground
NC	-	14	14	Not Connected	-
NC	-	15	15	Not Connected	-
NC	-	33	37	Not Connected	-
NC	-	43	43	Not Connected	-
NC	-	44	44	Not Connected	-
NC	-	45	45	Not Connected	-
NC	-	-	40	Not Connected	-
Total	-	12 pins	11 pins	-	-

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	ALC268/-VB1 (LQFP-48) Pin No	ALC268Q (QFN-48) Pin No.	Description	Characteristic Definition
AVDD1	I	25	25	Analog VDD (5V or 3.3V)	Analog power for mixer and amplifier
AVSS1	I	26	26	Analog GND	Analog ground for mixer and amplifier
AVDD2	I	38	38	Analog VDD (5V or 3.3V)	Analog power for DACs and ADCs
AVSS2	I	42	42	Analog GND	Analog ground for DACs and ADCs
DVDD	I	1	1	Digital VDD (3.3V)	Digital power
DVSS	I	4	-	Digital GND	Digital ground
DVDD-IO	I	9	3	Digital VDD (1.5V~3.3V)	Scalable digital power for HDA link
DVSS	I	7	7	Digital GND	Digital ground
DVDD	I	-	9	Digital VDD (3.3V)	Digital power
Total	-	8 pins	8 pins	-	-

7. High Definition Audio Link Protocol

7.1. Link Signals

The High Definition Audio (HDA) Link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 5 shows the basic concept of the HDA link protocol.

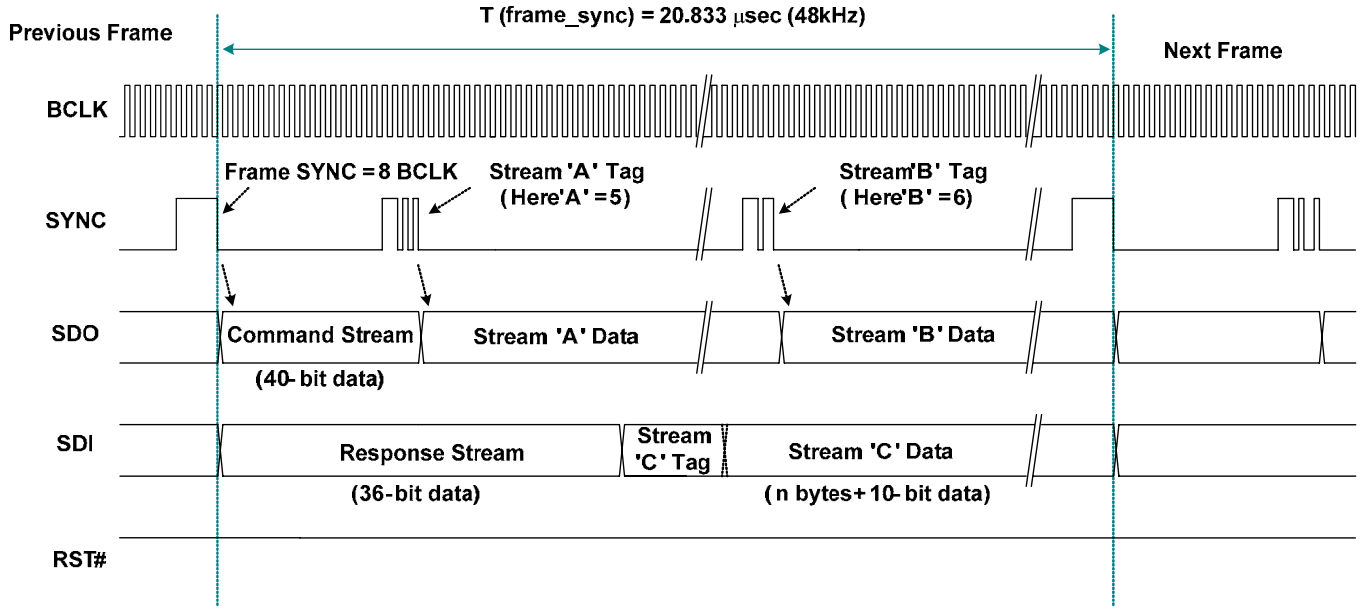


Figure 5. HDA Link Protocol

7.1.1. Signal Definitions

Table 5. Link Signal Definitions

Item	Description
BCLK	24.0MHz of bit clock sourced from the HDA controller and connecting to all codecs.
SYNC	48kHz of signal is used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs.
SDO	Serial data output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double-pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported.
SDI	Serial data input signal driven by the codec. It is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI, and up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID.
RST#	Active low reset signal. Asserted to reset the codec to default power on state. RST# is sourced from the HDA controller and connects to all codecs.

Table 6. HDA Signal Definitions

Signal Name	Source	Type for Controller	Description
BCLK	Controller	Output	Global 24.0MHz Bit Clock.
SYNC	Controller	Output	Global 48kHz Frame Sync and Outbound Tag Signal.
SDO	Controller	Output	Serial Data Output from Controller.
SDI	Codec/Controller	Input/Output	Serial Data Input from Codec. Weakly pulled down by the controller.
RST#	Controller	Output	Global Active Low Reset Signal.

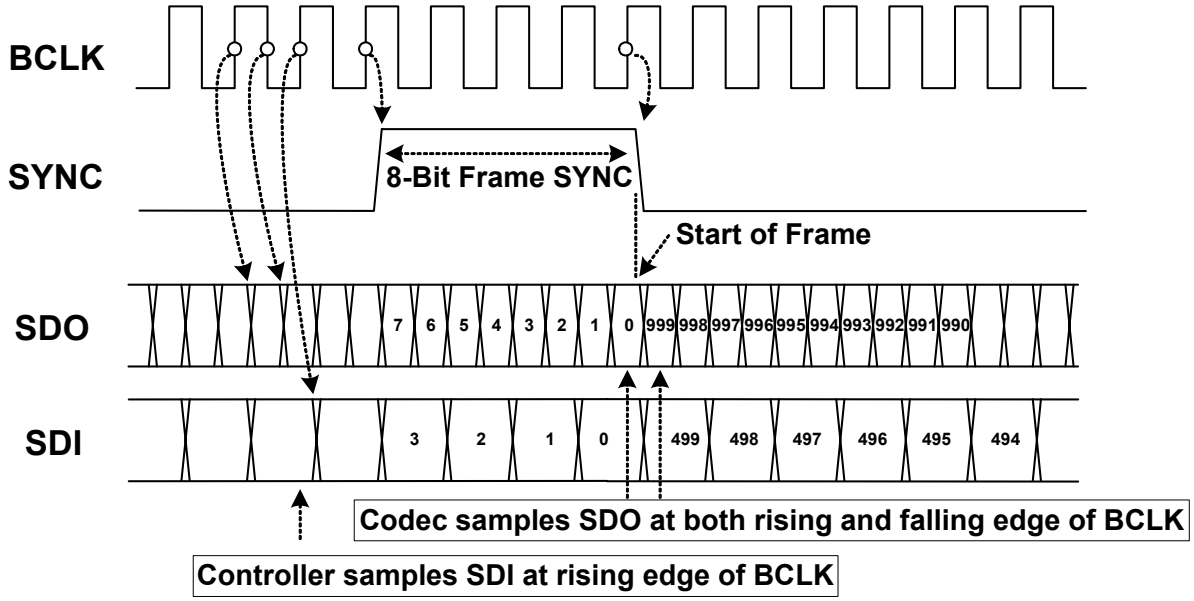


Figure 6. Bit Timing

7.1.2. Signaling Topology

The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0 and SDO1 are driven by controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 7 shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 14 describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 7 can be implemented concurrently in an HDA system. The ALC268 series are designed to receive a single SDO stream.

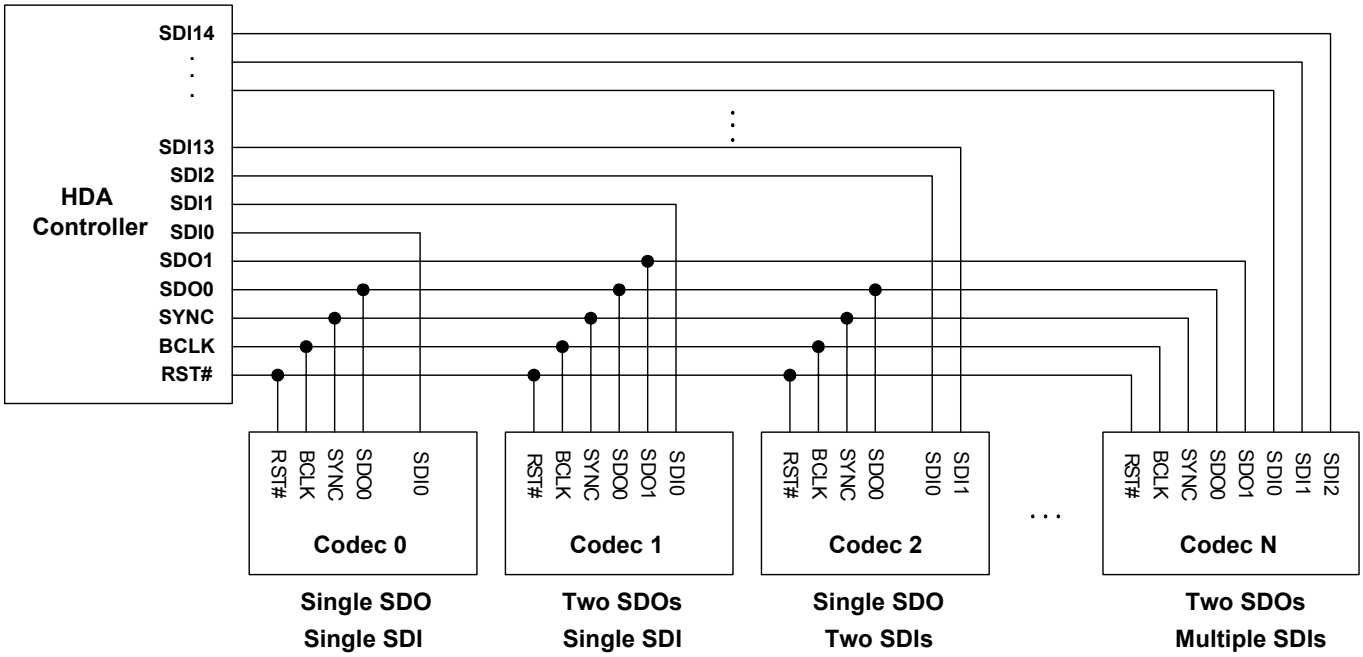


Figure 7. Signaling Topology

7.2. Frame Composition

7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-Bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be 2 blocks in the same stream to carry 96kHz samples (Figure 8).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-Bit preamble and 4-Bit stream ID (Figure 9).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

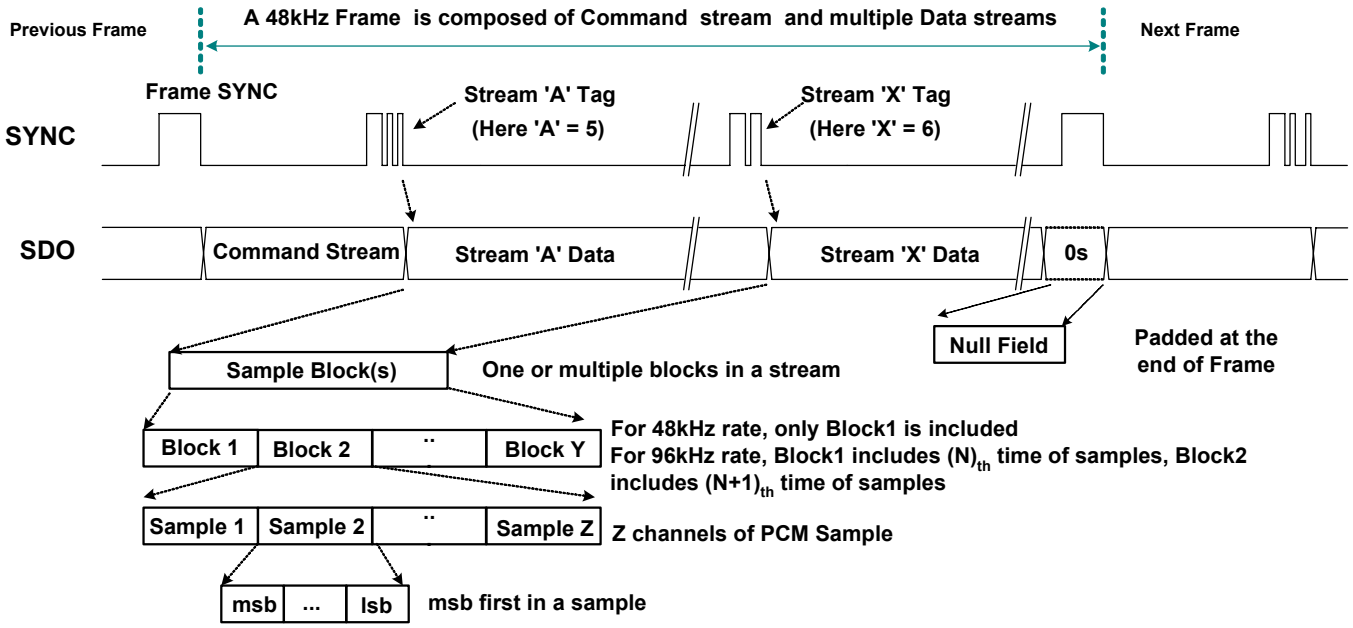


Figure 8. SDO Outbound Frame

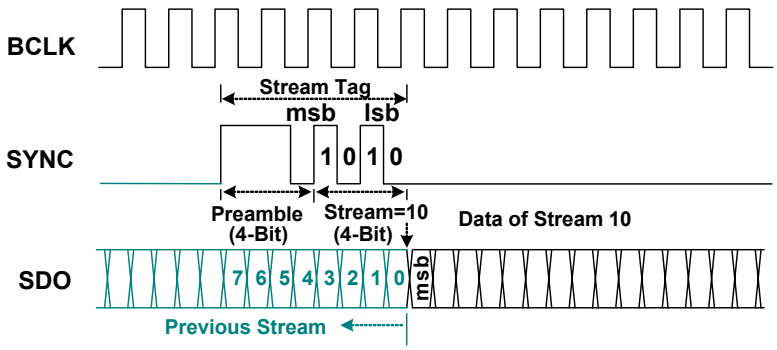


Figure 9. SDO Stream Tag is Indicated in SYNC

7.2.2. Outbound Frame – Multiple SDOs

The HDA controller allows two SDO signals to be used to stripe outbound data, completing transmission in less time to get more bandwidth. If software determines the target codec supports multiple SDO capability, it enables the 'Stripe Control' bit in the controller's Output Stream Control Register to initiate a specific stream (Stream 'A' in Figure 10) to be transmitted on multiple SDOs. In this case, the MSB of stream data is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a striped stream. The codec does not support multiple SDOs connected to SDO0.

To guarantee all codecs can determine their corresponding stream, the command stream is not striped. It is always transmitted on SDO0, and copied on SDO1.

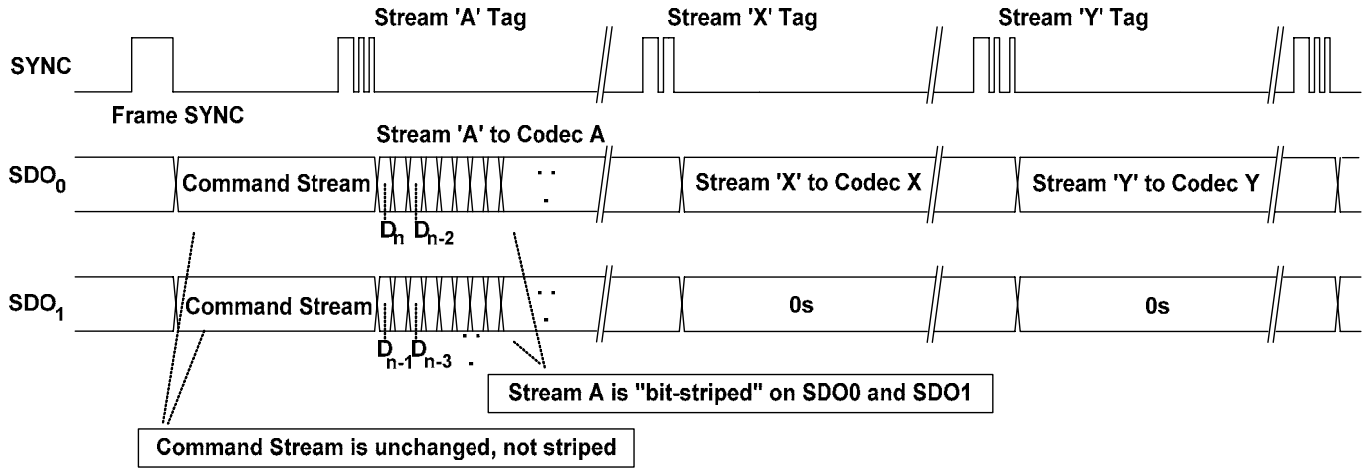


Figure 10. Striped Stream on Multiple SDOs

7.2.3. Inbound Frame – Single SDI

An Inbound Frame – A single SDI is composed of one 36-bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK (Figure 11).

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-bit stream tag, one 6-bit data length, and n-bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 12).

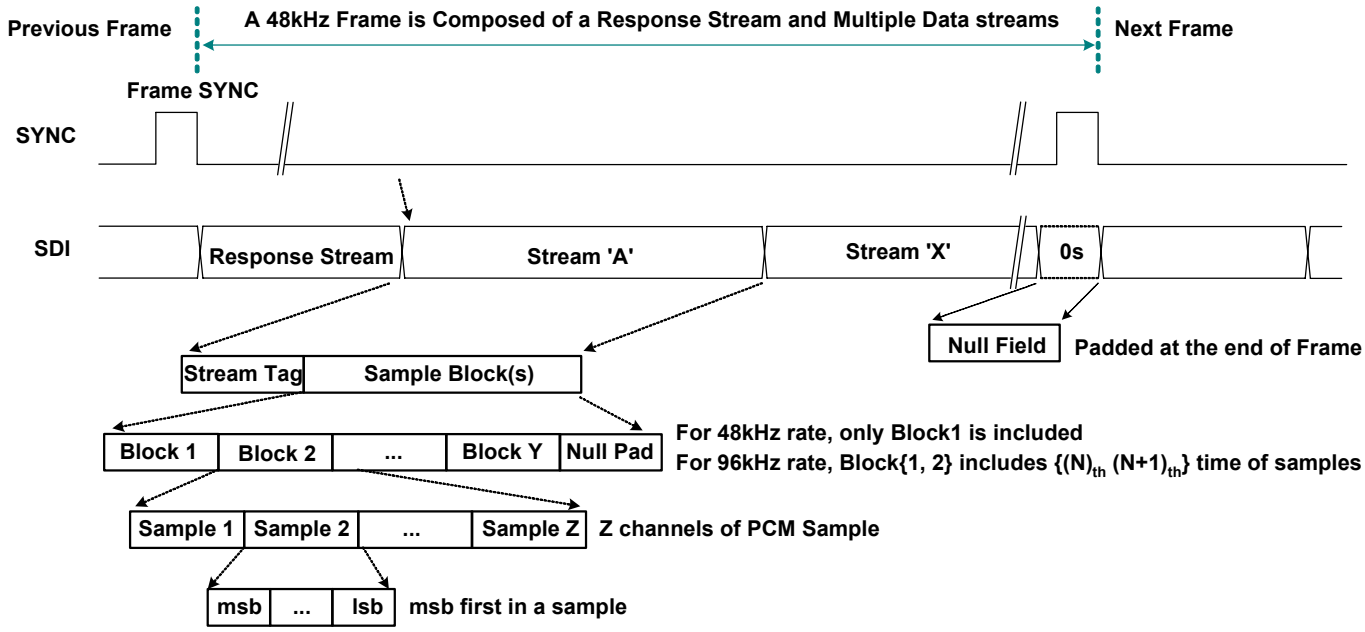


Figure 11. SDI Inbound Stream

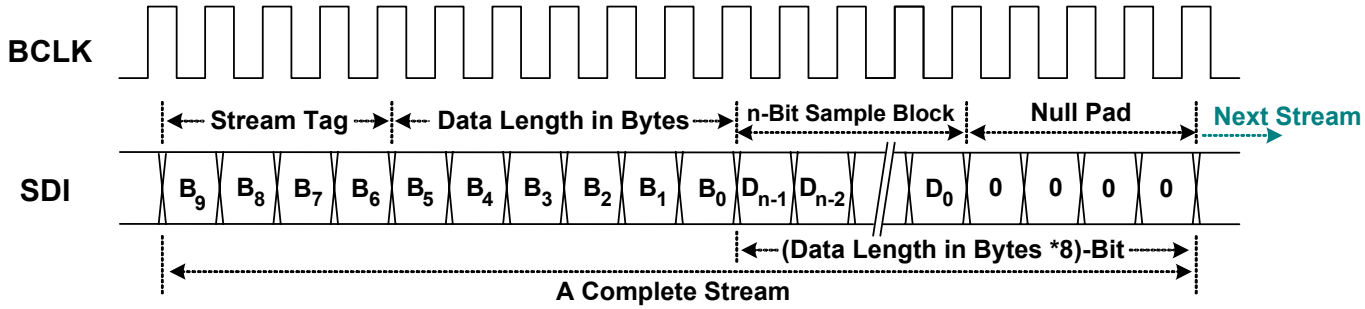


Figure 12. SDI Stream Tag and Data

7.2.4. Inbound Frame – Multiple SDIs

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data onto separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.

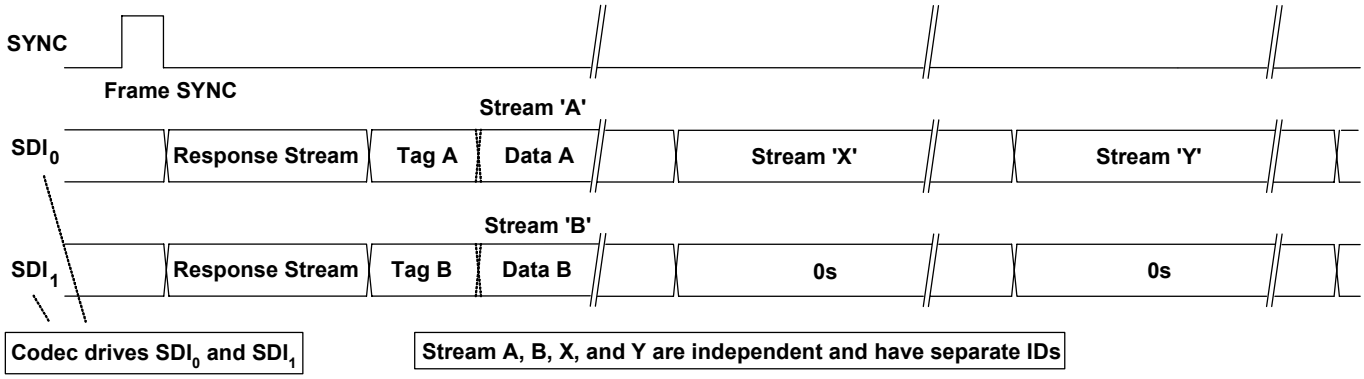


Figure 13. Codec Transmits Data Over Multiple SDIs

7.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable rates of sample are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 7, page 18, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 8, page 18, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames.

The cadence '12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)' interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence *and* interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame *and* interleave an empty frame between non-empty frames (Table 9, page 19).

Table 7. Defined Sample Rate and Transmission Rate

(Sub) Multiple	48kHz Base	44.1kHz Base
1/6	8kHz (1 sample block every 6 frames)	-
1/4	12kHz (1 sample block every 4 frames)	11.025kHz (1 sample block every 4 frames)
1/3	16kHz (1 sample block every 3 frames)	-
1/2	-	22.05kHz (1 sample block every 2 frames)
2/3	32kHz (2 sample blocks every 3 frames)	-
1	48kHz (1 sample block per frame)	44.1kHz (1 sample block per frame)
2	96kHz (2 sample blocks per frame)	88.2kHz (2 sample blocks per frame)
4	192kHz (4 sample blocks per frame)	176.4kHz (4 sample blocks per frame)

Table 8. 48kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence	Description
8kHz	YNNNNN (repeat)	One sample block is transmitted in every 6 frames
12kHz	YNNN (repeat)	One sample block is transmitted in every 4 frames
16kHz	YNN (repeat)	One sample block is transmitted in every 3 frames
32kHz	Y^2NN (repeat)	One sample block is transmitted in every 6 frames
48kHz	Y (repeat)	One sample block is transmitted in every 6 frames
96kHz	Y^2 (repeat)	Two sample blocks are transmitted in each frame
192kHz	Y^4 (repeat)	Four sample blocks are transmitted in each frame

N: No sample block in a frame
Y: One sample block in a frame
Y^x: X sample blocks in a frame

Table 9. 44.1kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence
11.025kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
22.05kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
44.1kHz	12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)
88.2kHz	12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-11^2- (repeat)
174.4kHz	12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-11^4- (repeat)

11.025kHz: {12}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN

{11}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN

{ - }=NNNN

22.050kHz: {12}=YNYNYNYNYNYNYNYNYNYNYNYN

{11}=YNYNYNYNYNYNYNYNYNYNYN

{ - }=NN

44.1kHz: 12- =Contiguous 12 frames containing 1 sample blocks each, followed by one frame with no sample block.

88.2kHz: 12^2- =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block.

176.4kHz: 12^4- =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block.

7.3. Reset and Initialization

There are two types of reset within an HDA link:

- Link Reset. Generated by assertion of the RST# signal, all codecs return to their power on state
- Codec Reset. Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

1. Link Reset

2. Codec Reset

3. Codec changes its power state (For example, hot docking a codec to an HDA system)

7.3.1. Link Reset

A link reset may be caused by 3 events:

1. The HDA controller asserts RST# for any reason (power up, or PCI reset)

2. Software initiates a link reset via the 'CRST' bit in the Global Control Register (GCR) of the HDA controller

3. Software initiates power management sequences. Figure 14, page 21, shows the 'Link Reset' timing including the 'Enter' sequence (❶~❺) and 'Exit' sequence (❻~❾)

Enter 'Link Reset':

❶ Software writes a 0 to the 'CRST' bit in the Global Control Register of the HDA controller to initiate a link reset

❷ As the controller completes the current frame, it does not signal the normal 8-Bit frame SYNC at the end of the frame

❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low

❹ The controller asserts the RST# signal to low, and enters the 'Link Reset' state

❺ All link signals driven by controller and codecs should be tri-state via internal pull-low resistors

Exit from 'Link Reset':

❻ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)

❼ Software is responsible for de-asserting RST# after a minimum of 100µsec BCLK running time (the 100µsec provides time for the codec PLL to stabilize)

❽ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC

❾ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC, it means the codec requests an initialization sequence)

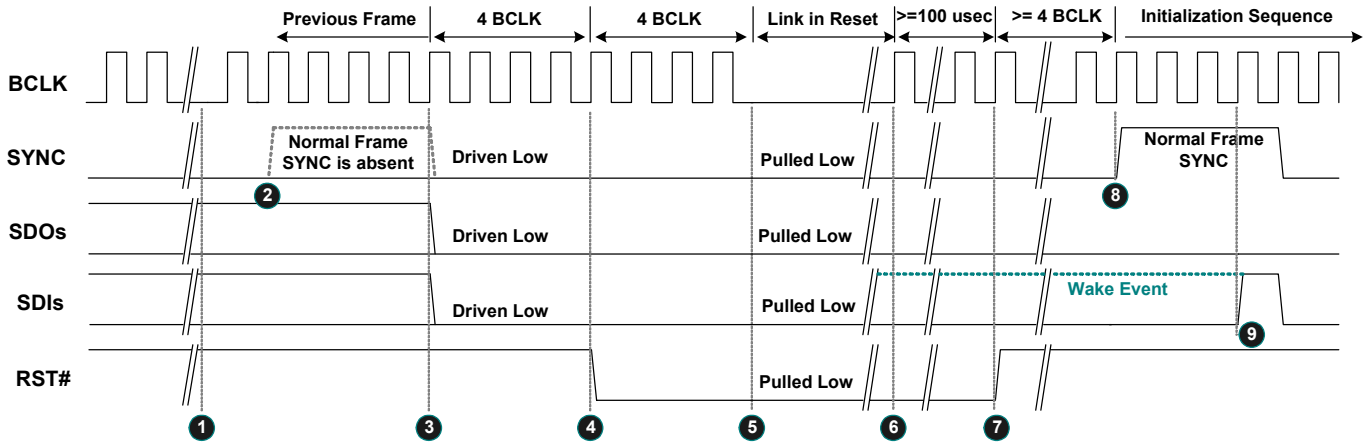


Figure 14. Link Reset Timing

7.3.2. Codec Reset

A 'Codec Reset' is initiated via the Codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

7.3.3. Codec Initialization Sequence

❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller.

❷ The codec will stop driving the SDI during this turnaround period.

❸❹❺❻ The controller drives SDI to assign a CAD to the codec.

❼ The controller releases the SDI after the CAD has been assigned.

❽ Normal operation state.

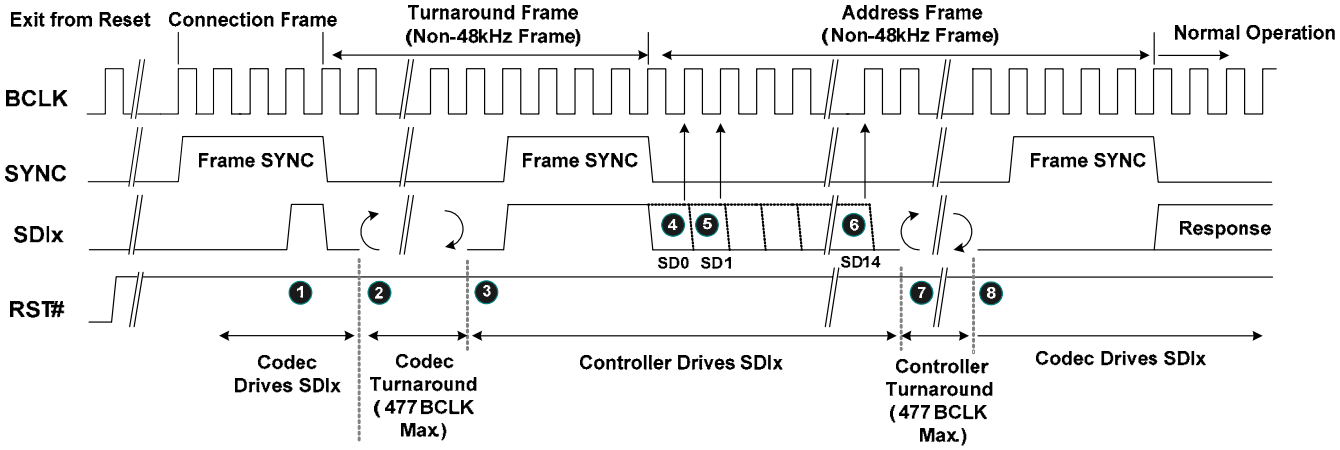


Figure 15. Codec Initialization Sequence

7.4. Verb and Response Format

7.4.1. Command Verb Format

There are two types of verbs: one with 4-Bit identifiers (4-Bit verbs) and 16-Bits of data, the other with 12-Bit identifiers (12-Bit verbs) and 8-Bits of data. Table 10 shows the 4-Bit verb structure of a command stream sent from the controller to operate the codec. Table 11 is the 12-Bit verb structure that gets and controls parameters in the codec.

Table 10. 40-Bit Commands in 4-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:16]	Bit [15:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

Table 11. 40-Bit Commands in 12-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:8]	Bit [7:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-bit Response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The 'Tag' in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

Table 12. Solicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:0]
Valid	Unsol=0	Reserved	Response

Table 13. Unsolicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:28]	Bit [27:0]
Valid	Unsol=1	Reserved	Tag	Response

Note: The response stream in the link protocol is 36-bits wide. The response is placed in the lower 32-bit field. Bit-35 is a 'Valid' bit to indicate the response is 'Ready'. Bit-34 is set to indicate that an unsolicited response was sent.

7.5. Power Management

The ALC268 does not support Wake-Up events when in low power mode. All power management state changes in widgets are driven by software. Table 14 shows the System Power State Definitions.

In the ALC268, all the widgets include output/input converters support power control. Software may have various power states depending on system configuration.

Table 15 indicates those nodes that support power management. To simplify power control, software can configure whole codec power states through the audio function (NID=01h). Output converters (DACs) and input converters (ADCs) have no individual power control to supply fine-grained power control.

Table 14. System Power State Definitions

Power States	Definitions
D0	All power on. Individual DACs and ADCs can be powered up or down as required.
D1	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, analog reference stays up.
D2	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, but analog reference off (D1 + analog reference off).
D3 (Hot)	Power still supplied. The codec stops the internal clock. State is maintained.
D3 (Cold)	All power removed. State lost.

Table 15. Power Controls in NID=01h

	Description	D0	D1	D2	D3 (Hot/Cold)	Link Reset
Audio Function (NID=01h)	LINK Response	Normal	Normal	Normal	PD	PD
	DACs	Normal	PD	PD	PD	PD
	ADCs	Normal	PD	PD	PD	PD
	All Headphone Drivers	Normal	Normal	PD	PD	Normal
	All Mixers	Normal	Normal	PD	PD	Normal
	All Reference	Normal	Normal	PD	PD	Normal

Note: PD=Powered Down

Table 16. Powered Down Conditions

Condition	Description
LINK Response powered down	Internal clock is stopped. SDATA-IN and S/PDIF-OUT are floated with pulled low 47K resistors internally. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied.
DAC powered down	Analog block and digital filter are powered down.
ADC powered down	Analog block and digital filter are powered down. The data on SDATA-IN is quiet.
Headphone Driver powered down	All headphone drivers are powered down.
Mixers powered down	All internal mixer widgets are powered down. The DC reference and VREFOUTx at individual pin complex are still alive.
Reference power down	All internal references, DC reference, and VREFOUTx at individual pin complexes are off.

8. Supported Verbs and Parameters

This chapter describes the Verbs and Parameters supported by various widgets in the ALC268. If a verb is not supported by the addressed widget, it will respond with 32 bits of '0'.

8.1. Verb – Get Parameters (Verb ID=F00h)

The 'Get Parameters' verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. Refer to section 7.4.1 Command Verb Format, page 23, to get detailed information about supported parameters.

Table 17. Verb – Get Parameters (Verb ID=F00h)

Get Parameter Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=00h	Verb ID=F00h	Parameter ID[7:0]

Codec Response Format

Response [31:0]
32-bit Response

Note: If the parameter ID is not supported, the returned response is 32 bits of '0'.

8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Table 18. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Codec Response Format

Bit	Description
31:16	Vendor ID=10Ech (Realtek's PCI vendor ID).
15:0	Device ID=0268h.

Note: The Root Node (NID=00h) supports this parameter.

8.1.2. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Table 19. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:20	MajRev. The major version number (in decimal) of the HDA Spec to which the ALC268 is fully compliant.
19:16	MinRev. The minor version number (in decimal) of the HDA Spec to which the ALC268 is fully compliant.
15:8	Revision ID. The vendor's revision number. 00h is for the first silicon version A, 01h is for the second version B, etc.
7:0	Stepping ID. The vendor's stepping number within the given Revision ID.

Note: The Root Node (NID=00h in the ALC268) supports this parameter.
For example the Revision ID=00h and Stepping ID=01h stand for the silicon is A1 version.

8.1.3. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node.

For function group nodes, it provides the total number of widgets associated with this function node.

Table 20. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:16	Starting Node Number. The starting node number in the sequential widgets.
15:8	Reserved. Read as 0's.
7:0	Total Number of Nodes. For a root node, the total number of function groups in the root node. For a function group, the total number of widget nodes in the function group.

8.1.4. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Table 21. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Codec Response Format

Bit	Description
31:9	Reserved. Read as 0's.
8	UnSol Capable. 0: Unsolicited response is not supported by this function group 1: Unsolicited response is supported by this function group
7:0	Function Group Type. 00h: Reserved 01h: Audio Function 02h: Modem Function 03h~7Fh: Reserved 80h~FFh: Vendor Defined Function.

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.5. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Table 22. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Codec Response Format

Bit	Description
31:17	Reserved. Read as 0's.
16	Beep Generator. A '1' indicates the presence of an integrated Beep generator within the Audio Function Group.
15:12	Reserved. Read as 0's.
11:8	Input Delay.
7:4	Reserved. Read as 0's.
3:0	Output Delay.

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.6. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Table 23. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:20	Widget Type. 0h: Audio Output 1h: Audio Input 2h: Mixer 3h: Selector 4h: Pin Complex 5h: Power Widget 6h: Volume Knob Widget 7h~Eh: Reserved Fh: Vendor defined audio widget
19:16	Delay. Samples delayed between the HDA link and widgets.
15:11	Reserved. Read as 0's.
10	Power Control. 0: Power state control is not supported on this widget 1: Power state is supported on this widget
9	Digital. 0: An analog input or output converter 1: A widget translating digital data between the HDA link and digital I/O (S/PDIF, I2S, etc.)
8	ConnList. Connection List. 0: Connected to HDA link. No Connection List Entry should be queried 1: Connection List Entry must be queried
7	UnsolCap. Unsolicited Capable. 0: Unsolicited response is not supported 1: Unsolicited response is supported
6	ProcWidget. Processing Widget. 0: No processing control 1: Processing control is supported
5	Reserved. Read as 0.
4	Format Override.
3	AmpParOvr, AMP Param Override.
2	OutAmpPre, Out AMP Present.
1	InAmpPre, In AMP Present.
0	Stereo. 0: Mono Widget 1: Stereo Widget

8.1.7. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameters in audio function provides default information about formats. Individual converters have their own parameters to provide supported formats if their 'Format Override' bit is set.

Table 24. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Codec Response Format

Bit	Description
31:21	Reserved. Read as 0's.
20	B32: Indicates whether 32-bit audio format is supported. 0: Not supported 1: Supported
19	B24: Indicates whether 24-bit audio format is supported. 0: Not supported 1: Supported
18	B20: Indicates whether 20-bit audio format is supported. 0: Not supported 1: Supported
17	B16: Indicates whether 16-bit audio format is supported. 0: Not supported 1: Supported
16	B8: Indicates whether 8-bit audio format is supported. 0: Not supported 1: Supported
15:12	Reserved. Read as 0's.
11	R12: Indicates whether 384kHz (=8*48kHz) rate is supported. 0: Not supported 1: Supported
10	R11: Indicates whether 192kHz (=4*48kHz) rate is supported. 0: Not supported 1: Supported
9	R10: Indicates whether 176.4kHz (=4*44.1kHz) rate is supported. 0: Not supported 1: Supported
8	R9: Indicates whether 96kHz (=2*48kHz) rate is supported. 0: Not supported 1: Supported
7	R8: Indicates whether 88.2kHz (=2*44.1kHz) rate is supported. 0: Not supported 1: Supported
6	R7: Indicates whether 48kHz rate is supported. 0: Not supported 1: Supported
5	R6: Indicates whether 44.1kHz rate is supported. 0: Not supported 1: Supported
4	R5: Indicates whether 32kHz (=2/3*48kHz) rate is supported. 0: Not supported 1: Supported
3	R4: Indicates whether 22.05kHz (=1/2*44.1kHz) rate is supported. 0: Not supported 1: Supported
2	R3: Indicates whether 16kHz (=1/3*48kHz) rate is supported. 0: Not supported 1: Supported
1	R2: Indicates whether 11.025kHz (=1/4*44.1kHz) rate is supported. 0: Not supported 1: Supported
0	R1: Indicates whether 8kHz (=1/6*48kHz) rate is supported. 0: Not supported 1: Supported

8.1.8. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the 'Format Override' bit is set.

Table 25. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Codec Response Format

Bit	Description
31:3	Reserved. Read as 0's.
2	AC3. 0: Not supported 1: Supported
1	Float32. 0: Not supported 1: Supported
0	PCM. 0: Not supported 1: Supported

Note: Input converters and output converters support this parameter.

8.1.9. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

Table 26. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's.
15:8	VREF Control Capability. '1' in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of AVDD.

7:6	5	4	3	2	1	0
Reserved	100%	80%	Reserved	Ground	50%	Hi-Z

Bit	Description
7	L-R Swap. Indicates the capability of swapping the left and rights.
6	Balanced I/O Pin. '1' indicates this pin complex has balanced pins.
5	Input Capable. '1' indicates this pin complex supports input.
4	Output Capable. '1' indicates this pin complex supports output.
3	Headphone Drive Capable. '1' indicates this pin complex has an amplifier to drive a headphone.
2	Presence Detect Capable. '1' indicates this pin complex can detect whether there is anything plugged in.
1	Trigger Required. '1' indicates whether a software trigger is required for an impedance measurement.
0	Impedance Sense Capable. '1' indicates this pin complex can perform analog sense on the attached device to determine its type.

Note: Only Pin Complex widgets support this parameter.

8.1.10. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the 'AMP Param Override' bit is set.

Table 27. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Codec Response Format

Bit	Description
31	(Input) Mute Capable.
30:23	Reserved. Read as 0.
22:16	Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. '0' indicates a step of 0.25dB. '127' indicates a step of 32dB.
15	Reserved. Read as 0.
14:8	Number of Steps. Indicates the number of steps in the gain range. '0' means the gain is fixed.
7	Reserved. Read as 0.
6:0	Offset. Indicates which step is 0dB.

8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the 'AMP Param Override' bit is set.

Table 28. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Codec Response Format

Bit	Description
31	(Output) Mute Capable.
30:23	Reserved. Read as 0.
22:16	Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. '0' indicates a step of 0.25dB. '127' indicates a step of 32dB.
15	Reserved. Read as 0.
14:8	Number of Steps. Indicates the number of steps in the gain range. '0' means the gain is fixed.
7	Reserved. Read as 0.
6:0	Offset. Indicates which step is 0dB.

8.1.12. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

Table 29. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0.
7	Short Form. 0: Short Form 1: Long Form
6:0	Connect List Length. Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (Not a MUX widget).

8.1.13. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Table 30. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Codec Response Format

Bit	Description
31:4	Reserved. Read as 0's.
3	D3Sup. 1: Power state D3 is supported.
2	D2Sup. 1: Power state D2 is supported.
1	D1Sup. 1: Power state D1 is supported.
0	D0Sup. 1: Power state D0 is supported.

8.1.14. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Table 31. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's.
15:8	NumCoeff. Number of Coefficient.
7:1	Reserved. Read as 0's.
0	Benign. 0: Processing unit is not linear and time invariant 1: Processing unit is linear and time invariant

8.1.15. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Table 32. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Codec Response Format

Bit	Description
31	GPIWake=0. The ALC268 does not support GPIO wake up function.
30	GPIUnsol=1. The ALC268 supports GPIO unsolicited response.
29:24	Reserved. Read as 0's.
23:16	NumGPIs=00h. No GPI pin is supported.
15:8	NumGPOs=00h. No GPO pin is supported.
7:0	NumGPIOs=04h. Two GPIO pins are supported.

8.1.16. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Table 33. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Codec Response Format for NID=21h (Volume Control Knob)

Bit	Description
31:8	Reserved. Read as 0's.
7	Delta. 0: Software cannot modify the Volume Control Knob volume 1: Software can write a base volume to the Volume Control Knob
6:0	NumSteps. The number of steps in the range of the Volume Control Knob.

Note: The ALC268 does not support volume control knob.

8.2. Verb – Get Connection Select Control (Verb ID=F01h)

Table 34. Verb – Get Connection Select Control (Verb ID=F01h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F01h	0's

Codec Response Format

Response [31:0]
Bit[7:0] are Connection Index

Codec Response for Multiplexer Widget NID=23h

Bit	Description
31:8	0's.
7:0	Connection Index Currently Set (Default value is 00h). 00h: Pin Widget NID=18h (port-B) 01h: Pin Widget NID=19h (port-F) 02h: Pin Widget NID=1Ah (port-C) 03h: Pin Widget NID=1Ch (Analog CD-IN) 04h: Pin Widget NID=14h (port-D) 05h: Pin Widget NID=15h (port-A) 06h: Pin Widget NID=12h (Digital MIC 1&2) Other: Reserved

Codec Response for Multiplexer Widget NID=24h

Bit	Description
31:8	0's.
7:0	Connection Index Currently Set (Default value is 00h). 00h: Pin Widget NID=18h (port-B) 01h: Pin Widget NID=19h (port-F) 02h: Pin Widget NID=1Ah (port-C) 03h: Pin Widget NID=1Ch (Analog CD-IN) 04h: Pin Widget NID=14h (port-D) 05h: Pin Widget NID=15h (port-A) 06h: Pin Widget NID=13h (Digital MIC 3&4) Other: Reserved

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.3. Verb – Set Connection Select (Verb ID=701h)

Table 35. Verb – Set Connection Select (Verb ID=701h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=701h	Select Index [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Note: Only MUX NID-23h and 24h support this verb.

8.4. Verb – Get Connection List Entry (Verb ID=F02h)

Table 36. Verb – Get Connection List Entry (Verb ID=F02h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F02h	Offset Index – N[7:0]

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=07h ADC

Bit	Description
31:8	Connection List Entry (N+3), (N+2), and (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 24h (Sum Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=08h ADC

Bit	Description
31:8	Connection List Entry (N+3), (N+2), and (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 23h (Sum Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Eh)

Bit	Description
31:24	Connection List Entry (N). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 03h (LOUT2 DAC) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 02h (LOUT1 DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Fh)

Bit	Description
31:24	Connection List Entry (N). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 1Dh (PCBEEP) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 02h (LOUT1 DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=10h)

Bit	Description
31:24	Connection List Entry (N). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 1Dh (PCBEEP) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 03h (LOUT2 DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID =18h (MIC1, port-B), 1Ah (LINE1, port-C)

Bit	Description
31:24	Connection List Entry (N+3). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 00h.
7:0	Connection List Entry (N). Returns 02h (LOUT1 DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID =14h (LOUT, port-D)

Bit	Description
31:24	Connection List Entry (N+3). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 00h.
7:0	Connection List Entry (N). Returns 0Fh (Mixer) for N=0~3. Returns 00h for N>3.

Codec Response for NID =15h (HPOUT, port-A)

Bit	Description
31:24	Connection List Entry (N+3). Returns 00h.
23:16	Connection List Entry (N+2). Returns 00h.
15:8	Connection List Entry (N+1). Returns 00h.
7:0	Connection List Entry (N). Returns 10h (Mixer) for N=0~3. Returns 00h for N>3.

Codec Response for NID=16h (Pin Widget: MONO-OUT)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), and (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 0Eh for N=0~3. Returns 00h for N>3.

Codec Response for NID=1Eh (Pin Widget: S/PDIF-OUT)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), and (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 06h (S/PDIF-OUT Converter) for N=0~3. Returns 00h for N>3.

Codec Response for NID=23h (MUX Widget)

Bit	Description
31:24	Connection List Entry (N+3). Returns 1Ch (Pin Complex – CD) for N=0~3. Returns 00h for N>3.
23:16	Connection List Entry (N+2). Returns 1Ah (Pin Complex – LINE1, port-C) for N=0~3. Returns 12h (Pin Complex – Digital MIC 1&2) for N=4~7. Returns 00h for N>7.
15:8	Connection List Entry (N+1). Returns 19h (Pin Complex – MIC2, port-F) for N=0~3. Returns 15h (Pin Complex – HPOUT, port-A) for N=4~7. Returns 00h for N>7.
7:0	Connection List Entry (N). Returns 18h (Pin Complex – MIC1, port-B) for N=0~3. Returns 14h (Pin Complex – LOUT, port-D) for N=4~7. Returns 00h for N>7.

Codec Response for NID=24h (MUX Widget)

Bit	Description
31:24	Connection List Entry (N+3). Returns 1Ch (Pin Complex – CD) for N=0~3. Returns 00h for N>3.
23:16	Connection List Entry (N+2). Returns 1Ah (Pin Complex – LINE1, port-C) for N=0~3. Returns 13h (Pin Complex – Digital MIC 3&4) for N=4~7. Returns 00h for N>7.
15:8	Connection List Entry (N+1). Returns 19h (Pin Complex – MIC2, port-F) for N=0~3. Returns 15h (Pin Complex – HPOUT, port-A) for N=4~7. Returns 00h for N>7.
7:0	Connection List Entry (N). Returns 18h (Pin Complex – MIC1, port-B) for N=0~3. Returns 14h (Pin Complex – LOUT, port-D) for N=4~7. Returns 00h for N>7.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.5. Verb – Get Processing State (Verb ID=F03h)

Table 37. Verb – Get Processing State (Verb ID=F03h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F03h	0's

Codec Response Format

Response [31:0]
32-bit response

Codec Response for All NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.6. Verb – Set Processing State (Verb ID=703h)

Table 38. Verb – Set Processing State (Verb ID=703h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=703h	Processing State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.7. Verb – Get Coefficient Index (Verb ID=Dh)

Table 39. Verb – Get Coefficient Index (Verb ID=Dh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=Dh	0's

Codec Response Format

Response [31:0]
Bit [15:0] are Coefficient Index

Codec Response for NID=20h (Realtek Vendor Registers)

Bit	Description
31:16	Reserved. Read as 0's.
15:0	Coefficient Index.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.8. Verb – Set Coefficient Index (Verb ID=5h)

Table 40. Verb – Set Coefficient Index (Verb ID=5h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=5h	Coefficient Index [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

Table 41. Verb – Get Processing Coefficient (Verb ID=Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=Ch	0's

Codec Response Format

Response [31:0]
Processing Coefficient [15:0]

Codec Response for NID=20h (Realtek Vendor Registers)

Bit	Description
31:16	Reserved. Read as 0's.
15:0	Processing Coefficient.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.10. Verb – Set Processing Coefficient (Verb ID=4h)

Table 42. Verb – Set Processing Coefficient (Verb ID=4h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=4h	Coefficient [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

Table 43. Verb – Get Amplifier Gain (Verb ID=Bh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=Bh	'Get' payload [15:0]

Codec Response Format

Response [31:0]
Bit[7:0] are responsible for 'Get'

'Get' Payload in Command Bit[15:0]

Bit	Description
15	Get Input/Output. 0: Input amplifier gain is requested 1: Output amplifier gain is requested
14	Reserved. Read as 0.
13	Get Left/Right. 0: Right amplifier gain is requested 1: Left amplifier gain is requested
12:4	Reserved. Read as 0's.
3:0	Index[3:0] for Input Source. Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored.

Codec Response for NID=02h (LOUT1 DAC) and 03h (LOUT2 DAC)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': 6-bit control specifying the volume from–64dB~ 0dB in 1dB step.

Node	Gain[6:0] (Default)	Gain Range
LOUT1 DAC(NID=02h)	1000000b=40h (0dB)	–64dB~0dB in 1dB step
LOUT2 DAC (NID=03h)	1000000b=40h (0dB)	–64dB~0dB in 1dB step

Codec Response for NID=0Eh (MONO Sum Widgets)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute; 1: Mute

Node	Index[3:0]=0 (from LOUT1) Default of Bit [7]	Index[3:0]=Other
MONO Sum (NID=0Eh)	0 (Unmute)	0

	Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 4 (No Output Amplifier Gain).

Codec Response for NID=0Fh (LINE-OUT Sum Widgets)

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>31:8</td><td>0’s.</td></tr>
<tr><td>7</td><td>Payload[15] is 0 in ‘Get Amplifier Gain’: Input Amplifier Mute. 0: Unmute; 1: Mute
<table>
<tr><th rowspan="2">Node</th><th>Index[3:0]=0 (from LOUT1)</th><th>Index[3:0]=1 (from BEEP)</th><th rowspan="2">Index[3:0]=Other</th></tr>
<tr><th>Default of Bit [7]</th><th>Default of Bit [7]</th></tr>
<tr><td>LINE-OUT Sum</td><td>0 (Unmute)</td><td>1 (Mute)</td><td>0</td></tr>
</table>
Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0 (No Output Amplifier Mute).</td></tr>
<tr><td>6:0</td><td>Payload[15] is 0 in ‘Get Amplifier Gain’: Read as 0’s (No Input Amplifier Gain).
Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0’s (No Output Amplifier Gain).</td></tr>
</table>

Codec Response for NID=10h (HP-OUT Sum Widgets)

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>31:8</td><td>0’s.</td></tr>
<tr><td>7</td><td>Payload[15] is 0 in ‘Get Amplifier Gain’: Input Amplifier Mute. 0: Unmute; 1: Mute
<table>
<tr><th rowspan="2">Node</th><th>Index[3:0]=0 (from LOUT2)</th><th>Index[3:0]=1 (from BEEP)</th><th>Index[3:0]=2 (from LOUT1)</th><th rowspan="2">Index[3:0]=Other</th></tr>
<tr><th>Default of Bit [7]</th><th>Default of Bit [7]</th><th>Default of Bit [7]</th></tr>
<tr><td>LINE-OUT Sum</td><td>1 (Mute)</td><td>1 (Mute)</td><td>1 (Mute)</td><td>0</td></tr>
</table>
Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0 (No Output Amplifier Mute).</td></tr>
<tr><td>6:0</td><td>Payload[15] is 0 in ‘Get Amplifier Gain’: Read as 0’s (No Input Amplifier Gain).
Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0’s (No Output Amplifier Gain).</td></tr>
</table>

Codec Response for NID=18h (MIC1, port-B) and 1Ah (LINE1, port-C)

Bit	Description
31:8	0’s.
7	Payload[15] is 0 in ‘Get Amplifier Gain’: Read as 0 (No Input Amplifier Mute). Payload[15] is 1 in ‘Get Amplifier Gain’: Output Amplifier Mute. 0:Unmute; 1:Mute (Default=1)
6:0	Payload[15] is 0 in ‘Get Amplifier Gain’: Input Amplifier Gain [6:0]. The volume 0dB/20dB/40dB in 20dB per step (Default=0, 0dB). Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0’s (No Output Amplifier Gain).

Codec Response for NID=19h (MIC2, port-F)

Bit	Description
31:8	0’s.
7	Payload[15] is 0 in ‘Get Amplifier Gain’: Read as 0 (No Input Amplifier Mute). Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in ‘Get Amplifier Gain’: Input Amplifier Gain [6:0]. The volume 0dB/20dB/40dB in 20dB per step (Default=0, 0dB). Payload[15] is 1 in ‘Get Amplifier Gain’: Read as 0’s (No Output Amplifier Gain).

Codec Response for NID=14h (LINE-OUT, port-D)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': Output Amplifier Mute. 0:Unmute; 1:Mute (Default=1)
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Gain).

Codec Response for NID=15h (HP-OUT, port-A)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': Output Amplifier Mute. 0:Unmute; 1:Mute (Default=1)
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Gain).

Codec Response for NID=1Dh (PCBEEP)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0] specifying the volume from –24dB to 0dB in 3dB per step (Default=0000001b, -21dB). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Mute).

Codec Response for NID=12h (Digital MIC DMIC-12) and 13h (Digital MIC DMIC-34)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Gain).

Codec Response for NID=16h (MONO-OUT)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': Output Amplifier Mute. 0:Unmute; 1:Mute (Default=1)
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Gain).

Codec Response for NID=23h and 24h (Multiplexer widgets in front of ADCs)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Mute for all index). Payload[15] is 1 in 'Get Amplifier Gain': Output Amplifier Mute. 0:Unmute; 1:Mute (Default=1)
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain for all index). Payload[15] is 1 in 'Get Amplifier Gain': Output Amplifier Gain [6:0] specifying the volume from –16.5dB to 30dB in 1.5dB per step (Default=0000001b, -15dB).

Codec Response to Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

Table 44. Verb – Set Amplifier Gain (Verb ID=3h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=3h	'Set' payload [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
15	Set Output Amp. 1 indicates output amplifier gain will be set.
14	Set Input Amp. 1 indicates input amplifier gain will be set.
13	Set Left Amp. 1 indicates left amplifier gain will be set.
12	Set Right Amp. 1 indicates right amplifier gain will be set.
11:8	Index Offset (for input amplifiers on Sum widgets and Selector Widgets). 5 bits index offset in connection list is used to select which input gain will be set on a mixer or a multiplexer widget. The index is ignored if the node is not a mixer or a multiplexer widget, or the 'Set Input Amp' bit is not set.
7	Mute. 0: Unmute 1: Mute (-∞gain)
6:0	Gain[6:0]. A 7-bit step value specifying the amplifier gain.

8.13. Verb – Get Converter Format (Verb ID=Ah)

Table 45. Verb – Get Converter Format (Verb ID=Ah)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Bit[15:0] are converter format

Codec Response for NID=02h, 03h, 06h (Output Converters: LOUT1 DAC, LOUT2 DAC, S/PDIF-OUT).
Codec Response for NID=07h, 08h (Input Converters: MIC ADC, LINE ADC)

Bit	Description
31:16	Reserved. Read as 0.
15	Stream Type (TYPE). 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT). 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved.
10:8	Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 The ALC268 does not support Divisor. Always read as 000b.
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels …… 15: 16 channels

	BASE	MULT	DIV	BITS	Sample Rate
NID=02h (LOUT1 DAC)	0	000b, 001b, 011b	000b	001b, 010b, 011b	48K, 96K,192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=03h (LOUT2 DAC)	0	000b, 001b, 011b	000b	001b, 010b, 011b	48K, 96K,192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=06h (S/PDIF-OUT)	0	000b, 001b, 011b	000b	001b, 010b, 011b, 100b	48K, 96K, 192K
	1	000b, 001b	000b	001b, 010b, 011b, 100b	44.1K, 88.2K
NID=07h (MIC ADC)	0	000b, 001b	000b	001b, 010b, 011b	48K, 96K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=08h (LINE ADC)	0	000b, 001b	000b	001b, 010b, 011b	48K, 96K
	1	000b	000b	001b, 010b, 011b	44.1K

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.14. Verb – Set Converter Format (Verb ID=2h)

Table 46. Verb – Set Converter Format (Verb ID=2h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=2h	Set format [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
31:16	Reserved. Read as 0.
15	Stream Type (TYPE). 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT). 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved
10:8	Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels …… 15: 16 channels

8.15. Verb – Get Power State (Verb ID=F05h)

Table 47. Verb – Get Power State (Verb ID=F05h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Power State [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:6	Reserved. Read as 0's.
5:4	PS-Act. Actual Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set.
3:2	Reserved. Read as 0's.
1:0	PS-Set. Set Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Set controls the current power setting of the referenced node.

Note: Specific blocks will be powered down in each power state. Refer to section 7.5 Power Management, page 24.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.16. Verb – Set Power State (Verb ID=705h)

Table 48. Verb – Set Power State (Verb ID=705h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=705h	Power State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Power State' in Command Bit[7:0]

Bit	Description
7:6	Reserved. Read as 0's.
5:4	PS-Act. Actual Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3 PS-Act indicates the actual power state of the referenced node.
3:2	Reserved. Read as 0's.
1:0	PS-Set. Set Power State [1:0]. 00: Power state is D0 01: Power state is D1 10: Power state is D2 11: Power state is D3

8.17. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Table 49. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F06h	0's

Codec Response Format

Response [31:0]
Stream & Channel [7:0]

Codec Response for NID=02h, 03h, 06h (Output Converters: LOUT1 DAC, LOUT2 DAC, S/PDIF-OUT).
Codec Response for NID=07h, 08h (Input Converters: MIC ADC, LINE ADC)

Bit	Description
31:8	Reserved. Read as 0's.
7:4	Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
3:0	Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.18. Verb – Set Converter Stream, Channel (Verb ID=706h)

Table 50. Verb – Set Converter Stream, Channel (Verb ID=706h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=706h	Stream & Channel [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Stream and Channel' in Command Bit[7:0]

Bit	Description
31:8	Reserved. Read as 0's.
7:4	Set Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
1:0	Set Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel.

Note: This verb assigns stream and channel for output converters (NID=02h, 03h, 06h) and input converters (NID=07h, 08h). Other widgets will ignore this verb.

8.19. Verb – Get Pin Widget Control (Verb ID=F07h)

Table 51. Verb – Get Pin Widget Control (Verb ID=F07h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F07h	0's

Codec Response Format

Response [31:0]
Pin Control [7:0]

Codec Response for pin widget NID=12h (DMIC-12), 13h (DMIC-34), 14h (LINE-OUT), 15h (HP-OUT), 16h (MONO), 18h (MIC1), 19h (MIC2), 1Ah (LINE1), 1Ch (CD-IN), 1Dh (PCBEEP), and 1Eh (S/PDIF-OUT)

Bit	Description
31:1	Reserved. Read as 0's.
7	H-Phn Enable (Headphone Amplifier Enable, EN_AMP for an I/O unit). 0: Disabled 1: Enabled *Note: Only HP-OUT (NID=15h) and LINE-OUT (NID=14h) support the headphone amplifier.*
6	Out Enable (Output Buffet Enable, EN_OBUF for an I/O unit). 0: Disabled 1: Enabled *Note: DMIC-12 (NID=12h), DMIC-34 (NID=13h), MIC2 (NID=19h), CD-IN (NID=1Ch), and PCBEEP (NID=1Dh) do not support output.*
5	In Enable (Input Buffer Enable, EN_IBUF for an I/O unit). 0: Disabled 1: Enabled *Note: MONO-OUT (NID-16h) does not support input.*
4:3	Reserved.
2:0	VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved *Note: Only MIC1 (NID=18h), MIC2 (NID=19h), and LINE1 (NID=1Ah) support reference voltage outputs.*

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.20. Verb – Set Pin Widget Control (Verb ID=707h)

Table 52. Verb – Set Pin Widget Control (Verb ID=707h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=707h	Pin Control [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Pin Control' in command [7:0]: pin widget NID=12h (DMIC-12), 13h (DMIC-34), 14h (LINE-OUT), 15h (HP-OUT), 16h (MONO), 18h (MIC1), 19h (MIC2), 1Ah (LINE1), 1Ch (CD-IN), 1Dh (PCBEEP) and 1Eh (S/PDIF-OUT)

Bit	Description
31:1	Reserved. Read as 0's.
7	H-Phn Enable. 0: Disabled 1: Enabled *Note: Only HP-OUT (NID=15h) and LINE-OUT (NID=14h) support the headphone amplifier.*
6	Out Enable. 0: Disabled 1: Enabled *Note: DMIC-12 (NID=12h), DMIC-34 (NID=13h), MIC2 (NID=19h), CD-IN (NID=1Ch), and PCBEEP (NID=1Dh) do not support output.*
5	In Enable (Input Buffer Enable, EN_IBUF for an I/O unit). 0: Disabled 1: Enabled *Note: MONO-OUT (NID-16h) does not support input.*
4:	Reserved.
2:0	VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD) 101b: 100% of AVDD 110b~111b: Reserved *Note: Only MIC1 (NID=18h), MIC2 (NID=19h), and LINE1 (NID=1Ah) support reference voltage outputs.*

8.21. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Determines whether a widget is enabled to send an unsolicited response. An HDA codec can use an unsolicited response to inform software of a real-time event.

Table 53. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F08h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (GPIO in Audio Function Group), 14h~16h (port jack detect), 18h~1Bh (port jack detect)

Bit	Description
31:8	Reserved. Read as 0's.
7	Unsolicited Response is Enabled. 0: Disabled 1: Enabled
6:4	Reserved. Read as 0's.
3:0	Assigned Tag for Unsolicited Response. The tag[3:0] is assigned by software to determine which widget generates unsolicited responses.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.22. Verb – Set Unsolicited Response Control (Verb ID=708h)

Enable a widget to generate an unsolicited response.

Table 54. Verb – Set Unsolicited Response Control (Verb ID=708h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=708h	EnableUnsol [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'EnableUnsol' in Command Bit[7:0]
For NID=01h (GPIO in Audio Function Group), 14h~16h (port jack detect), 18h~1Bh (port jack detect)

Bit	Description
31:8	Reserved. Read as 0's.
7	Enable Unsolicited Response. 0: Disable 1: Enable
6:4	Reserved. Read as 0's.
3:0	Tag for Unsolicited Response. Tag[3:0] is defined by software to assign a 4-bit tag for nodes that are enabled to generate unsolicited responses.

8.23. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

Table 55. Verb – Get Pin Sense (Verb ID=F09h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F09h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response: Pin widget 14h (LINE-OUT), 15h (HP-OUT), 18h (MIC1), 19h (MIC2), 1Ah (LINE1)

Bit	Description
31	Presence Detect Status. 0: No device is attached to the pin 1: Device is attached to the pin
30:0	Measured Impedance. *Note: The ALC268 does not support impedance sensing. Read as 0's.*

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.24. Verb – Execute Pin Sense (Verb ID=709h)

Table 56. Verb – Execute Pin Sense (Verb ID=709h)

Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=709h	Right Channel[0]

Codec Response Format

Response [31:0]
0's for all nodes

'Payload' in Command Bit[7:0]

Bit	Description
7:1	Reserved. Read as 0's.
0	Right (Ring) Channel Select. 0: Sense Left channel (Tip) 1: Sense Right channel (Ring)

Note: The ALC268 does not support 'Execute Pin Sense' and will ignore this verb and respond with 0's.

8.25. Verb – Get Configuration Default (Verb ID=F1Ch)

Read the 32-bit sticky register for each Pin Widget configured by software.

Table 57. Verb – Get Configuration Default (Verb ID=F1Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F1Ch	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for Pin Widget: NID=14h (LINE-OUT), 15h (HP-OUT), 16h (MONO-OUT), 18h (MIC1), 19h (MIC2), 1Ah (LINE1), 1Ch (CD-IN), 1Dh (PCBEEP), 1Eh (S/PDIF-OUT), 12h (DMIC-12), and 13h (DMIC-34)

Bit	Description
31:0	32-bit configuration information for each pin widget.

Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).

8.26. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions for the Pin Widgets 14h~1Bh and 1Eh~1Fh such as placement and expected default device.

Table 58. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=71Ch, 71Dh, 71Eh, 71Fh	Label [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Note: Supported by Pin Widget NID=14h (LINE-OUT), 15h (HP-OUT), 16h (MONO-OUT), 18h (MIC1), 19h (MIC2), 1Ah (LINE1), 1Ch (CD-IN), 1Dh (PCBEEP), 1Eh (S/PDIF-OUT), 12h (DMIC-12), and 13h (DMIC-34). Other widgets will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.27. Verb – Get BEEP Generator (Verb ID=F0Ah)

Table 59. Verb – Get BEEP Generator (Verb ID=F0Ah)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F1Bh	0's

Codec Response Format

Response [31:0]
Divider [7:0]

'Response' for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:0	Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48kHz/(255*4)=47Hz. The highest tone is 48kHz/(1*4)=12kHz. A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.28. Verb – Set BEEP Generator (Verb ID=70Ah)

Table 60. Verb – Set BEEP Generator (Verb ID=70Ah)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=71Bh	Divider [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Divider' in Set Command

Bit	Description
31:8	Reserved.
7:0	Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48kHz/(255*4)=47Hz. The highest tone is 48kHz/(1*4)=12kHz. A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input.

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.29. Verb – Get GPIO Data (Verb ID=F15h)

Table 61. Verb – Get GPIO Data (Verb ID=F15h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F15h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:4	GPIO[7:4] Data. Not supported in the ALC268.
3:0	GPIO[3:0] Data. The value written (output) or sensed (input) on the corresponding pin if it is enabled.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.30. Verb – Set GPIO Data (Verb ID=715h)

Table 62. Verb – Set GPIO Data (Verb ID=715h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=715h	Data [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Data' in Set command for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:4	GPIO[7:4] Output Data. Not supported in the ALC268.
3:0	GPIO[3:0] Output Data. The value written determines the value driven on a pin that is configured as an output pin.

Codec Response for All NID

Bit	Description
31:0	0's.

8.31. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Table 63. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F16h	0's

Codec Response Format

Response [31:0]
EnableMask [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:4	Reserved.
3:0	GPIO[3:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. It's behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.32. Verb – Set GPIO Enable Mask (Verb ID=716h)

Table 64. Verb – Set GPIO Enable Mask (Verb ID=716h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=716h	Enable Mask [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:4	GPIO[7:4] Enable Mask. Not supported in the ALC268.
3:0	GPIO[3:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.33. Verb – Get GPIO Direction (Verb ID=F17h)

Table 65. Verb – Get GPIO Direction (Verb ID=F17h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F17h	0's

Codec Response Format

Response [31:0]
Direction [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:4	GPIO[7:4] Direction Control. Not supported in the ALC268.
3:0	GPIO[3:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.34. Verb – Set GPIO Direction (Verb ID=717h)

Table 66. Verb – Set GPIO Direction (Verb ID=717h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=717h	Direction [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:4	GPIO[7:4] Direction Control. Not supported in the ALC268.
3:0	GPIO[3:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.35. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Table 67. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F19h	0's

Codec Response Format

Response [31:0]
UnsolEnable [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:4	GPIO[7:4] Unsolicited Enable Mask. Not supported in the ALC268.
3:0	GPIO[3:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.36. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Table 68. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=719h	UnsolEnable [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:4	GPIO[7:4] Unsolicited Enable Mask. Not supported in the ALC268
3:0	GPIO[3:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.

Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb-'Unsolicited Response' for NID=01h are enabled.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.37. Verb – Function Reset (Verb ID=7FFh)

Table 69. Verb – Function Reset (Verb ID=7FFh)

Command Format (NID=01H)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=7FFh	0's

Codec Response Format

Response [31:0]
0's

Codec Response

Bit	Description
31:0	Reserved. Read as 0's.

Note: The Function Reset command causes all widgets in the ALC268 to return to their power-on default state.

8.38. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID=F0Dh, F0Eh)

Table 70. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID=F0Dh, F0Eh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F0Dh/F0Eh	0's

Codec Response Format

Response [31:0]
Bit[31:16]=0's, Bit[15:0] are SIC bit

NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Dh (Control 1 for SIC bit[15:0]).
NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Eh (Control 2 for SIC bit[15:0])

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
31:16	Read as 0's.
15	Reserved. Read as 0's.
14:8	CC[6:0] (Category Code).
7	LEVEL (Generation Level).
6	PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright). 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame).
1	V for Validity Control (control V bit and data in Sub-Frame).
0	DigEn. Digital Enable. 0: OFF 1: ON

Codec Response for Other NID

Bit	Description
31:0	0's.

8.39. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Table 71. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Set Command Format (Verb ID=70Dh, Set Control 1)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=70Dh	SIC [7:0]

Codec Response Format

Response [31:0]
0's

Set Command Format (Verb ID=70Eh, Set Control 2)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=70Eh	SIC [15:8]

Codec Response Format

Response [31:0]
0's

'Payload' in Set Control 1 for NID=06h (S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	LEVEL (Generation Level).
6	PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright). 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame).
1	V for Validity Control (control V bit and data in Sub-Frame).
0	DigEn. Digital Enable. 0: OFF 1: ON

'Payload' in Set Control 2 for NID=06h (S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	Reserved. Read as 0's.
6:0	CC[6:0] (Category Code).

8.40. Get/Set Volume Knob Widget (Verb ID=F0Fh/70Fh)

Table 72. Get/Set Volume Knob Widget (Verb ID=F0Fh/70Fh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F0Fh	0's

Codec Response Format

Response [31:0]
Bit[31:8]=0's, Bit[7:0] is volume

Codec Response for Volume Knob Widget

Bit	Description
31:8	Reserved.
7	Direct. 0: The volume generated by an external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by an external HW volume control will directly affect amplifier volume
6:0	Volume in Steps.

Note: The ALC268 does not support volume knob widget will ignore this verb and respond with 0's.

Set Command Format (Verb ID=70Fh)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=70Fh	Bit[7] is 'Direct' control

Codec Response Format

Response [31:0]
0's

'Payload' in Set Command for Volume Knob Widget

Bit	Description
31:8	Reserved.
7	Direct. 0: The volume generated by an external HW volume control will be sent by unsolicited response. Software is responsible for programming the amplifier appropriately 1: The volume generated by an external HW volume control will directly affect amplifier volume
6:0	Reserved.

Note: The ALC268 does not support volume knob widget will ignore this verb and respond with 0's.

8.41. Get/Set Subsystem ID [31:0] (Verb ID=F20h / 723h~720h to Set Bit[31:0])

Table 73. Get/Set Subsystem ID [31:0] (Verb ID=F20h / 723h~720h to Set Bit[31:0])

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F20h	0's

Codec Response Format

Response [31:0]
32 bits response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:16	Subsystem ID[23:8] (Default=10Ech).
15:8	Subsystem ID[7:0] (Default=02h).
7:0	Assembly ID[7:0] (Default=68h).

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 74. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital Power for Core	DVDD	3.0	3.3	3.6	V
Digital Power for Link	DVDD-IO	1.5	3.3	3.6	V
Analog Power	AVDD1, AVDD2	3.0	3.3	5.5	V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts	-	-	+125	°C
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				
All Pin	4000V				

Note: DVDD-IO must be lower than DVDD.

If customers have lower AVDD(=3.0V) request, please contact Realtek sales representatives or agents.

9.1.2. Threshold Voltage

DVDD-IO=3.3V±5%, $T_{ambient}$=25°C, with 50pF external load.

Table 75. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V_{in}	-0.30	-	DVDD+0.30	V
Low Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI)	V_{IL}	-	-	0.30*DVDDIO	V
High Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI)	V_{IH}	0.65*DVDDIO	-	-	V
Low Level Input Voltage (S/PDIF-OUT, GPIOs)	V_{IL}	-	-	0.44*DVDD	V
High Level Input Voltage (S/PDIF-OUT, GPIOs)	V_{IH}	0.56*DVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9*DVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1*DVDD	V
Input Leakage Current	-	-10	-	10	µA
Output Leakage Current (Hi-Z)	-	-10	-	10	µA
Output Buffer Drive Current	-	-	5	-	mA
Internal Pull Up Resistance	-	-	50k	-	Ω

9.1.3. Digital Filter Characteristics

Table 76. Digital Filter Characteristics

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	0.454*Fs (-1dB)	kHz
	Stopband	28.8	-	-	kHz
	Stopband Rejection	-	-76.0	-	dB
	Passband Ripple	-	±0.05	-	dB
DAC Lowpass Filter	Passband	0	-	0.454*Fs (-1dB)	kHz
	Stopband	28.8	-	-	kHz
	Stopband Rejection	-	-78.5	-	dB
	Passband Ripple	-	±0.05	-	dB

9.1.4. S/PDIF Output Characteristics

DVDD=3.3V, $T_{ambient}$=25°C, with 75Ω external load.

Table 77. S/PDIF Input/Output Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT High Level Output	V_{OH}	3.0	3.3	-	V
S/PDIF-OUT Low Level Output	V_{OL}	-	0	0.3	V

9.2. AC Characteristics

9.2.1. Link Reset and Initialization Timing

Table 78. Link Reset and Initialization Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# Active Low Pulse Width	T_{RST}	1.0	-	-	µs
RESET# Inactive to BCLK Startup Delay for PLL Ready Time	T_{PLL}	20	-	-	µs
SDI Initialization Request	T_{FRAME}	-	-	1	Frame Time

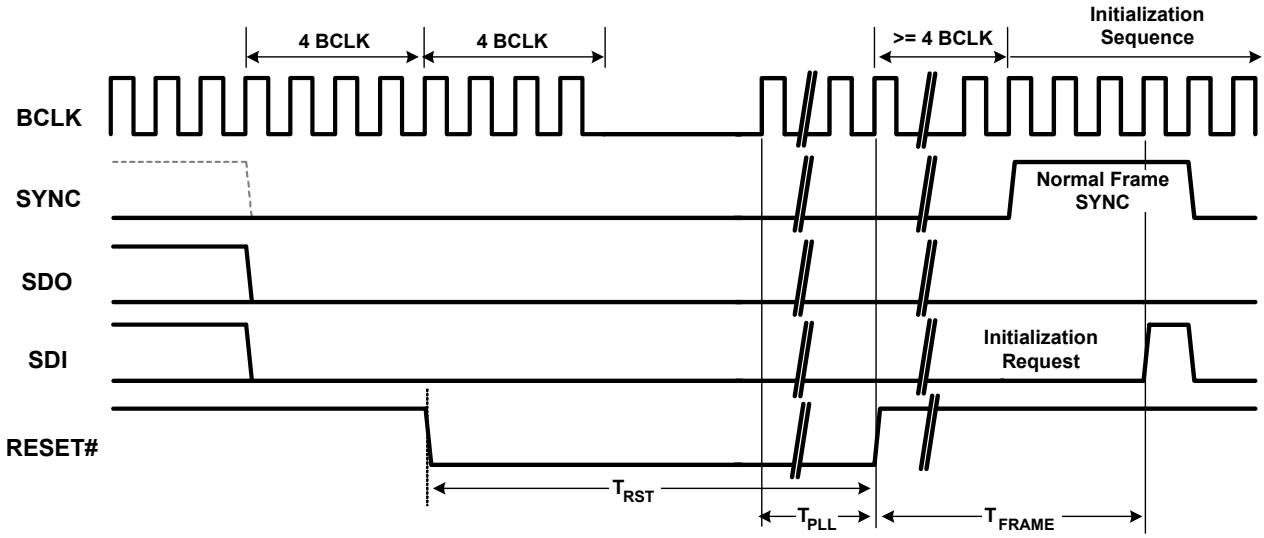


Figure 16. Link Reset and Initialization Timing

9.2.2. Link Timing Parameters at the Codec

Table 79. Link Timing Parameters at the Codec

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK Frequency	-	-	24.0	-	MHz
BCLK Period	T_{cycle}	-	41.67	-	ns
BCLK Jitter	T_{jitter}	-	-	2.0	ns
BCLK High Pulse Width	T_{high}	18.75 (45%)	-	22.91 (55%)	ns (%)
BCLK Low Pulse Width	T_{low}	18.75 (45%)	-	22.91 (55%)	ns (%)
SDO Setup Time at Both Rising and Falling Edge of BCLK	T_{setup}	2.1	-	-	ns
SDO Hold Time at Both Rising and Falling Edge of BCLK	T_{hold}	2.1	-	-	ns
SDI Valid Time After Rising Edge of BCLK (1:50pF External Load)	T_{tco}	-	7.5	8.0	ns
SDI Flight Time	T_{flight}	-	2.0	-	ns

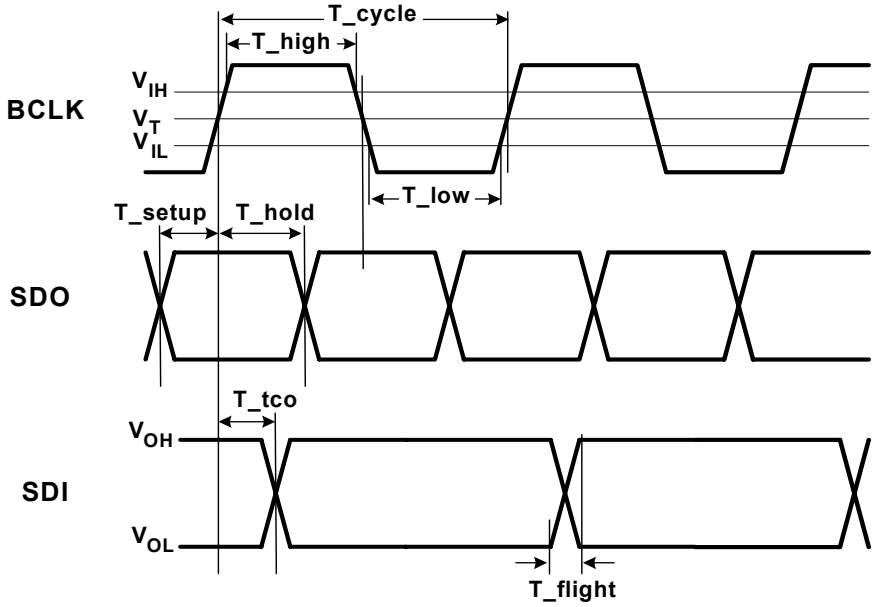


Figure 17. Link Signals Timing

9.2.3. S/PDIF Output Timing

Table 80. S/PDIF Output Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT Frequency*1	-	-	3.072	-	MHz
S/PDIF-OUT Period*1	T_{cycle}	-	325.6	-	ns
S/PDIF-OUT Jitter	T_{jitter}	-	-	4	ns
S/PDIF-OUT High Level Width*1	T_{High}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Low Level Width*1	T_{Low}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Rising Time	T_{rise}	-	2.0	-	ns
S/PDIF-OUT Falling Time	T_{fall}	-	2.0	-	ns

**1: Bit parameters for 48kHz sample rate of S/PDIF-OUT.*

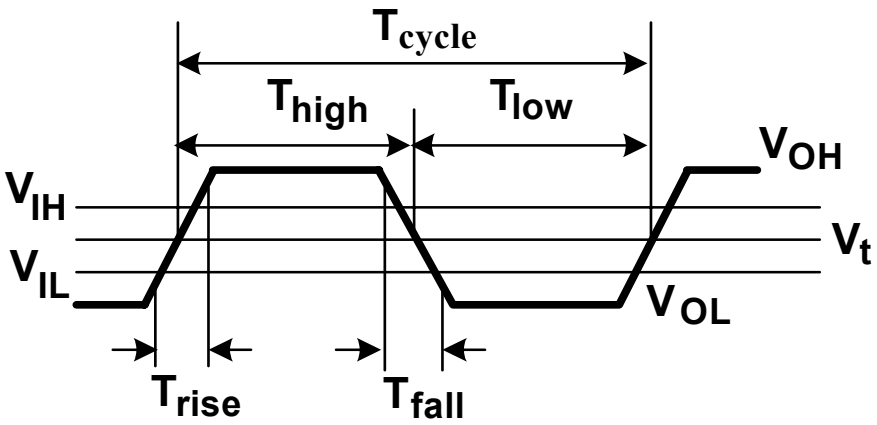


Figure 18. Output Timing

9.2.4. Test Mode

The ALC268 does not support codec test mode or Automatic Test Equipment (ATE) mode.

9.3. Analog Performance

Standard Test Conditions

- $T_{ambient}$=25 °C, DVDD-CORE=3.3V ±5%, AVDD=5.0V±5%
- 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
- 10KΩ/50pF load; Test bench Characterization BW:10Hz~22kHz

Table 81. Analog Performance

Parameter	Min	Typ	Max	Units
Full-Scale Input Voltage				
All ADC (Gain=0dB)	-	1.1	-	Vrms
Full-Scale Output Voltage				
All DAC (Gain=0dB)	-	1.4	-	Vrms
Dynamic Range with 1kHz Tone, DR (A Weighted)				
ADC	-	90	-	dB FSA*
DAC	-	95	-	dB FSA
Total Harmonic Distortion Plus Noise, THD+N				
ADC	-	-85	-	dB FS*
DAC	-	-92	-	dB FS
Headphone Out @32Ω Load	-	-80	-	dB FS
Frequency Response				
ADC (-3dB Lower Edge, -1dB Higher Edge)	10	-	0.454*Fs	Hz
DAC (-3dB Lower Edge, -1dB Higher Edge)	10	-	0.454*Fs	Hz
Power Supply Rejection Ratio	-	-40	-	dB
Total Out-of-Band Noise (28.8kHz~100kHz)	-	-60	-	dB
Amplifier Gain Step				
ADC	-	1.5	-	dB
DAC	-	1.0	-	dB
Crosstalk Between Input Channels	-	-80	-	dB
Input Impedance (Gain=0dB)	-	47	-	KΩ
Output Impedance				
Amplified Output	-	1	-	Ω
Non-Amplified Output	-	200	-	Ω
Digital Power Supply Current (Normal Operation) DVDD=3.3V, DVDD-IO=3.3V	-	25	-	mA
Digital Power Supply Current (Power Down Mode) DVDD=3.3V, DVDD-IO=3.3V	-	-	400	μA
Analog Power Supply Current (Normal Operation)				
AVDD1, AVDD2=5.0V	-	35	-	mA
AVDD1, AVDD2=3.3V	-	19	-	mA
Analog Power Supply Current (Power Down Mode)				
AVDD1, AVDD2=5.0V	-	-	700	μA
VREFOUTx Output Voltage	0	2.50	4.20	V
VREFOUTx Output Current	-	5	-	mA

Note: FSA=Full-Scale with A-weighting filter. FS=Full-Scale.

10. Application Notes

10.1. Application Circuits

Please contact Realtek for the latest application circuits. To get the best compatibility in hardware design and software driver, any modification should be confirmed by Realtek. Realtek may upload the latest application circuits onto our web site (www.realtek.com.tw) without modifying this datasheet.

10.2. Filter Connection

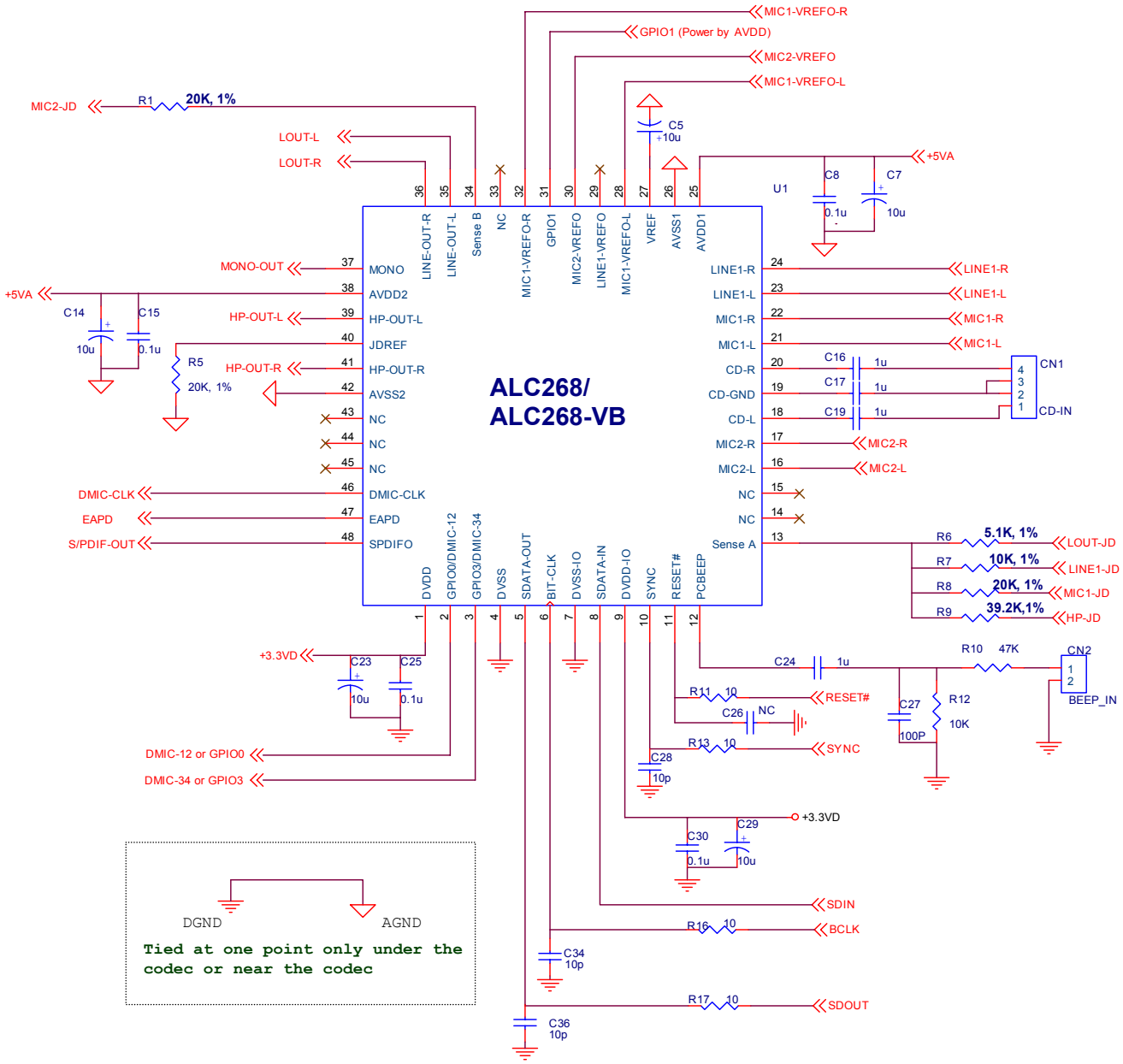
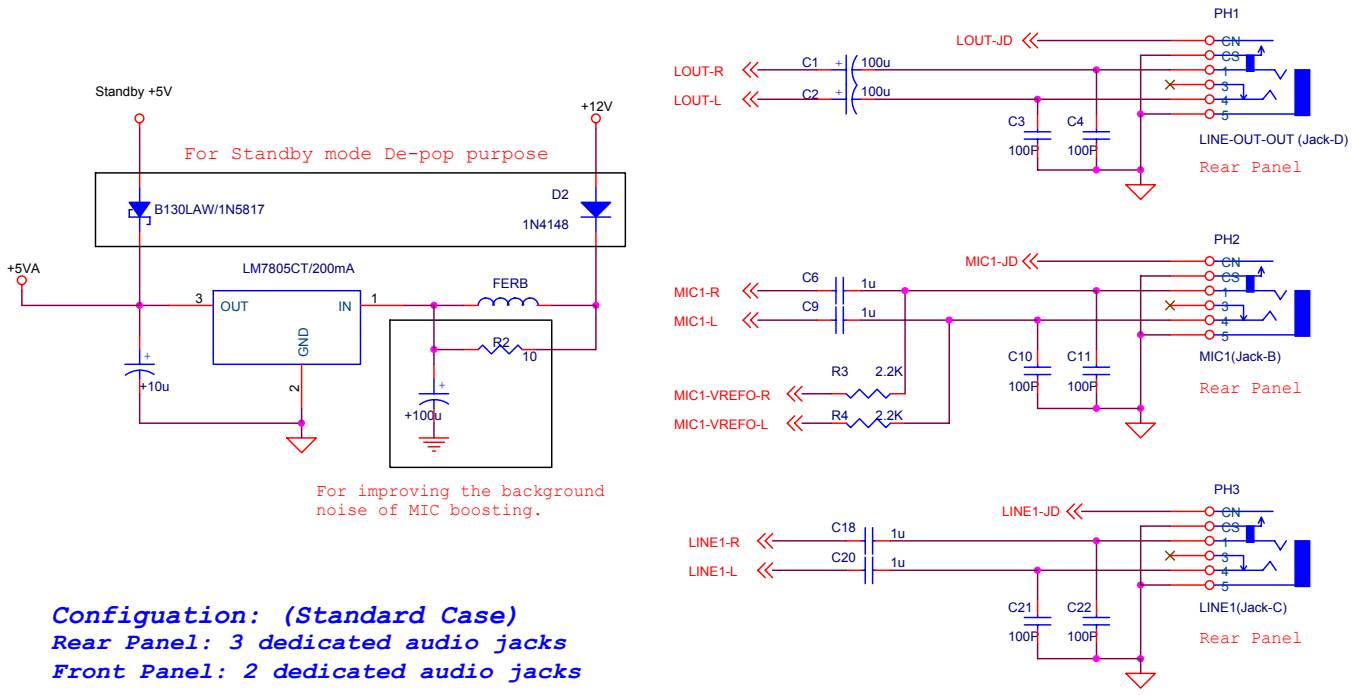


Figure 19. Filter Connection

10.3. Power and Rear Panel Jack Connection



Configuation: (Standard Case)
Rear Panel: 3 dedicated audio jacks
Front Panel: 2 dedicated audio jacks

Pin/Port Assignment	Location	Functions
FRONT(pin-35,36)/Port-D	Rear Panel	LINE-OUT w/ amplfier
MIC1 (pin-21,22)/Port-B	Rear Panel	Mic-In
LINE1 (pin-23,24)/Port-C	Rear Panel	Line-In
HP-OUT (pin-39,41)/Port-A	Front Panel	HP-OOUT w/ amplifier
MIC2 (pin-16,17)/Port-F	Front Panel	Mic-In

Figure 20. Power and Rear Panel Jack Connection

10.4. Front Panel Header and Front Panel I/O Cable

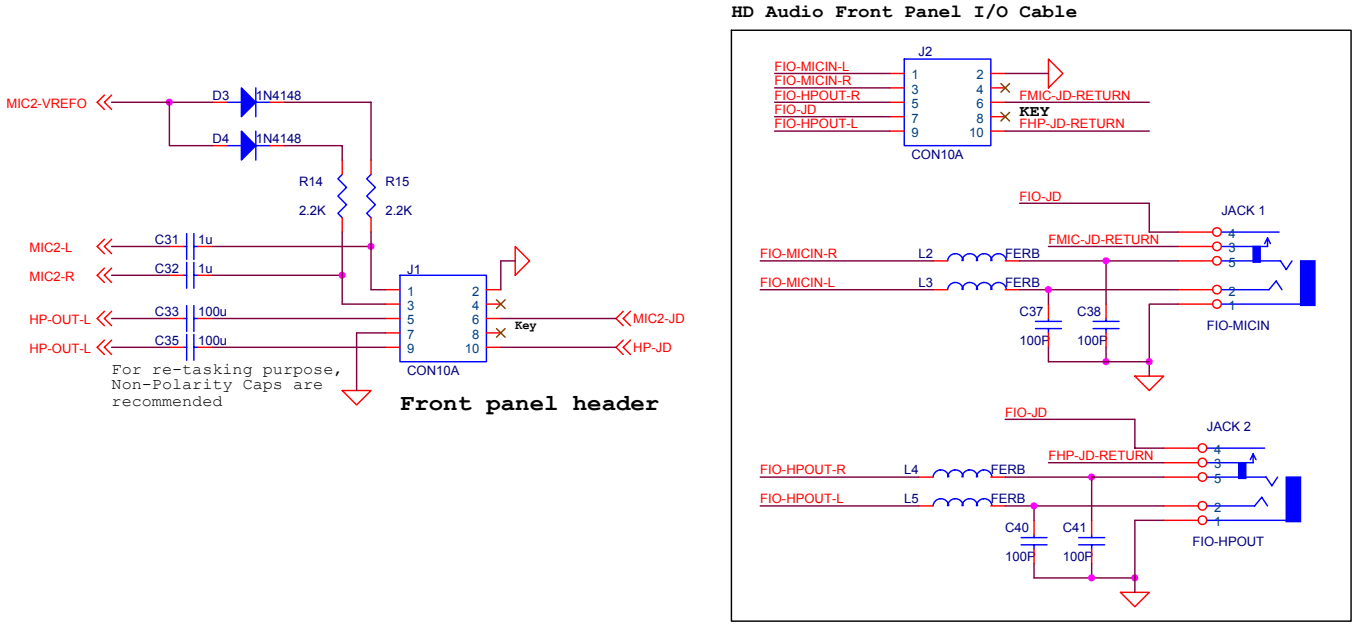
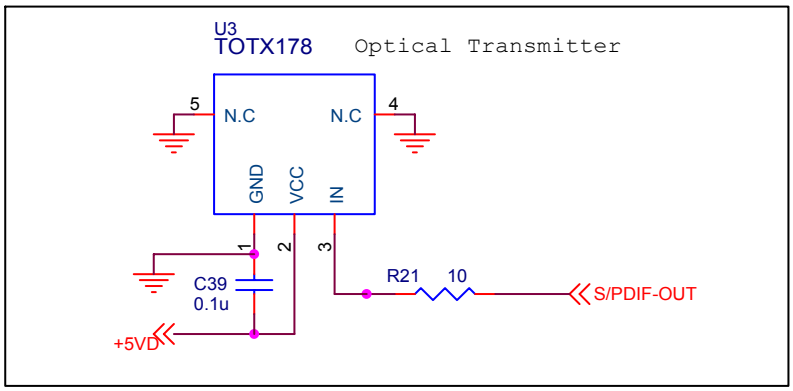


Figure 21. Front Panel Header and Front Panel I/O Cable

As the ALC268 series does not support LINE2 (port-E) or HP-OUT (port-A), these pins may be connected to the front panel header as the headphone output. To accommodate the ALC268 series and ALC262 series on the same front panel I/O cable, the connection of the front panel header in Figure 21 is modified. Please contact Realtek to confirm your design can accommodate all ALC series HD Audio Codecs.

S/PDIF module option 1: Optical



S/PDIF module option 2: Coaxial

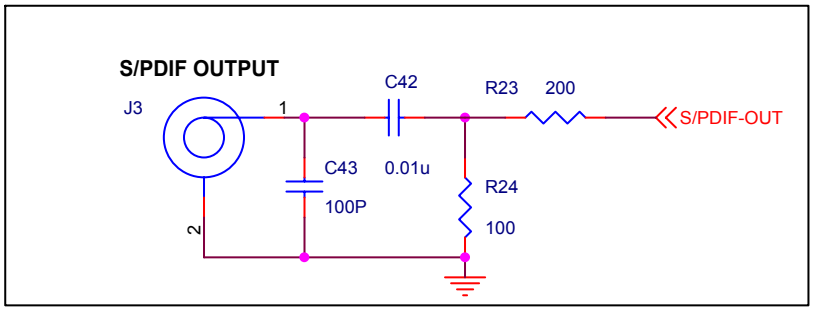


Figure 22. S/PDIF-OUT Connection

10.5. Digital Microphone Implementation

This section describes the ALC268 series digital microphone implementation. There is one Clock output pin and 1 Data input pin in the ALC268 series. The ALC268 series provide the clock signal to the digital microphone. When the digital microphone receives the external sound input, it converts the analog signals to digital in a 1-bit format. The 1-bit data is delivered to the codec though the data input pin. The Digital Filter in the audio codec converts the 1-bit data stream into Pulse Code Modulation (PCM) data. The PCM data is sent to the HDA controller through the HDA link.

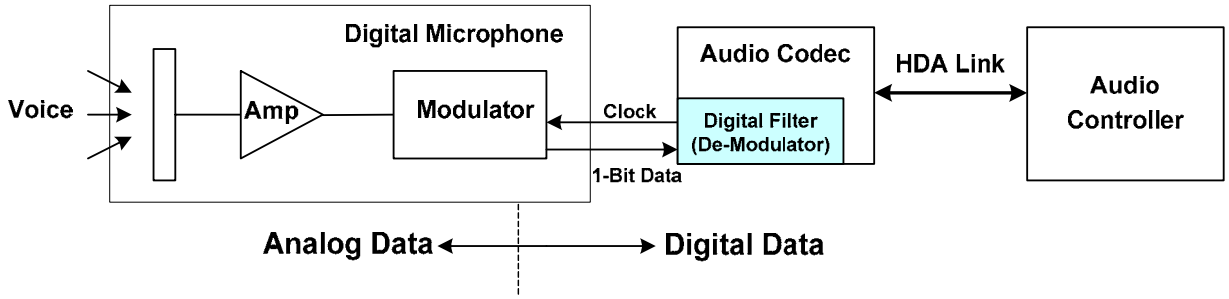


Figure 23. Digital Microphone Implementation-1

The ALC268Q supports a two-wire interface (DMIC-CLK and DMIC-DATA) for the digital microphone and operates in single-channel (mono type) or stereo-channels (stereo) digital microphone mode. One pin is clock output to the digital microphone, and the other two are serial pins. The default clock output is 2.048MHz.

The ALC268 and ALC268-VB1 support a 3-wire interface. DMIC-CLK is clock output to a digital microphone, DMIC-12 and DMIC-34 are data inputs from a digital microphone. With the extra data pin DMIC-34, the ALC268 and ALC268-VB1 can support up to 4 channels of digital microphone input.

In Type 1 (Figure 24), the ALC268 uses one data pin to support mono input from digital microphones with an LMV1024 (L), SPD0205ND (L), or AKU2000 (L).

In Type 2 (Figure 24), the ALC268 uses one data pin to support stereo inputs from digital microphones with an LMV1024/1026 (L/R), SPD0205ND (L & R), or AKU2000 (L & R).

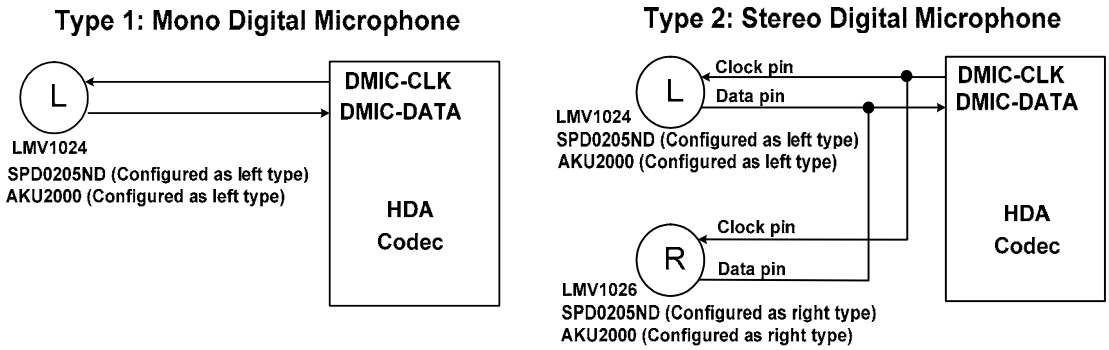
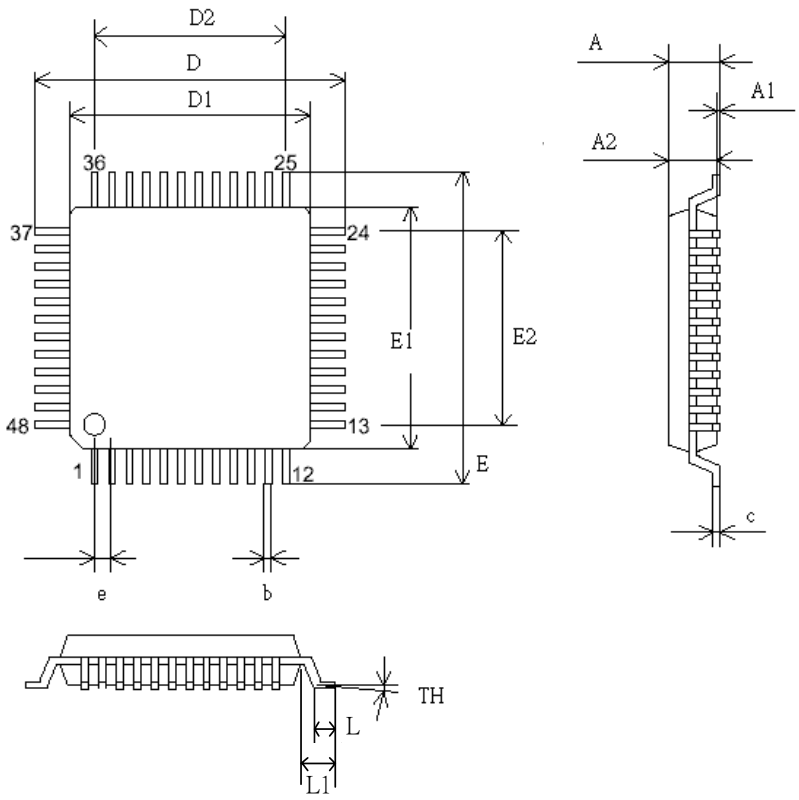


Figure 24. Digital Microphone Implementation-2

11. Mechanical Dimensions

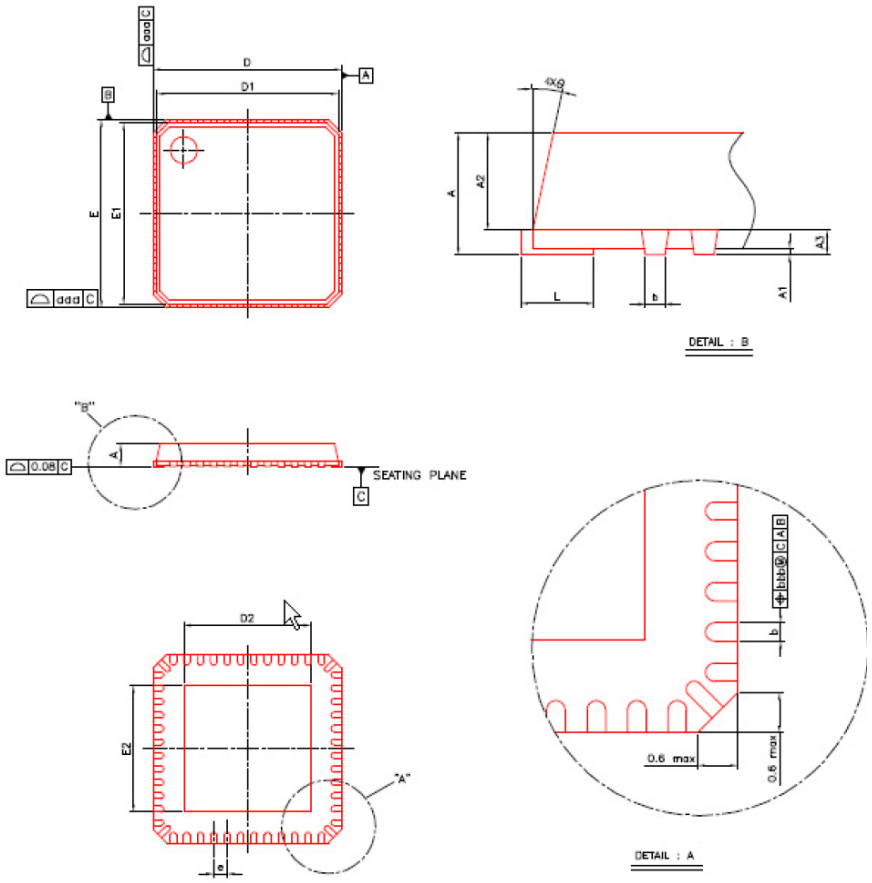
11.1. LQFP-48 Mechanical Dimensions (ALC268/ALC268-VB)



SYMBOL	MILLIMETER			INCH		
	MIN.	TYP	MAX.	MIN.	TYP	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09	-	0.20	0.004	-	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1	-	1.00	-	-	0.0393	-

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm			
LEADFRAME MATERIAL			
APPROVE		DOC. NO.	
		VERSION	02
CHECK		DWG NO.	PKGC-065
		DATE	
REALTEK SEMICONDUCTOR CORP.			

11.2. QFN-48 Mechanical Dimensions (ALC268Q)



SYMBOL	MILLIMETER			INCH		
	MIN.	TYP	MAX.	MIN.	TYP	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	-	0.65	1.00	-	0.026	0.039
A3	-	0.20	0	-	0.008	-
b	0.18	0.23	0.30	0.007	0.009	0.012
D	7.00BSC			0.276BSC		
D1	6.75BSC			0.266BSC		
D2	2.25	4.70	5.25	0.089	0.185	0.207
E	7.00BSC			0.276 BSC		
E1	6.75BSC			0.266 BSC		
E2	2.25	4.70	5.25	0.089	0.185	0.207
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
TH	0°	-	12°	0°	-	12°
aaa	-	-	0.25	-	-	0.010
bbb	-	-	0.10	-	-	0.004
chamfer	-	-	0.60	-	-	0.024

TITLE: QFN-48 (7.0x7.0x1.0mm) PACKAGE OUTLINE DRAWING			
LEADFRAME MATERIAL			
APPROVE		DOC. NO.	
		VERSION	
CHECK		DWG NO.	
		DATE	
REALTEK SEMICONDUCTOR CORP.			

12. Ordering Information

Table 82. Ordering Information

Part Number	Package	Status
ALC268-GR	LQFP-48 & 'Green' Package (ALC268 Version A)	Mass Production
ALC268Q-GR	QFN-48 & 'Green' Package (ALC268 Version A)	Mass Production
ALC268-VB1-GR	ALC268 Version B1, LQFP-48 with 'Green' Package	Mass Production

Note 1: See page 6 and page 7 for Green package and version identification.

Note 2: Above parts are tested under AVDD =5.0V. If customers have lower AVDD request, please contact Realtek sales representatives or agents.

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