2.4W Stereo Audio Power Amplifier & Capfree Headphone Driver

Features

- **Operating Voltage**
  - **– HV_{DD}= 3.0~3.6V**
  - **– V_{DD}= 4.5~5.5V**
- **No Output Capacitor at Headphone Amplifier Required**
- **Meeting VISTA Requirement**
- **Low Distortion**

  AMP mode
  - **– THD+N=56dB, at V_{DD} = 5V, R_L = 4Ω, P_O=1.5W**
  - **– THD+N=64dB, at V_{DD} = 5V, R_L = 8Ω, P_O=0.9W**

  HP mode
  - **– THD+N=73dB, at HV_{DD}=3.3V, R_L=16Ω P_O=125mW**
  - **– THD+N=77dB, at HV_{DD}=3.3V, R_L=32Ω, P_O=88mW**
  - **– THD+N=85dB, at HV_{DD}=3.3V, R_L=10kΩ, V_O=1.7Vrms**
- **Output Power at 1% THD+N**
  - **– 1.9W, at V_{DD} = 5V, AMP mode, R_L = 4Ω**
  - **– 1.2W, at V_{DD} = 5V, AMP mode, R_L = 8Ω**
- **at 10% THD+N**
  - **–2.4W at V_{DD} = 5V, AMP mode, R_L = 4Ω**
  - **–1.5W at V_{DD} = 5V, AMP mode, R_L = 8Ω**
- **Depop Circuitry Integrated**
- **Thermal Shutdown Protection and Over Current Protection Circuitry**
- **High Supply Voltage Ripple Rejection**
- **Surface-Mount Packaging**
  - **– TSSOP-28P (with enhanced thermal pad)**
  - **– TQFN5x5-28 (with enhanced thermal pad)**
- **Lead Free Available (RoHS Compliant)**

General Description

The APA2056A is a monolithic integrated circuit, which combines a stereo power amplifier and a stereo output capacitor-less headphone amplifier. The headphone amplifier is ground-reference output, and no need the output capacitors for DC blocking. The advantages of eliminating the output capacitor are saving the cost, PCB's space and component height.

Both the de-pop circuitry and the thermal shutdown protection circuitry are integrated in the APA2056A, which reduces pops and clicks noise during power on/off and in shutdown mode. Thermal shutdown protects the chip from being destroyed by over-temperature failure. To simplify the audio system design in notebook computer applications, the APA2056A provides the internal fixed gain (10.5dB), and these features can minimize components and PCB area.

The APA2056A is available in a TSSOP-28P and TQFN5x5-28 package. Both packages are characterized by space saving and thermal efficiency.

Applications

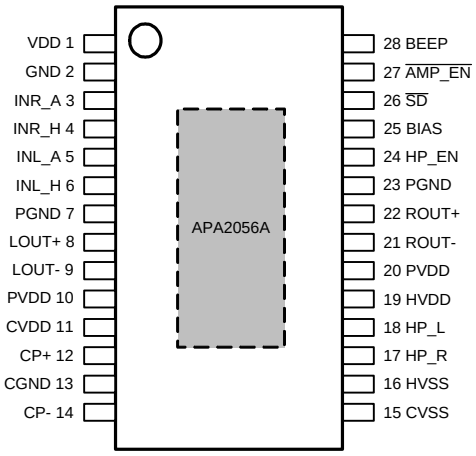
- **Note book PCs**
- **LCD monitor**

Ordering and Marking Information

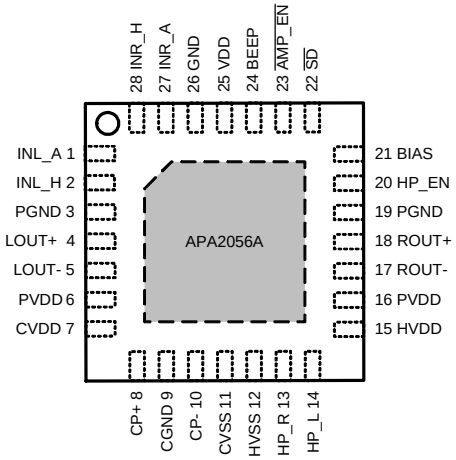
APA2056A □□□-□□ □ Lead Free Code Handling Code Temperature Range Package Code		Package Code R : TSSOP-28P QB : TQFN5x5-28 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device
APA2056A R :	APA2056A XXXXX	XXXXX - Date Code
APA2056A QB :	APA2056A XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Configurations



(TSSOP-28P)
(Top view)



(TQFN5x5-28)
(Top view)

= ThermalPad (connected the ThermalPad to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (PVDD, CVDD, VDD)	-0.3 to 6	V
$HV_{DD,}$	Supply Voltage (HVDD)		
V_{SS}	Supply Voltage (VSS)	+0.3 to -6	V
$V_{\overline{SD}}$, $V_{\overline{AMP\_EN}}$, V_{HP_EN}	Input Voltage	0 to V_{DD}+0.3V	
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	150	°C

Absolute Maximum Ratings (Cont.) (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature	260, 10 seconds	°C
P_D	Power Dissipation	Internally Limited	W

Note 1 : Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient (Note 2) TSSOP-28P TQFN5x5-28	 45 43	°C/W

Note 2 : 3.42 in^2 printed circuit board with 2OZ trace and copper through 10 vias of 15mil diameter vias. The thermal pad on the TSSOP-28P & TQFN-28 packages with solder on the printed circuit board.

Recommended Operating Conditions

		Min.	Max.	Unit
Supply voltage, V_{DD}		4.5	5.5	V
Supply voltage, HV_{DD}		3.0	3.6	V
High level threshold voltage, V_{IH}	$\overline{AMP\_EN}$, HP_EN, $\overline{SD}$	2		V
Low level threshold voltage, V_{IL}	$\overline{AMP\_EN}$, HP_EN, $\overline{SD}$		0.8	V
Common mode input voltage, Vicm	for Amplifier		V_{DD}-1	V
	for Headphone Amplifier		HV_{DD}-1	V

Electrical Characteristics

V_{DD} = 5V, HV_{DD} = 3.3V, GND = PGND = CPGND = 0V, T_A = 25°C (unless otherwise noted).

Symbol	Parameter	Test Condition	APA2056A			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage		4.5		5.5	V
HV_{DD}	Headphone Amplifier supply voltage		3.0		3.6	V
I_{VDD}	V_{DD} Supply Current	Only Speaker mode, $\overline{AMP\_EN}$ = HP_EN = 0V		17.5	29	mA
I_{HVDD}	H_{VDD} Supply Current			0.15	1	
I_{VDD}	V_{DD} Supply Current	Only Headphone mode, HP_EN = $\overline{AMP\_EN}$ = 5V		12	20	
I_{HVDD}	H_{VDD} Supply Current			3	5	
I_{VDD}	V_{DD} Supply Current	All Enable, HP_EN=5V and $\overline{AMP\_EN}$ = 0V		20	35	
I_{HVDD}	H_{VDD} Supply Current			3	5	

Electrical Characteristics (Cont.)

V_{DD} = 5V, HV_{DD} = 3.3V, GND = PGND = CPGND = 0V, T_A = 25°C (unless otherwise noted).

Symbol	Parameter	Test Condition	APA2056A			Unit
			Min.	Typ.	Max.	
$I_{SD(HVDD)}$	HV_{DD} Shutdown Current	$\overline{SD}$ = 0V		50	90	µA
$I_{SD(VDD)}$	V_{DD} Shutdown Current			1	10	
$I_{\overline{AMP\_EN}}$	Input current	$\overline{AMP\_EN}$		1		µA
I_{HP_EN}	Input current	HP_EN,		10	15	µA
Speaker mode						
P_O	Output Power	THD+N =1%, F_{in} =1KHz R_L =4Ω R_L =8Ω	 1.0	 1.9 1.2		W
		THD+N =10%, F_{in} =1KHz R_L =4Ω R_L =8Ω	 1.3	 2.4 1.5		
V_{OS}	Output Offset Voltage	R_L =8Ω, Gain =10.5dB			10	mV
THD+N	Total Harmonic Distortion plus Noise	F_{in} =1KHz P_O = 1.5W, R_L =4Ω P_O = 0.9W, R_L =8Ω		 0.15 0.06		%
X'talk	Channel Separation	F_{in} =1KHz, C_B=2.2µF, R_L=8Ω, P_O=0.92W		80		dB
		F_{in} =1KHz, C_B=2.2µF, R_L =4Ω, P_O=1.5W		83		
PSRR	Power Supply Rejection Ratio	C_B =2.2µF, R_L =8Ω, F_{in} =120Hz		70		dB
S/N		P_O =0.8W, R_L =8Ω, A-weighted Filter		90		dB
Vn	Noise Output Voltage	Gain =10.5dB, R_L =8Ω, C_B =2.2µF		80		µV (rms)
Headphone mode						
P_O	Output Power	THD+N = 1%, F_{in} =1KHz R_L = 16Ω R_L = 32Ω	 100	 160 120		mW
		THD+N = 10%, F_{in} =1KHz R_L =16Ω R_L =32Ω	 150	 200 165		
V_O	Output Voltage Swing	R_L =10KΩ, THD+N=10%		2.9		Vrms
		R_L =10KΩ, THD+N=1%		2.4		
V_{OS}	Output Offset Voltage	R_L =32Ω	-10		+10	mV
THD+N	Total Harmonic Distortion plus Noise	F_{in} = 1KHz P_O = 125mW, R_L =16Ω P_O = 88mW, R_L =32Ω V_O=1.7Vrms, R_L=10kΩ		 0.02 0.02 0.005		%
X'talk	Channel Separation	F_{in} =1KHz, R_L =16Ω, P_O =125mW		80		dB
		F_{in} =1KHz, R_L =32Ω, P_O =88mW		85		
		F_{in} =1KHz, R_L=10KΩ, V_O =1.7Vrms		105		
PSRR	Power Supply Rejection Ratio	C_B = 2.2µF, R_L=32Ω, F_{in} =120Hz		80		dB

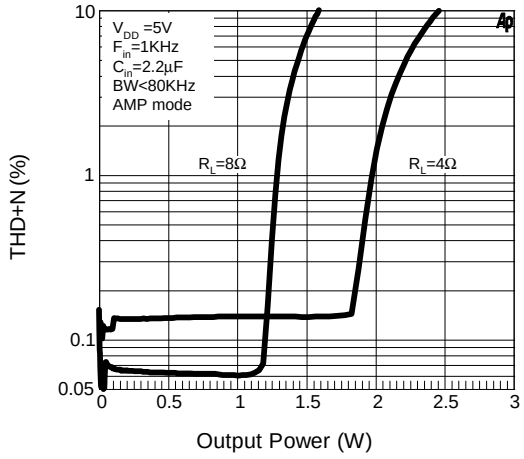
Electrical Characteristics (Cont.)

V_{DD} = 5V, HV_{DD} = 3.3V, GND = PGND = CPGND = 0V, T_A = 25°C (unless otherwise noted).

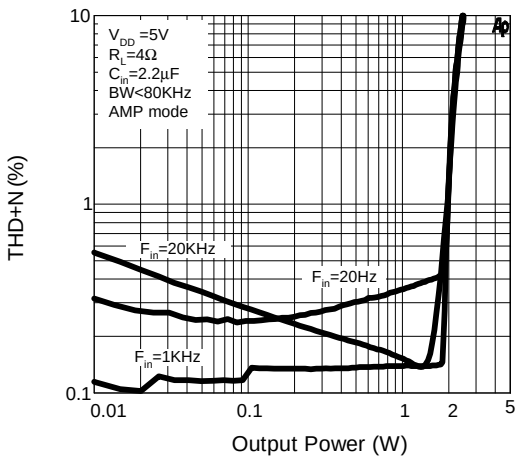
Symbol	Parameter	Test Condition	APA2056A			Unit
			Min.	Typ.	Max.	
Headphone mode (Cont.)						
S/N		With A-weighted Filter P_O = 70mW, R_L =32Ω V_O =1.2Vrms, R_L=10kΩ		 95 92		dB
Vn	Noise Output Voltage	C_B =2.2μF		30		μV (rms)
Rf	Input Feedback Resistance		38	40	42	kΩ
Charge Pump						
F_{OSC}	Switching frequency		460	540	620	KHz
CV_{SS}	Charge Dump Output Voltage (CVSS)	No load		-0.98 V_{DD}		V
Req	Charge pump requirement resistance			9	12	Ω
Beep						
Vbeep	Beep trigger level			3		V_{PP}
T_{RES}	Beep response time			4		ms
Attenuation						
Att(HP_EN)	HP disable attenuation	R_L = 32Ω, V_O = 1.1Vrms, F_{in} = 1KHz		115		dB
		R_L = 10KΩ, V_O = 1.1Vrms, F_{in} = 1KHz		85		dB
Att($\overline{AMP\_EN}$)	AMP disable attenuation	R_L = 8Ω, V_O = 2Vrms, F_{in} = 1KHz		112		dB
		R_L = 4Ω, V_O = 2Vrms, F_{in} = 1KHz		112		dB
Att_SD(HP_EN)	Shutdown active	R_L = 10KΩ on the Headphone Mode, V_O = 1.1Vrms, F_{in} = 1KHz		90		dB
Att_SD($\overline{AMP\_EN}$)	Shutdown active	R_L = 8Ω on the AMP Mode, V_O = 1Vrms, F_{in} = 1KHz		100		dB
Headphone to Speaker Crosstalk						
X'talk	Channel Separation	$\overline{AMP\_EN}$ = 0V, R_L = 8Ω HP_EN = 5V, R_L = 16Ω, F_{in} = 1KHz, P_O = 125mW		85		dB
Speaker to Headphone Crosstalk						
X'talk	Channel Separation	HP_EN = 5V, R_L = 10KΩ $\overline{AMP\_EN}$ = 0V, R_L = 4Ω, F_{in} = 1KHz, P_O = 1.5W		80		dB
Amplifier Start up Time						
$T_{start-up}$	Start up time			120		msec

Typical Operating Characteristics

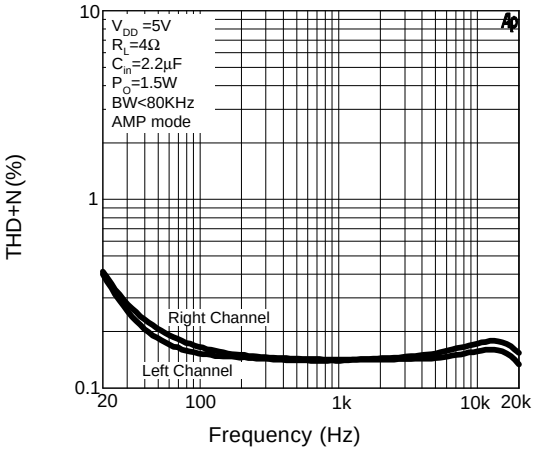
THD+N vs. Output Power



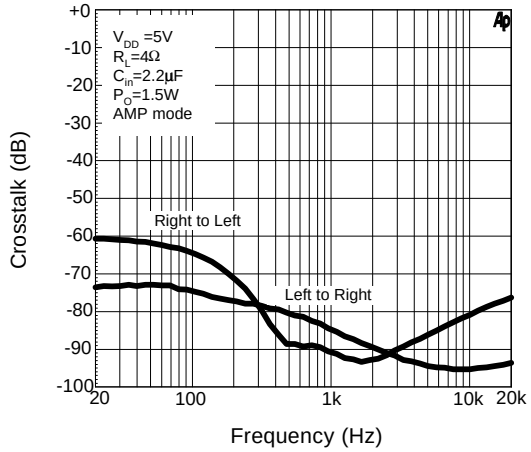
THD+N vs. Output Power



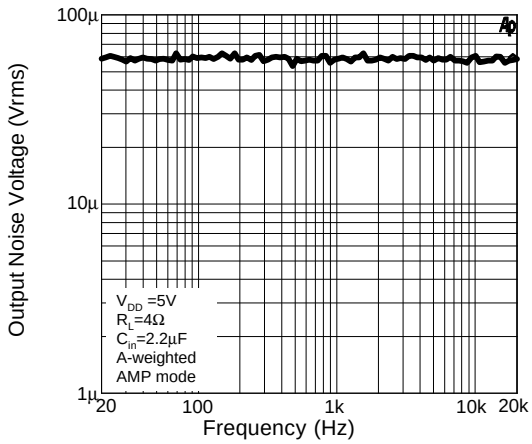
THD+N vs. Frequency



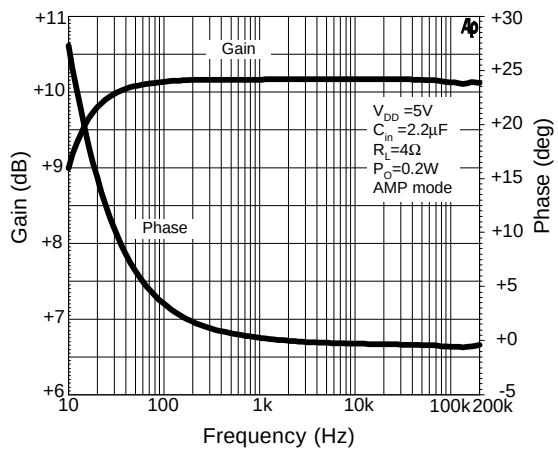
Crosstalk vs. Frequency



Output Noise Voltage vs. Frequency

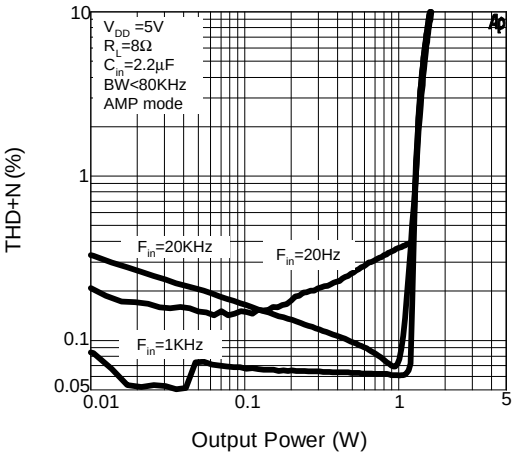


Frequency Response

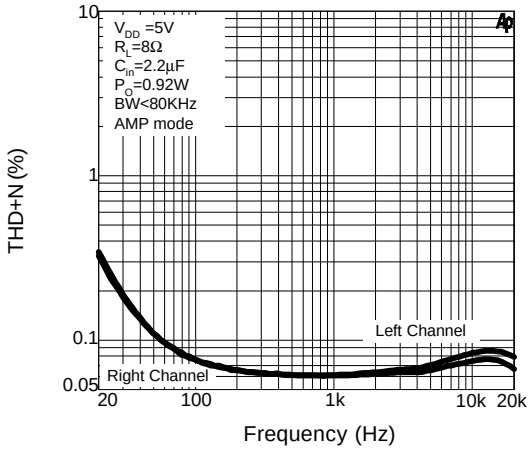


Typical Operating Characteristics (Cont.)

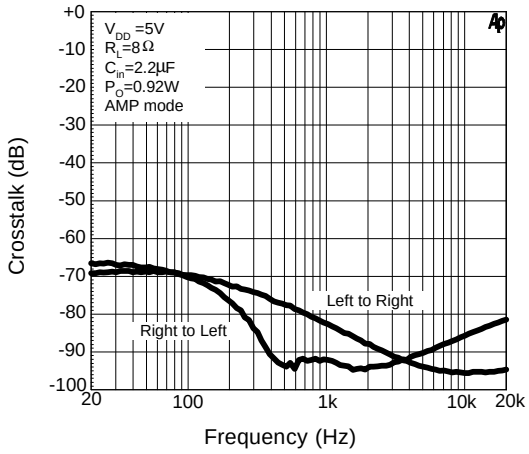
THD+N vs. Output Power



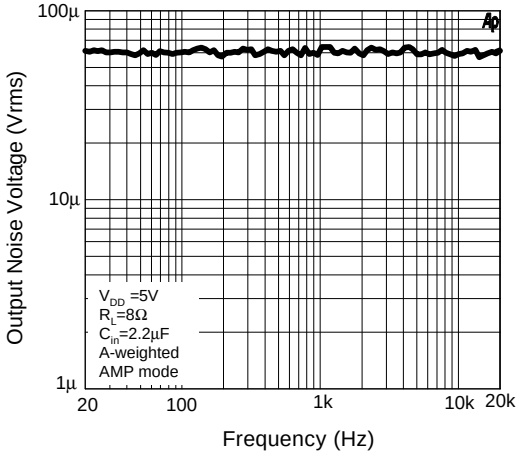
THD+N vs. Frequency



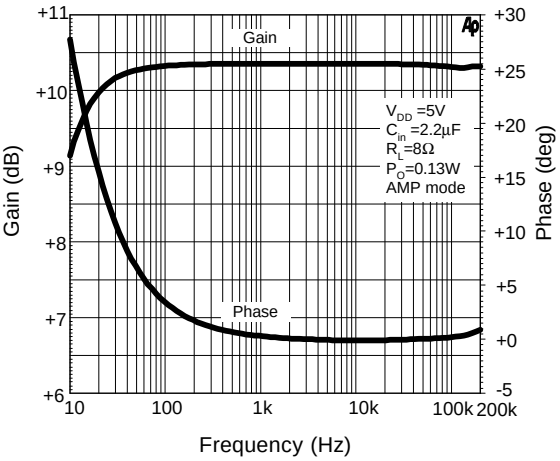
Crosstalk vs. Frequency



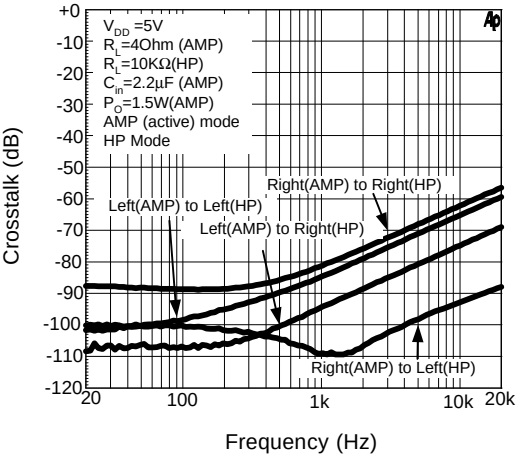
Output Noise Voltage vs. Frequency



Frequency Response

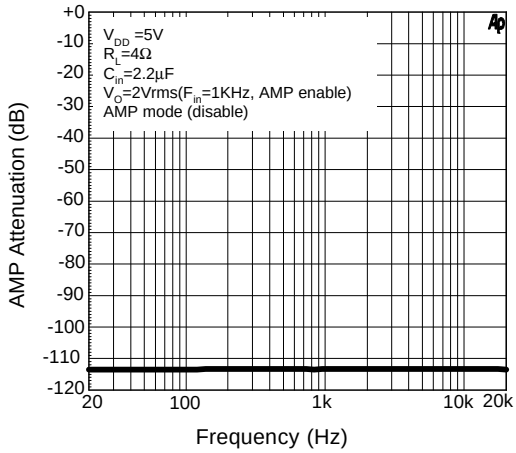


Crosstalk vs. Frequency

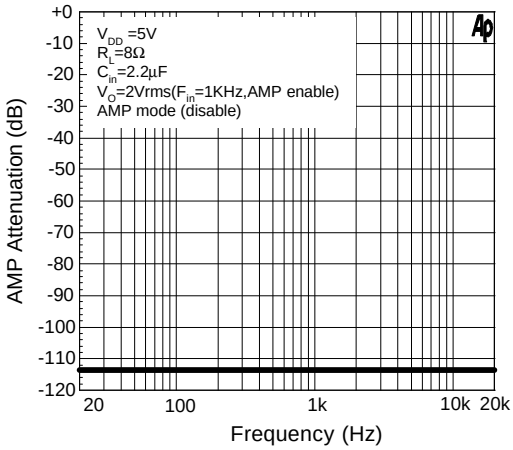


Typical Operating Characteristics (Cont.)

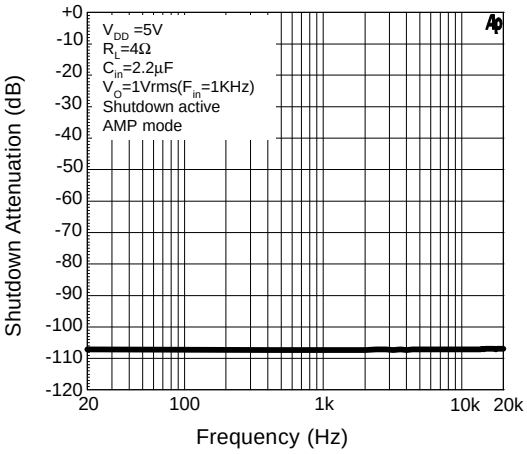
AMP Attenuation vs. Frequency



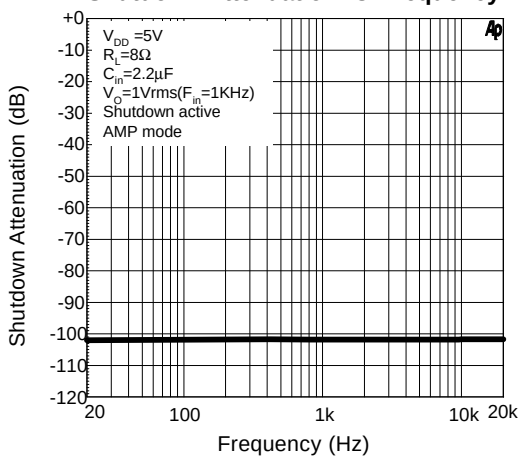
AMP Attenuation vs. Frequency



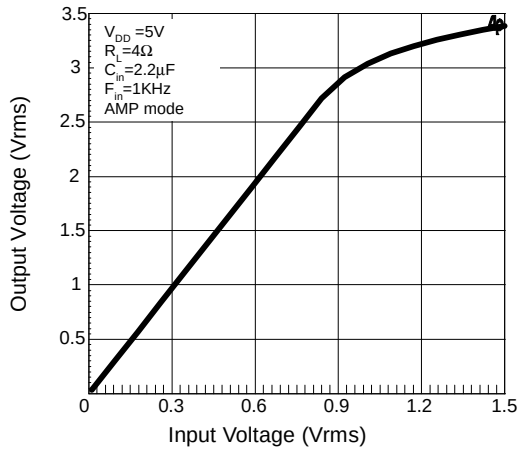
Shutdown Attenuation vs. Frequency



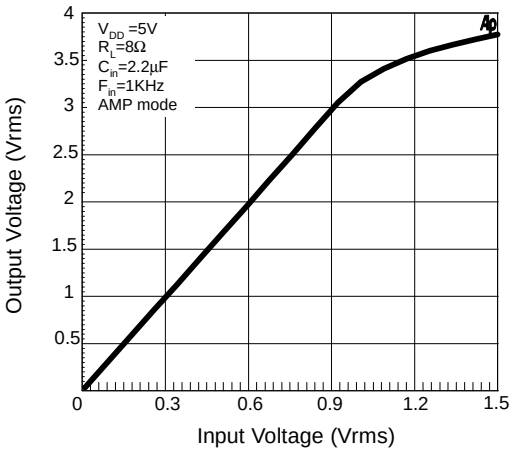
Shutdown Attenuation vs. Frequency



Input Voltage vs. Output Voltage

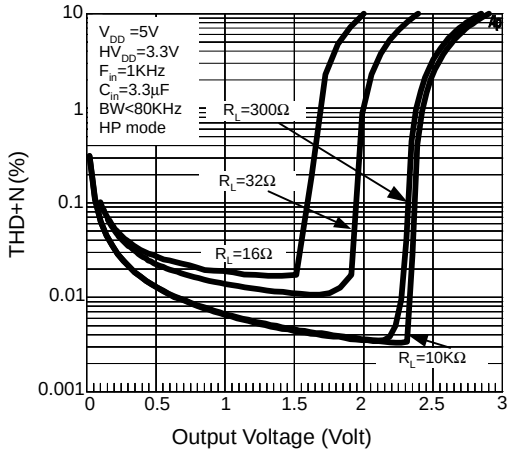


Input Voltage vs. Output Voltage

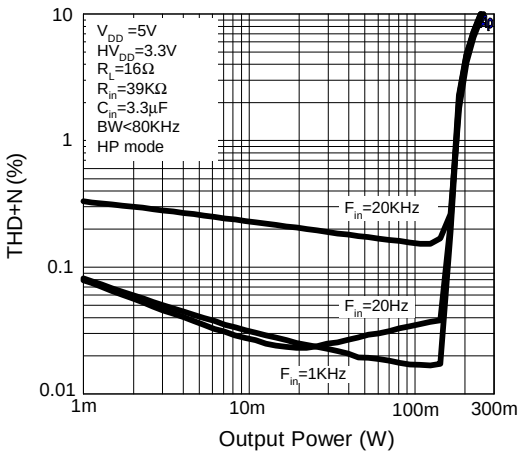


Typical Operating Characteristics (Cont.)

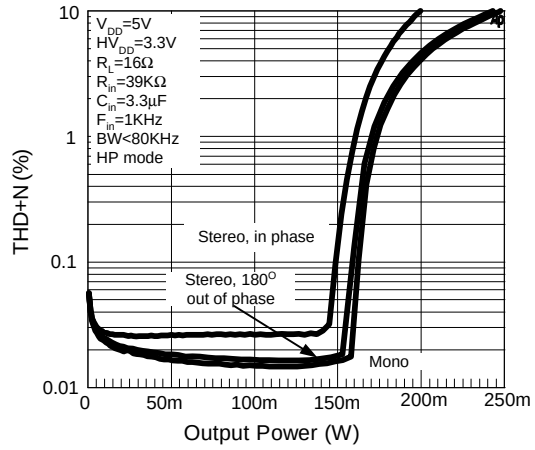
THD+N vs. Output Voltage



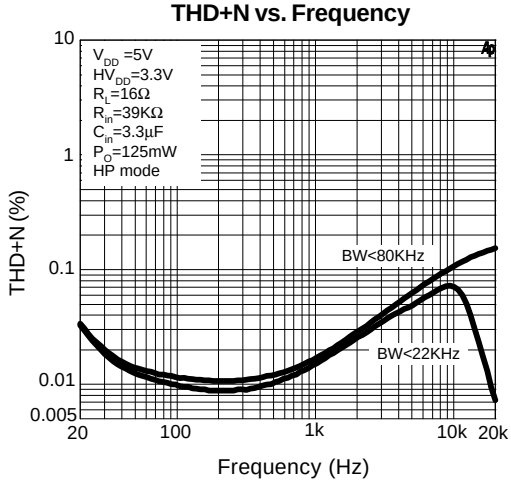
THD+N vs. Output Power



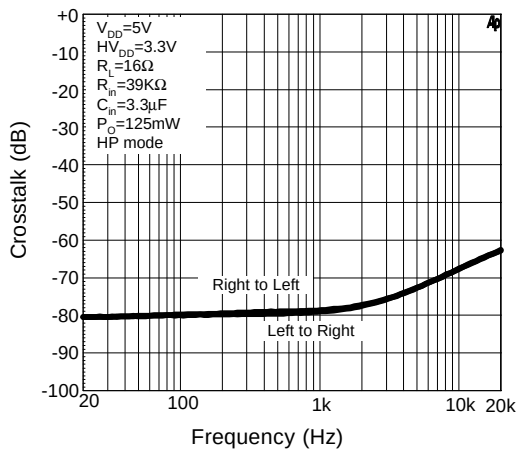
THD+N vs. Output Power



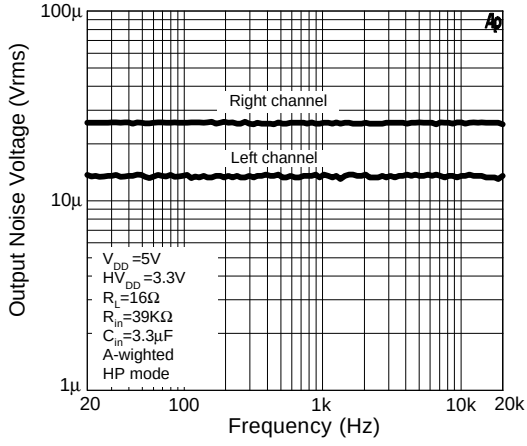
THD+N vs. Frequency



Crosstalk vs. Frequency

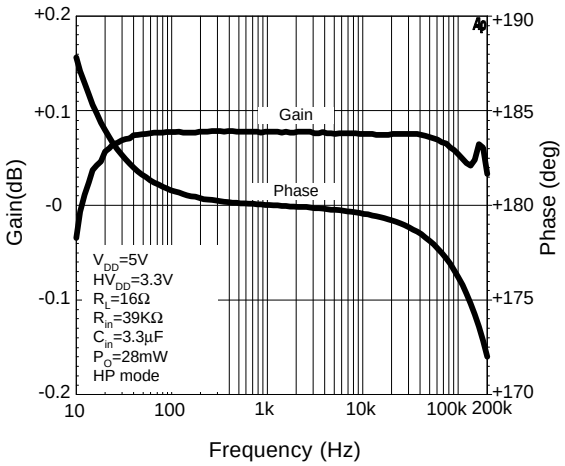


Output Noise Voltage vs. Frequency

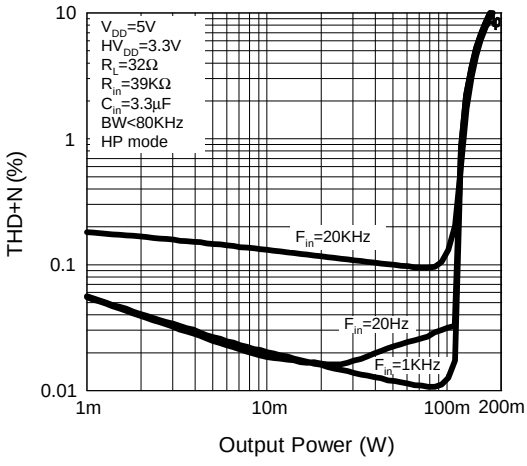


Typical Operating Characteristics (Cont.)

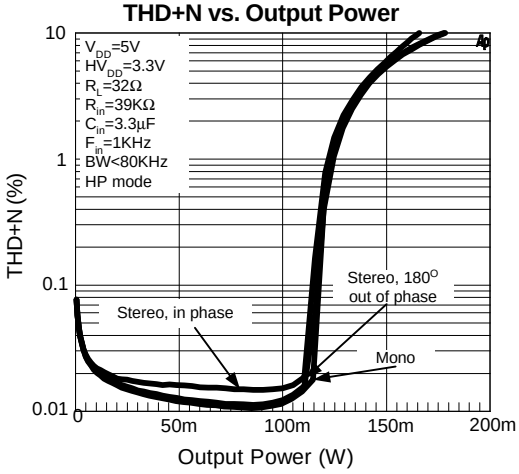
Frequency Response



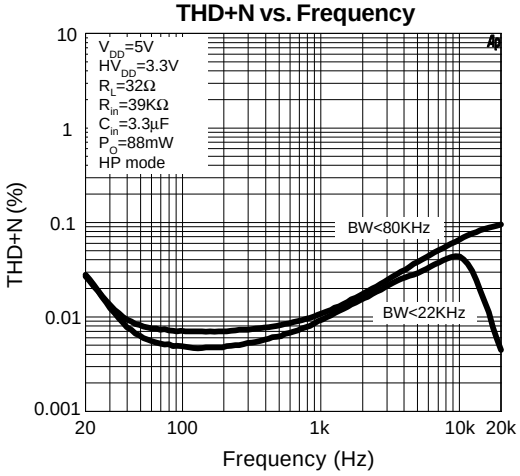
THD+N vs. Output Power



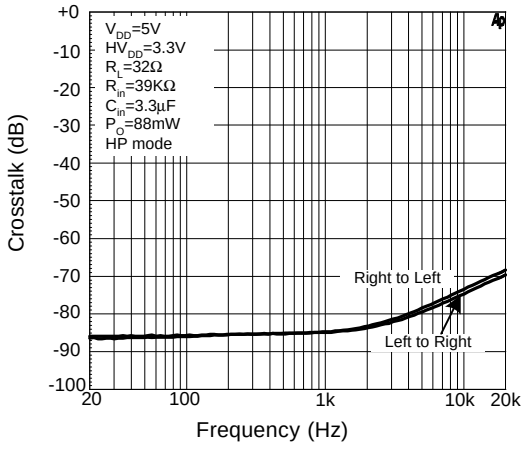
THD+N vs. Output Power



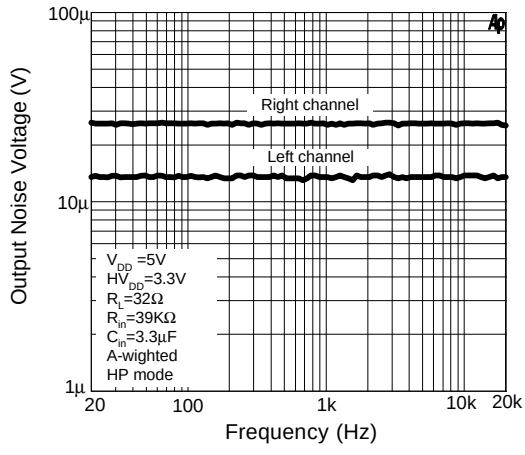
THD+N vs. Frequency



Crosstalk vs. Frequency

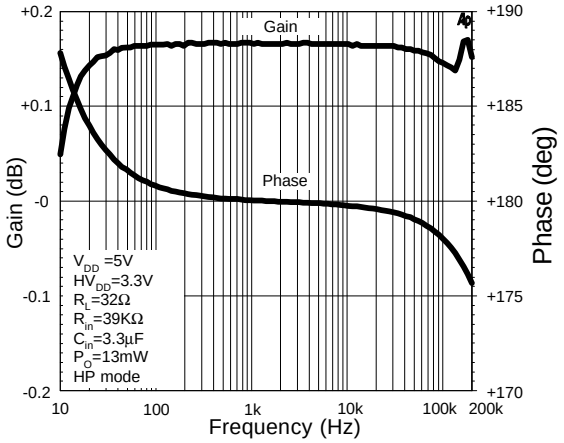


Output Noise Voltage vs. Frequency

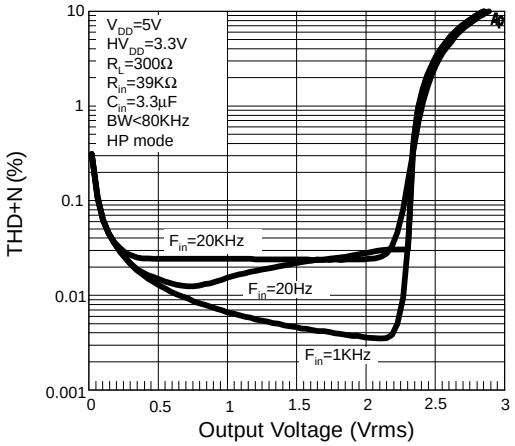


Typical Operating Characteristics (Cont.)

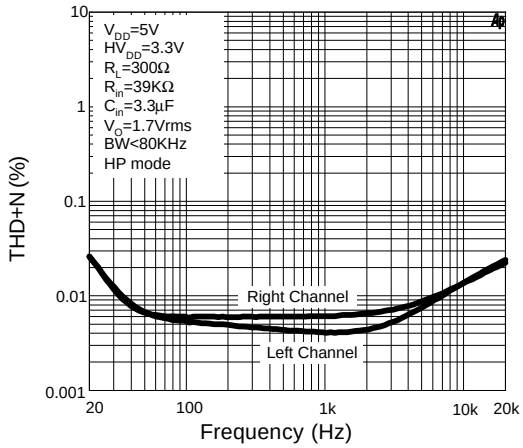
Frequency Response



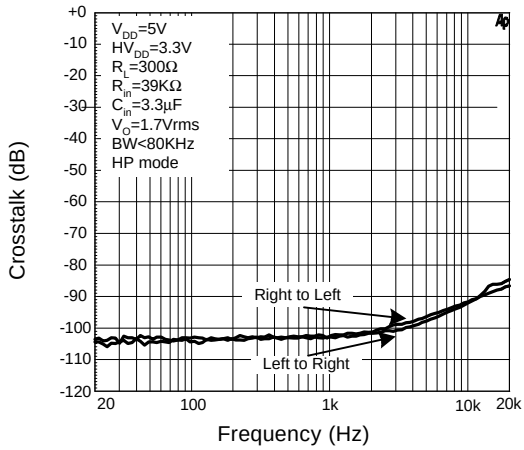
THD+N vs. Output Voltage



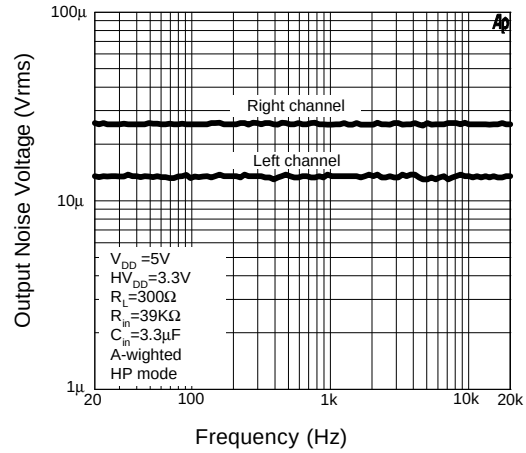
THD+N vs. Frequency



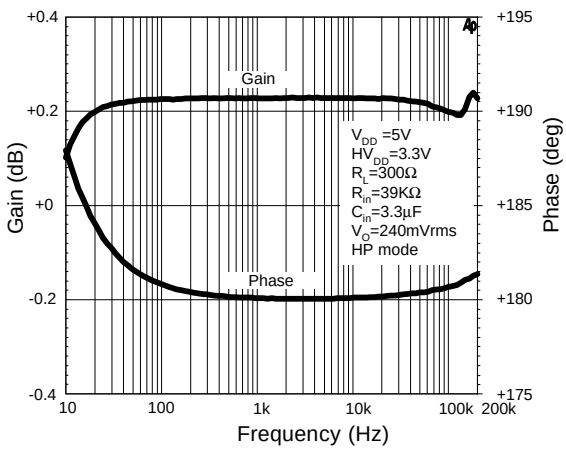
Crosstalk vs. Frequency



Output Noise Voltage vs. Frequency

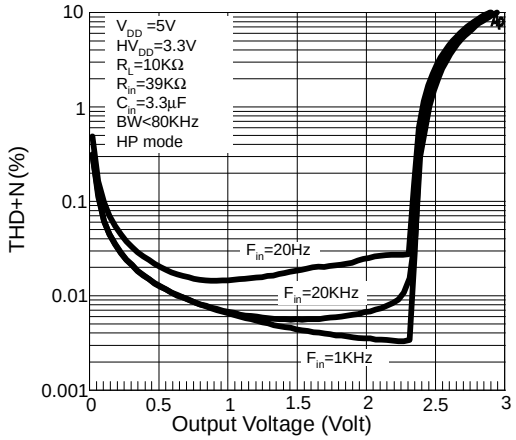


Frequency Response

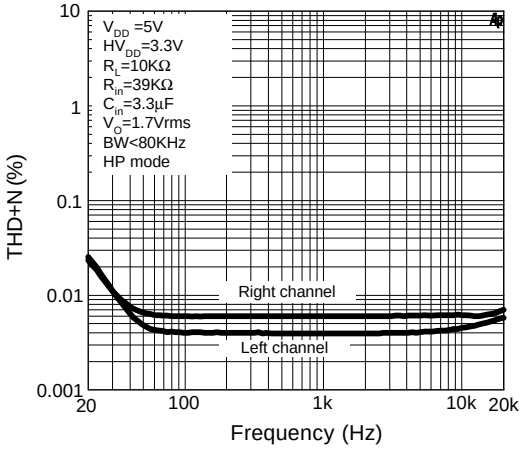


Typical Operating Characteristics (Cont.)

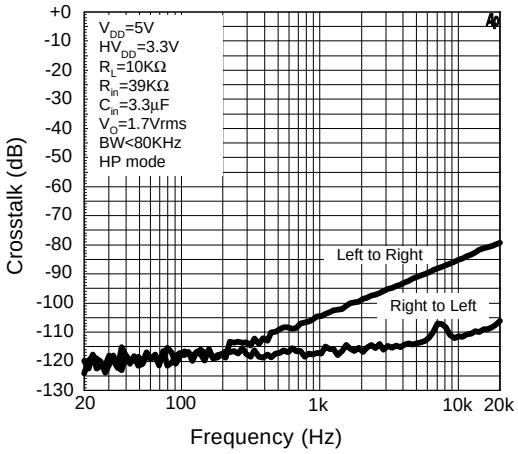
THD+N vs. Output Voltage



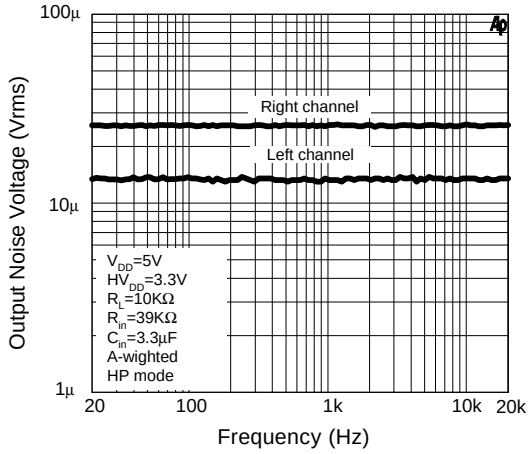
THD+N vs. Frequency



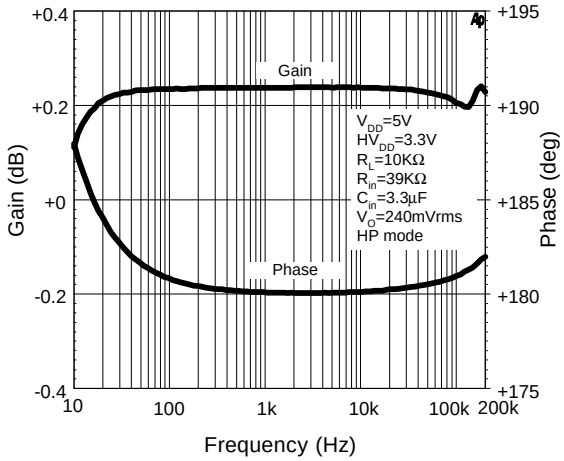
Crosstalk vs. Frequency



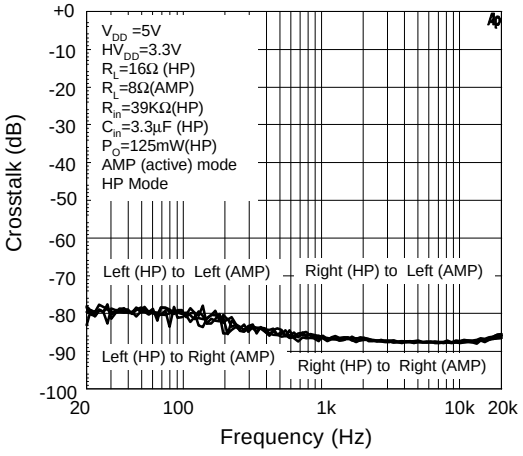
Output Noise Voltage vs. Frequency



Frequency Response

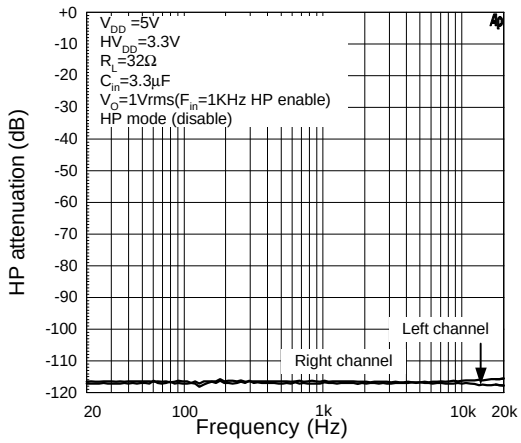


Crosstalk vs. Frequency

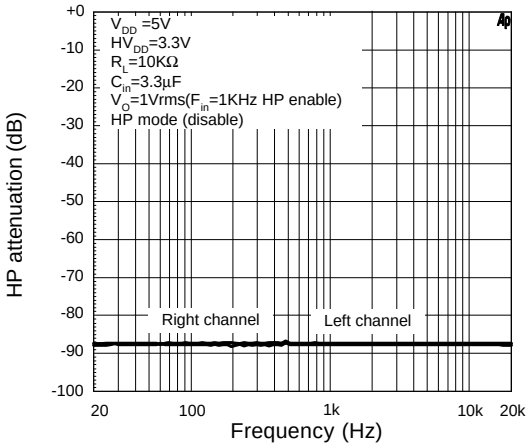


Typical Operating Characteristics (Cont.)

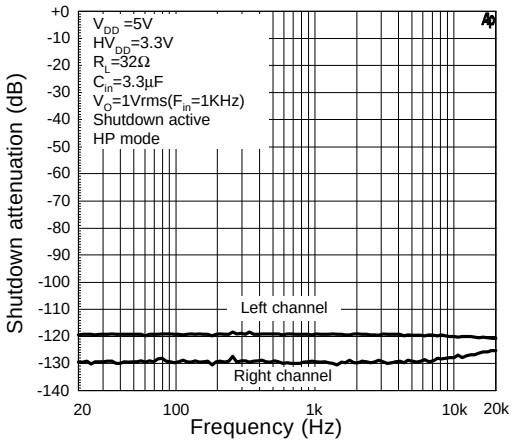
HP attenuation vs. Frequency



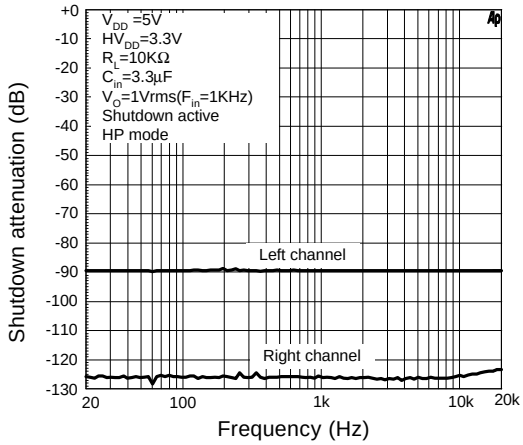
HP attenuation vs. Frequency



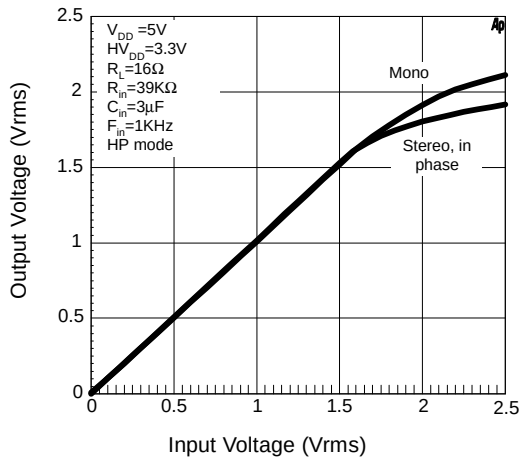
Shutdown attenuation vs. Frequency



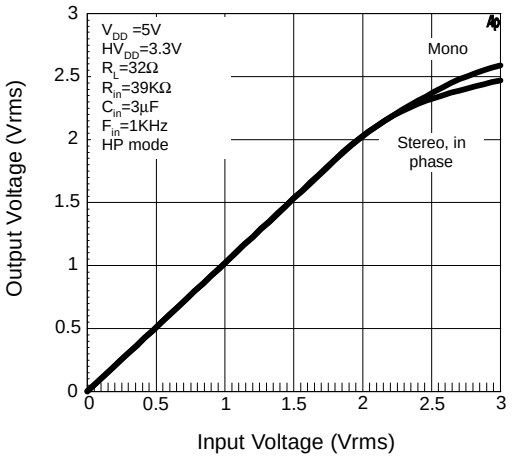
Shutdown attenuation vs. Frequency



Input Voltage vs. Output Voltage

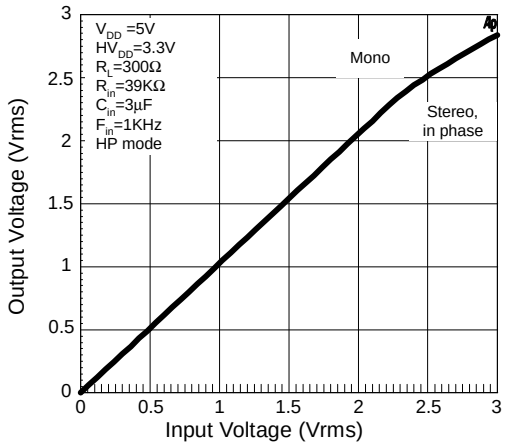


Input Voltage vs. Output Voltage

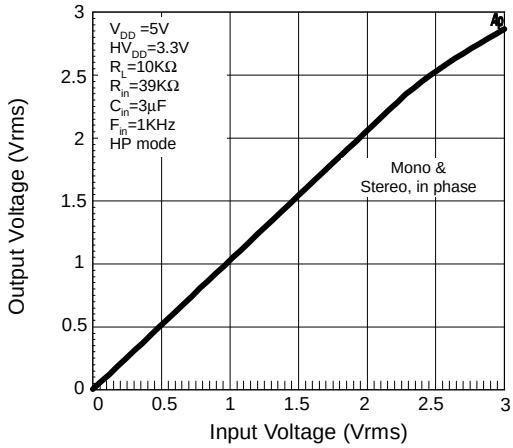


Typical Operating Characteristics (Cont.)

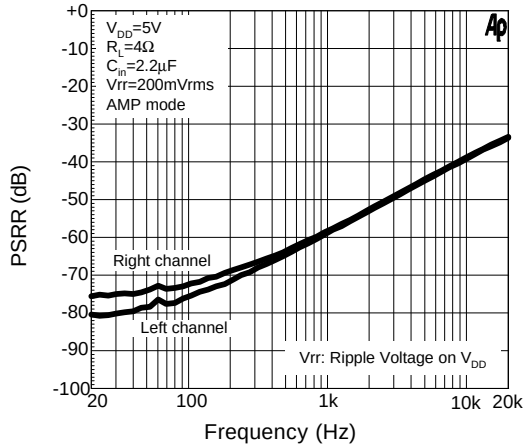
Input Voltage vs. Output Voltage



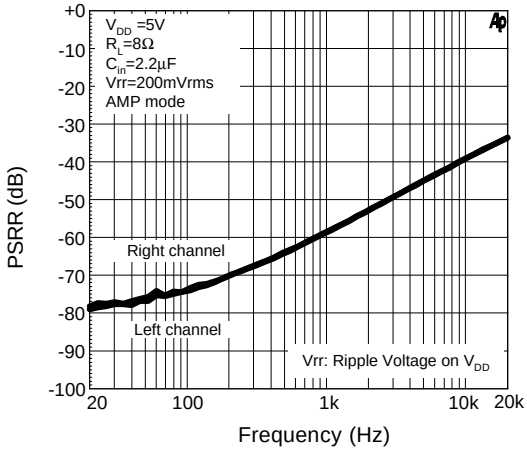
Input Voltage vs. Output Voltage



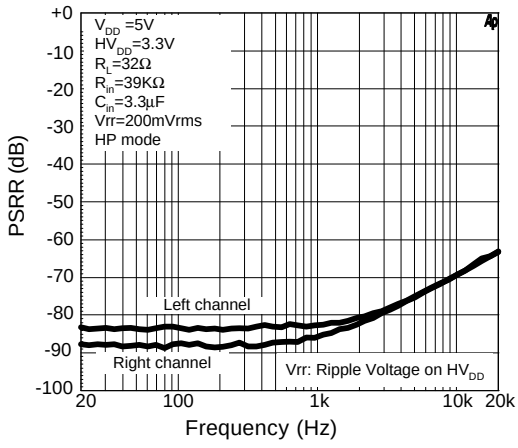
PSRR vs. Frequency



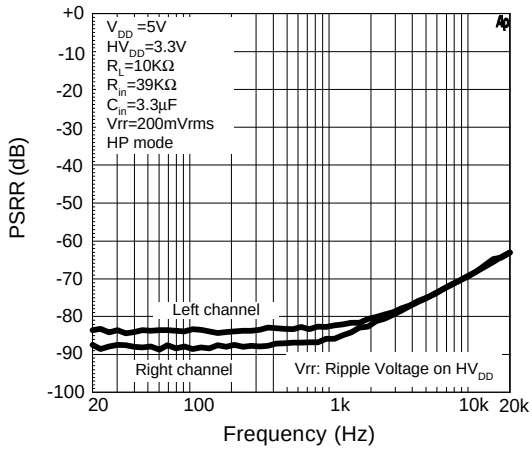
PSRR vs. Frequency



PSRR vs. Frequency

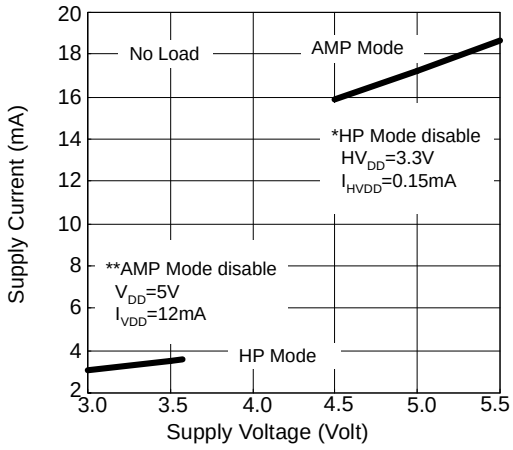


PSRR vs. Frequency

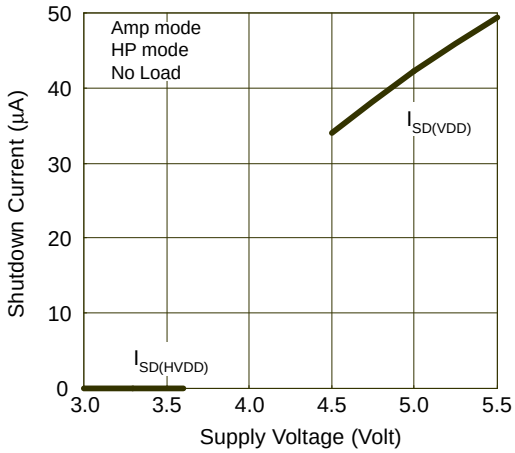


Typical Operating Characteristics (Cont.)

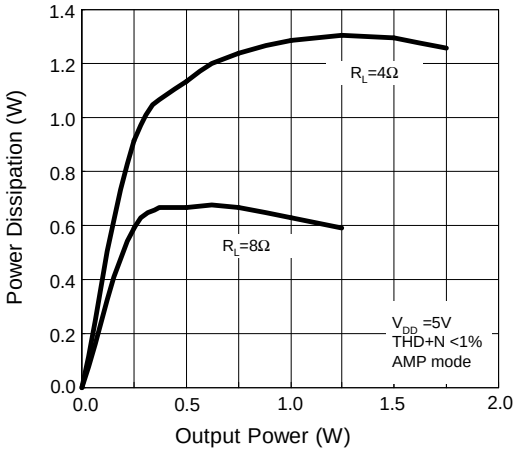
Supply Current vs. Supply Voltage



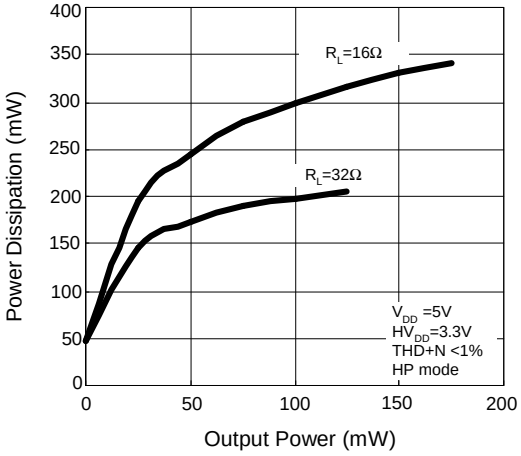
Shutdown Current vs. Supply Voltage



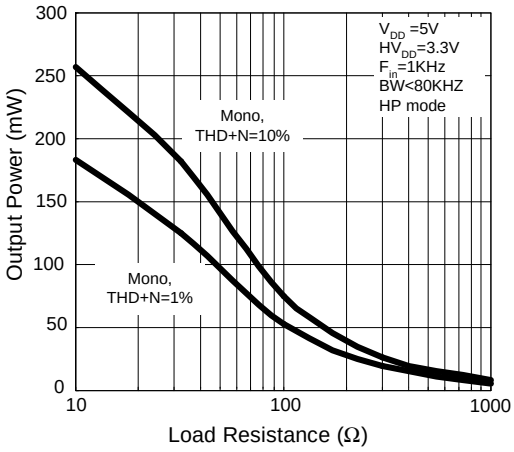
Power Dissipation vs. Output Power



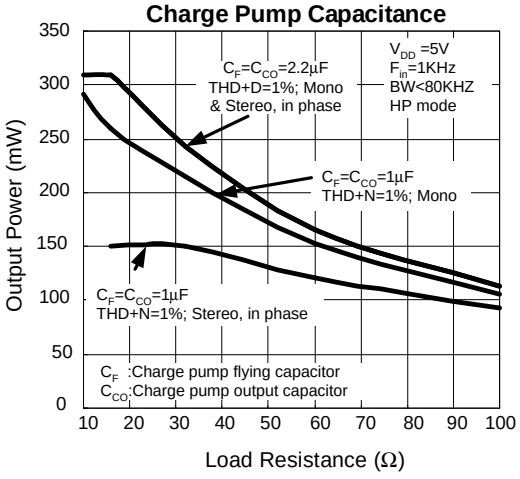
Power Dissipation vs. Output Power



Output Power vs Load Resistance

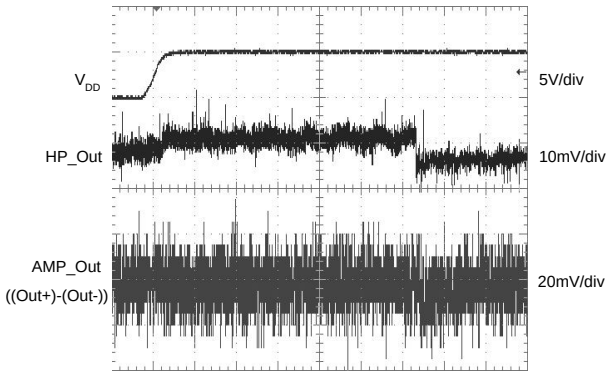


Output Power vs Load Resistance & Charge Pump Capacitance



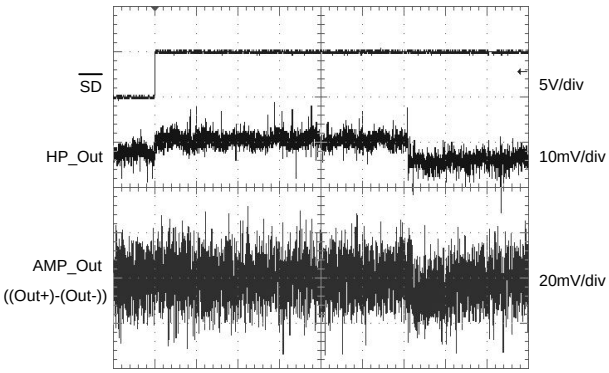
Operating Waveforms

Output Transient at Turn On



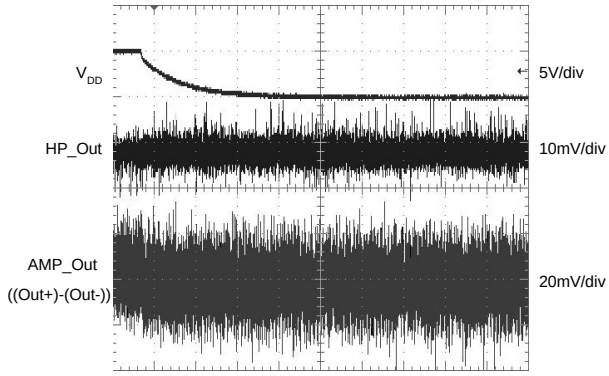
20ms/div

Output transient at Shutdown Release



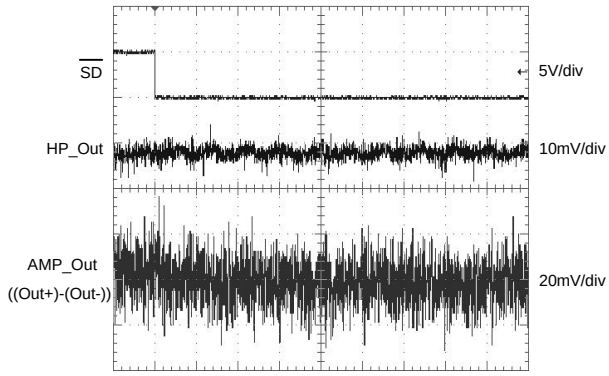
20ms/div

Output Transient at Turn Off



200ms/div

Output transient at Shutdown Active

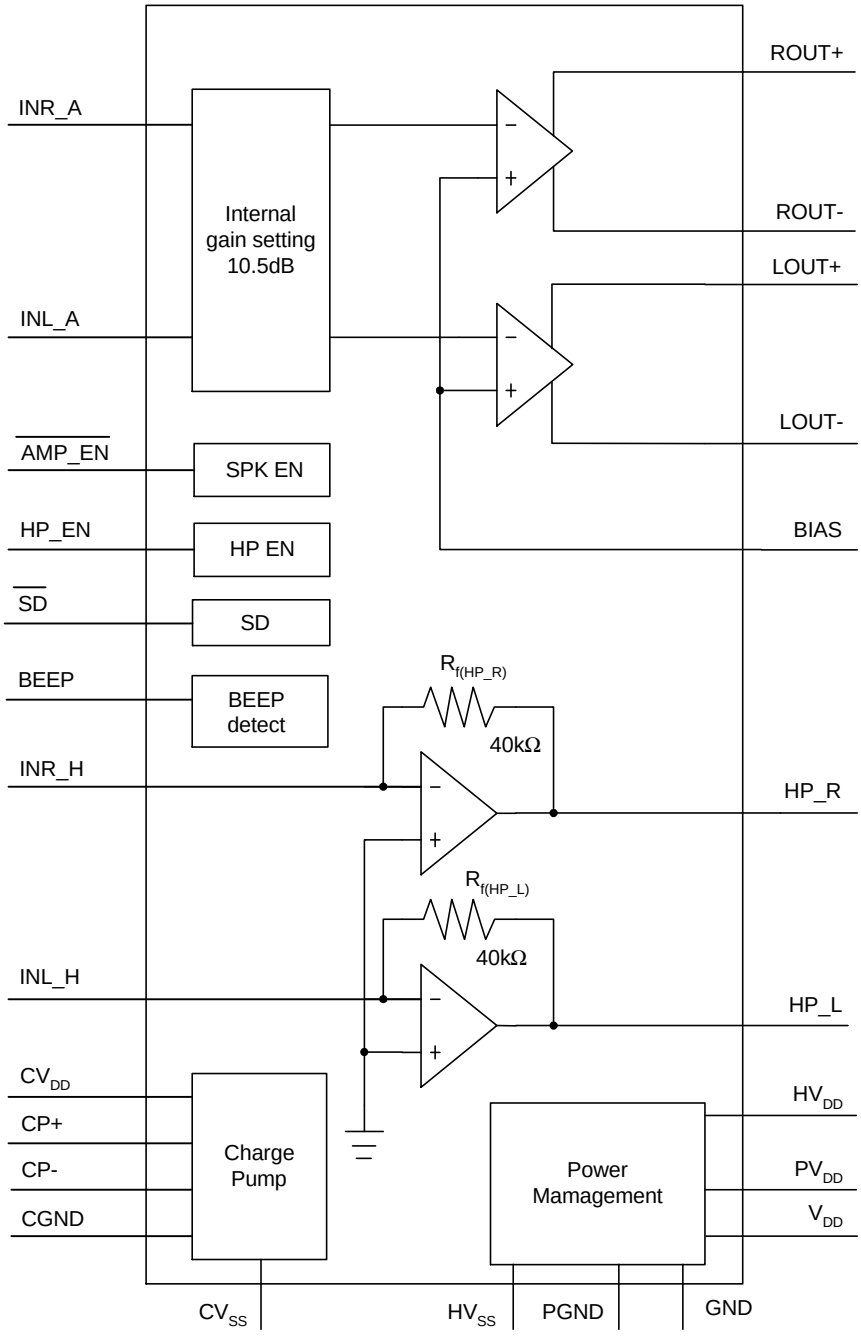


20ms/div

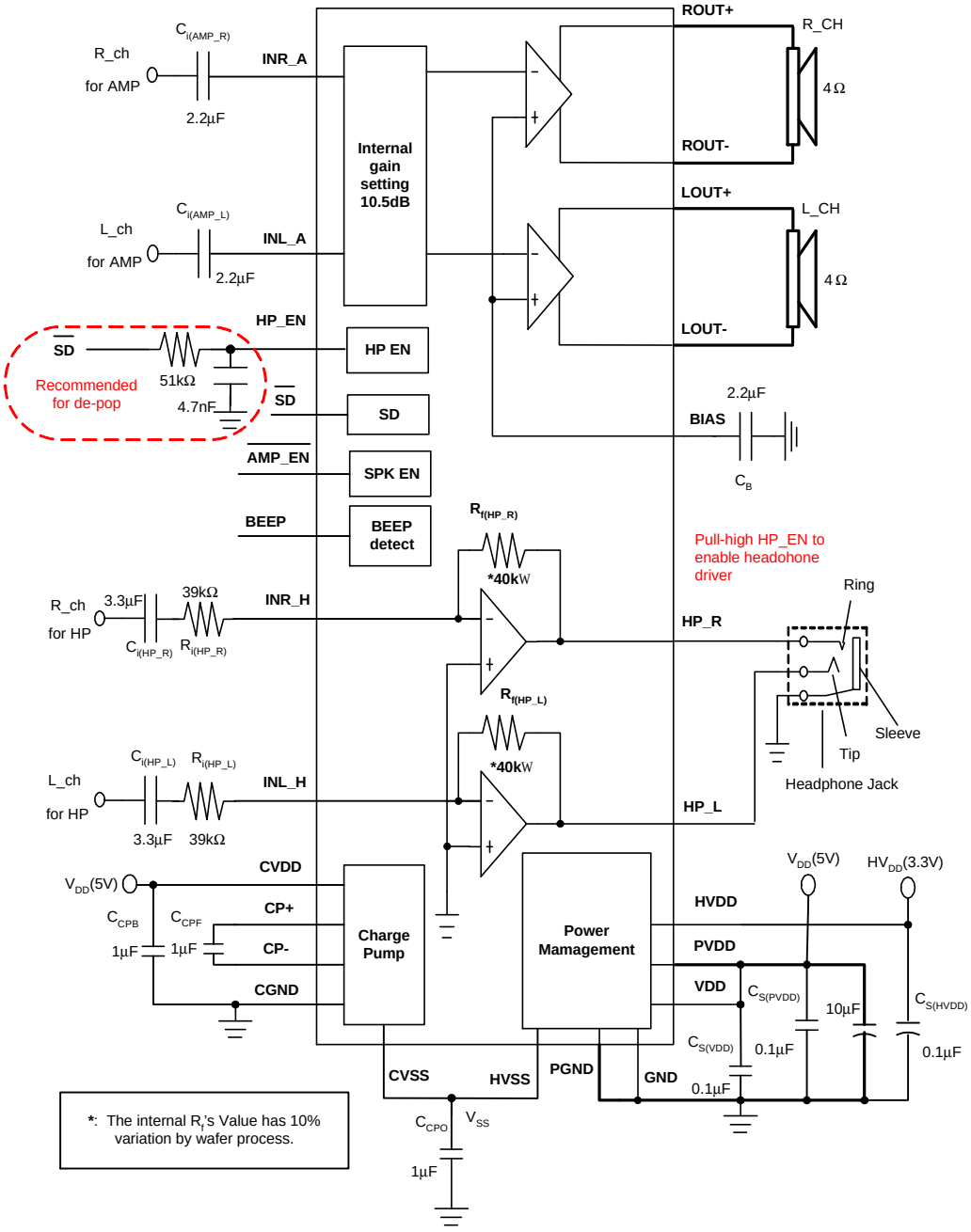
Pin Descriptions

TSSOP-28 NO.	TQFN-28 NO.	Name	Function Description
1	25	VDD	Power supply for control section
2	26	GND	Ground
3	27	INR_A	Right channel input terminal for speaker amplifier
4	28	INR_H	Right channel input terminal for headphone driver
5	1	INL_A	Left channel input terminal for speaker amplifier
6	2	INL_H	Left channel input terminal for headphone driver
7,23	3,19	PGND	Power ground
8	4	LOUT+	Left channel positive output for speaker
9	5	LOUT-	Left channel negative output for speaker
10,20	6,16	PVDD	Power amplifier power supply
11	7	CVDD	Charge pump power supply
12	8	CP+	Charge pump flying capacitor positive connection
13	9	CGND	Charge pump ground
14	10	CP-	Charge pump flying capacitor negative connection
15	11	CVSS	Charge pump output, connect to the “HVSS”
16	12	HVSS	Headphone amplifier negative power supply
17	13	HP_R	Right channel output for headphone
18	14	HP_L	Left channel output for headphone
19	15	HV DD	Headphone amplifier positive power supply
21	17	ROUT-	Right channel negative output for speaker
22	18	ROUT+	Right channel positive output for speaker
24	20	HP_EN	Headphone driver enable pin, pull high to enable headphone mode
25	21	BIAS	Bias voltage generator
26	22	$\overline{SD}$	It will be into shutdown mode when pull now. I_{SD}=80μA
27	23	$\overline{AMP\_EN}$	Speaker driver enable pin, pull low to enable speaker mode
28	24	BEEP	PC BEEP Trigger signal input

Block Diagram



Typical Application Circuit



Application Information

Amplifier Mode Operation

The APA2056A has two pairs of operational amplifiers internally, which allows different amplifier configurations.

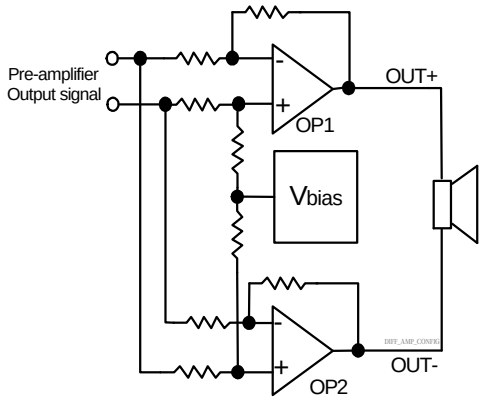


Figure 1: APA2056A internal configuration (each channel)

The OP1 and OP2 are all differential drive configurations. The differential drive configurations doubling the voltage swing on the load. Compare with the single-ending configuration, the differential gain for each channel is 2X (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration commonly referred to all differential mode is established. All differential mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A differential amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus it is doubling the output swing for a specified supply voltage. The output power can be 4 times greater than the SE amplifier working under the same condition. A differential configuration, similar as the one used in APA2056A, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, there is no need for DC voltage across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Headphone Mode Operation

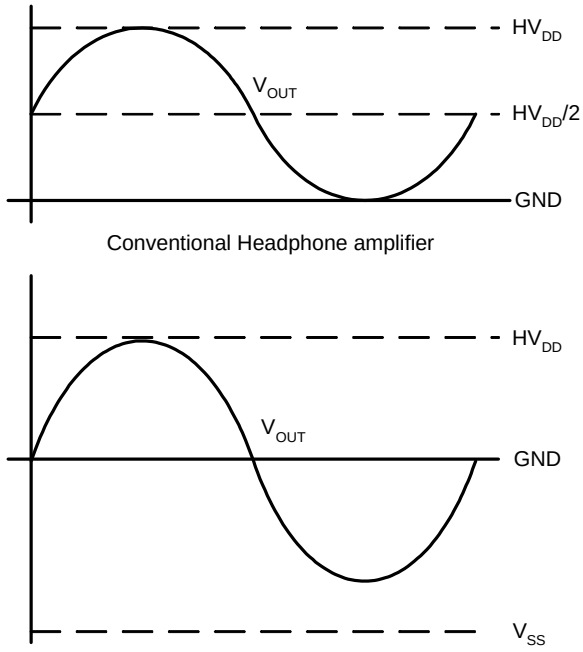


Figure 2: Cap-free Operation

The APA2056A's headphone amplifiers uses a charge pump to invert the positive power supply (CV_{DD}) to negative power supply (CV_{SS}), see Figure2. The headphone amplifiers operate at this bipolar power supply (HV_{DD} & V_{SS}), and the outputs reference refers to the ground. This feature eliminates the output capacitor that is using in conventional single-ended headphone amplifier. The headphone amplifier internal supply voltage comes from HV_{DD} and V_{SS}. For good AC performance, the HV_{DD} connected to 3.3V is recommended. It can avoid the output over voltage for line out application.

Charge Pump Flying Capacitor

The flying capacitor (C_{CPF}) affects the load transient of the charge pump. If the capacitor's value is too small, then that will degrade the charge pump's current driver capability and the performance of headphone amplifier.

Increasing the flying capacitor's value will improve the load transient of charge pump. It is recommend to use the low ESR ceramic capacitors (X7R type is recommended) above 1μf.

Application Information (Cont.)

Charge Pump Output Capacitor

The output capacitor (C_{CPO})'s value affects the power ripple directly at CV_{SS}(V_{SS}). Increasing the value of output capacitor reduces the power ripple. The ESR of output capacitor affects the load transient of CV_{SS}(V_{SS}). Lower ESR and greater than 1μf ceramic capacitor (X7R type is recommended) is recommendation.

Charge Pump Bypass Capacitor

The bypass capacitor (C_{CPB}) relates with the charge pump switching transient. The capacitor's value is same as flying capacitor (1μf). Place it close to the CV_{DD} and PGND.

Headphone Detection Input

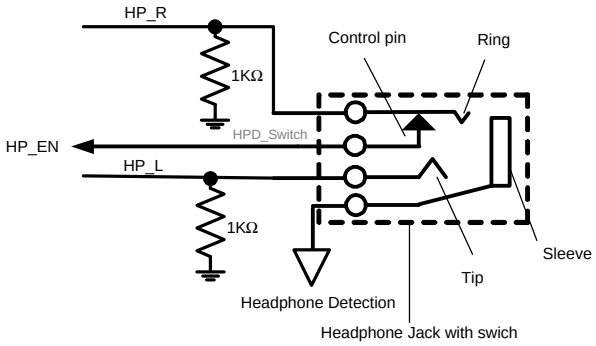


Figure 3 HPD configurations

The HP_EN will detect the voltage. If the voltage is less than 0.8V, the headphone amplifiers will be disabled; if greater than 2V, then the headphone amplifier will be enabled.

In Figure 3, phone-jack with the control pin is used and connected to HP_EN input from control pin. When a headphone plug is inserted, the HP_EN will pull high internally which enables headphone amplifiers; without headphone plug, the HP_EN is pulled to GND.

Operation Mode

The APA2056A amplifier has two pairs of independent amplifier. One for stereo speaker is BTL structure, and the other for headphone is cap-less structure. Each pair has independent input pin; INR_A and INA_L are for stereo speaker drivers, and INR_H and INL_H are for stereo headphone drivers.

- Amplifier mode operation: Pull low the $\overline{\text{AMP\_EN}}$ control pin can enable the stereo speaker driver.
- Headphone mode operation: Pull high the HP_EN control pin can enable the cap-less headphone drive.
- Both amplifier and headphone "ON" mode: Pull low the $\overline{\text{AMP\_EN}}$ and pull high the HP_EN control pins, then turn on both speaker drivers and headphone drivers
- Both amplifier and headphone "OFF" mode: Pull high the $\overline{\text{AMP\_EN}}$ and pull low the HP_EN control pins, then turn off both speaker drivers and headphone drivers

If the $\overline{\text{AMP\_EN}}$ and HP_EN are connected together, then this pin will be connected to headphone jack's control pin (Figure 3), the APA2056A is switchable between "Amplifier mode (Headphone mute), or Headphone mode (Amplifier mute).

Gain Setting

The gain for speaker driver is 10.5dB, but it can low down the gain by external input resistor (Ri.external). that add on INR_A and INL_A input pins. The Table 1 shows the reference gain setting with external input resistor (Ri. external) for speaker amplifier (AMP Mode).

For headphone driver, the internal feedback resistor is 40kΩ ($R_{f(HP)}$external, 10% variation by process), so the headphone driver's gain is setting by the input resistor ($R_{i(HP)}$ external), the Table 1 show the reference gain setting with external resistor for headphone driver (HP Mode).

AMP Mode Gain Setting Table for Reference			
APA2056A AMP Mode gain is 10.5dB default			
R_i,extena l(kΩ)	OUTP (V/V)	BTL O/P (V/V)	Gain (dB)
6.2	1.25	2.51	8.0
3.3	1.42	2.85	9.1
1	1.59	3.19	10.1
0	1.68	3.36	10.5
HP Mode Gain Setting Table for Reference			
$R_{i(HP)}$,external (kΩ)	*$R_{f(HP)}$,internal (kΩ)	HP OUT (V/V)	HP Gain(dB)
62	40	0.65	-3.8
50	40	0.80	-1.9
39	40	1.03	0.2
30	40	1.33	2.5
24	40	1.67	4.4
20	40	2.00	6.0

*The internal Rf's value has 10% variation by process.

Application Information (Cont.)

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance Ri from a high-pass filter with the corner frequency are determined by the following equation:

$$F_C\,(\text{highpass}) = \frac{1}{(2\pi R_{i(MIN)} \times C_i)} \qquad (1)$$

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where R_i is 10kΩ and the specification calls for a flat bass response down to 10Hz. Equation is reconfigured as below:

$$C_i = \frac{1}{(2\pi R_i Fc)} \qquad (2)$$

Consider to input resistance variation, the C_i is 1.6µF, so one would likely choose a value in the range of 2.2µF to 3.3µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i+R_f, C_i) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input. As the DC level is held at V_{DD}/2, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Note: The headphone dirver's input is ground reference, so please check the $C_{i(HP)}$'s polarized at design.

Effective Bias Capacitor, C_B

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger bypass capacitor is improved PSRR due to increased 1.8V bias voltage stability. Typical applications employ a 5V regulator with 2.2µF and a 0.1µF bypass capacitor, which aids in supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA2056A. The selection of bypass capacitors, especially C_B, is thus dependent upon desired PSRR requirements and click-and-pop performance.

Power Supply Decoupling, C_s

The APA2056A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitor that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF, is placed as close as possible to the device V_{DD} lead works best (the pin1 (V_{DD}) and pin2 (GND)'s capacitor must short less than 1cm). For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater is placed near the audio power amplifier is recommended.

Shutdown Function

In order to reduce power consumption while not in use, the APA2056A contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the SET pin. The trigger point between a logic high and logic low level is typically 2.0V. It is the best to switch between ground and the supply V_{DD} to provide maximum device performance.

By switching the SET pin to low, the amplifier enters a low-current consumption state, I_{DD}<80µA. Even the APA2056A is in shutdown mode, PC_BEEP will keep detecting circuit. In normal operating, SET pin is pulled to high level to keep the IC out of the shutdown mode. The SET pin should be tied to a definite voltage to avoid unwanted state changes.The wake-up time of shutdown is about 150ms, and the shutdown release's pop is caused by the operational amplifier's offset.

PC-BEEP Detection

The APA2056A integrates a PCBEEP circuit detection for notebook PC using. When PC-BEEP signal

Application Information (Cont.)

Shutdown Function (Cont.)

drives to PCBEEP input pin, PCBEEP mode is active. The APA2056A will turn on speaker drivers and the internal gain is fixed as 0dB. The PCBEEP signal becomes the amplifiers input signal. If the amplifiers in the shutdown mode, it will be out of shutdown mode whenever PCBEEP mode is enabled. The APA2056A will return to previous setting when it is out of PC BEEP mode. The input impedance is 100KΩ on PCBEEP input pin.

Speaker Driver Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{Psup} \quad (3)$$

Where:

$$P_O = \frac{V_O rms * V_O rms}{R_L} = \frac{(V_P * V_P)}{2R_L} \quad (4)$$

$$V_O rms = \frac{V_P}{\sqrt{2}} \quad (5)$$

$$Psup = V_{DD} * I_{DD}(AVG) = V_{DD} * \frac{2V_P}{\pi R_L} \quad (6)$$

Efficiency of a Differential configuration:

$$\frac{P_O}{Psup} = \left\{\frac{(V_P * V_P)}{2R_L}\right\} / \left\{V_{DD} * \frac{2V_P}{\pi R_L}\right\} = \frac{\pi R_L}{4V_{DD}} \quad (7)$$

Table 1 calculates efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8W loads and a 5V supply, the maximum draw on the power supply is almost 3W.

Po (W)	Efficiency (%)	IDD(A)	VPP(V)	PD (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

**High peak voltages cause the THD+N to increase

Table 2. Efficiency vs. Output Power in 5-V/8W Differential Amplifier Systems.

A final point to remember about linear amplifiers is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, using the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. Equation 8 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode: } P_{D,MAX} = \frac{V_{DD}^2}{2\pi R_L} \quad (8)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode: } P_{D,MAX} = \frac{4V_{DD}^2}{2p^2 R_L} \quad (9)$$

Since the APA2056A is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depending on the mode of operation. Even with this substantial increasing in power dissipation, the APA2056A does not require extra heatsink. The power dissipation from equation 9, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation 9:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \quad (10)$$

For TSSOP-28 package with thermal pad, the thermal resistance (θ_{JA}) is equal to 45°C/W.

Since the maximum junction temperature ($T_{J,MAX}$) of APA2056A is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation that the IC package is able to handle can be obtained from equation10. Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Application Information (Cont.)

Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the APA2056A requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA2056A 4Ω will go into thermal shutdown when driving a 4Ω load. The thermal pad on the bottom of the APA2056A should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 15 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane. For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA2056A junction temperature below the thermal shutdown temperature (150°C).

In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown. See Demo Board Circuit Layout as an example for PCB layout.

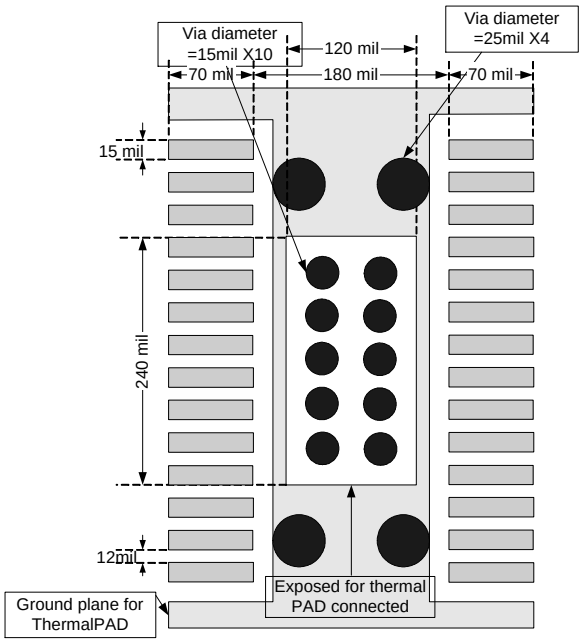


Figure 5: TSSOP-28P layout recommendation

Thermal Considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. In the Power Dissipation vs. Output Power graph, the APA2056A is operating at a 5V supply and a 4Ω speaker that 2W output power peaks are available. The vertical axis gives the information of power dissipation (P_D) in the IC with respect to each output driving power (P_O) on the horizontal axis.

This is valuable information when attempting to estimate the heat dissipation of the IC requirements for the amplifier system.

Using the power dissipation curves for a 5V/4Ω system, the internal dissipation in the APA2056A and maximum ambient temperatures is shown in Table 3.

Peak output power (W)	Average output power (W)	Power dissipation (W/channel)	Max. T_A (°C)
			With thermal pad
2	1.95	1.25	37
2	1.17	1.25	37
2	0.74	1.19	43
2	0.43	1.05	55
2	0.19	0.8	78

Table 3: APA2056A Power information, 5V/4Ω, Stereo, Differential mode

Package	q_{JA}
TSSOP-28	45°C/W
TQFN -28	43°C/W

Table 4: Thermal resistance Table

This parameter is measured with the recommended copper heat sink pattern on a 2-layer PCB, 23cm² in 5.7mm*4mm in PCB, 2oz. Copper, 100mm² coverage. Airflow 0 CFM the maximum ambient temperature depends on the heat sink ability of the PCB system.

To calculate maximum ambient temperatures, first consideration is that the numbers from the dissipation graphs are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation.

Given θ_{JA}, the maximum allowable junction temperature ($T_{J,Max}$), and the total intemal dissipation (P_D), the maximum ambient temperature can be calculated with the following

Application Information (Cont.)

Thermal Considerations (Cont.)

equation. The maximum recommended junction temperature for the APA2056A is 150°C. The internal dissipation figures are taken from the Power Dissipation vs. Output Power graph.

$$T_{A,Max} = T_{J,Max} - \theta_{JA} P_D \quad (11)$$

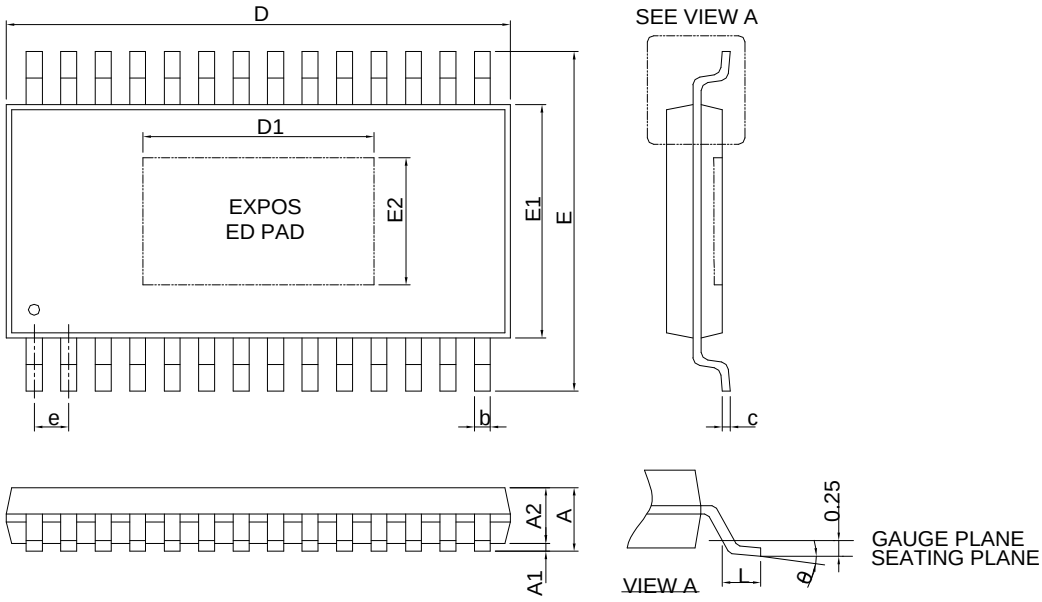
150 - 45(0.8*2) = 78°C (with thermal pad)

NOTE: Internal dissipation of 0.8W is estimated for a 2W system with 15-dB headroom per channel.

Table 3 shows that for some applications, no airflow is required to keep junction temperatures in the specified range. The APA2056A is designed with a thermal shut-down protection that turns the device off when the junction temperature surpasses 150°C to prevent IC from damage. The information in table 3 was calculated for maximum listen volume with limited distortion. When the output level is reduced, the numbers in the table change significantly. Also, using 8Ω speakers will dramatically increase the thermal performance by increasing amplifier efficiency.

Package Information

TSSOP-28P

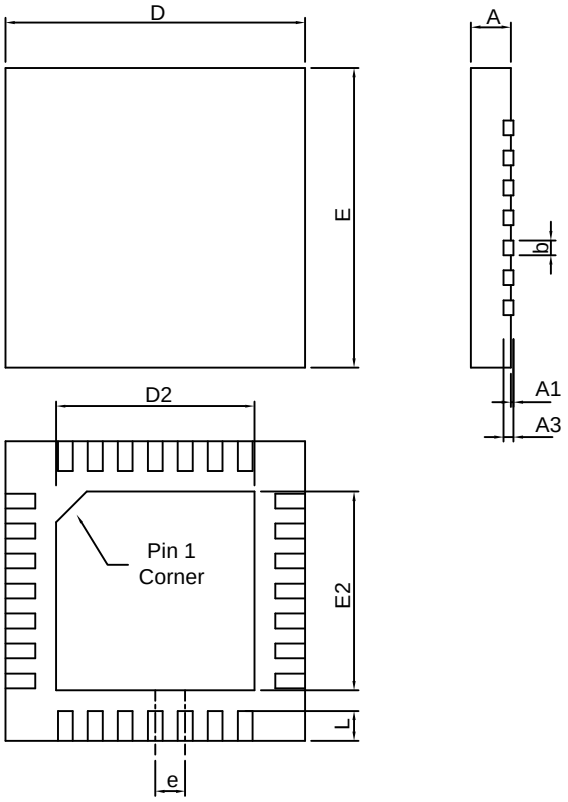


SYMBOL	TSSOP-28P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	9.60	9.80	0.378	0.386
D1	3.30	7.00	0.130	0.276
E	6.40 BSC		0.252 BSC	
E1	4.30	4.50	0.169	0.177
E2	1.50	4.00	0.059	0.157
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0 °	8 °	0 °	8°

Note : 1. Followed from JEDEC MO-153 AET.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

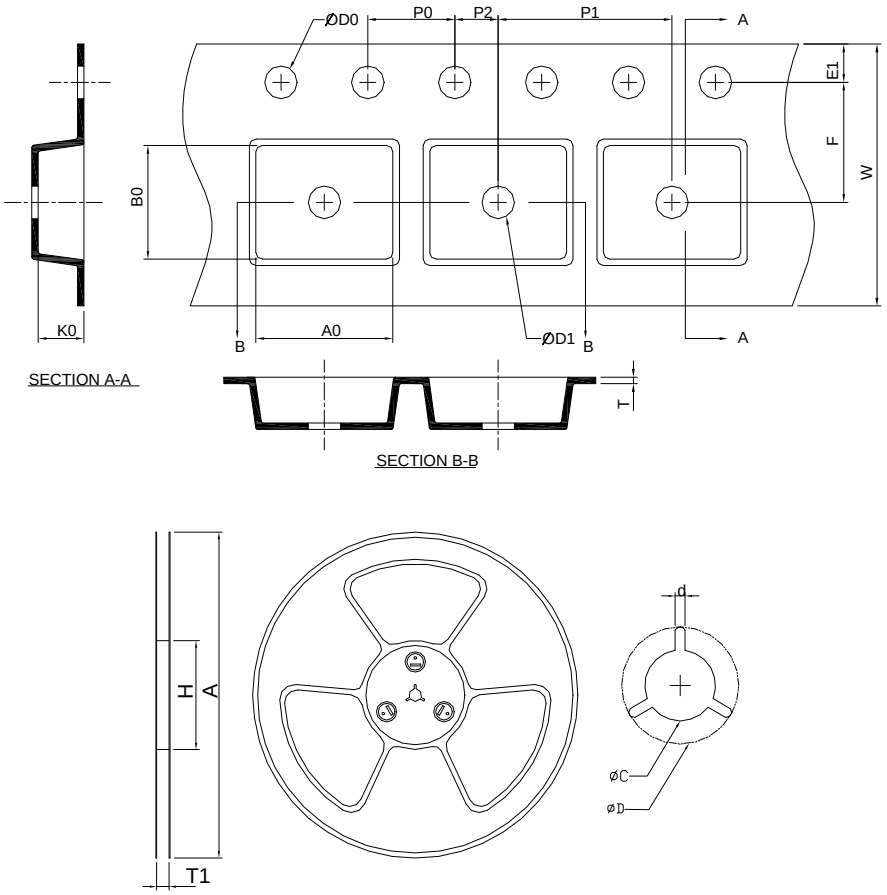
Package Information

TQFN5x5-28



SYMBOL	TQFN5x5-28			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	5.00 BSC		0.197 BSC	
D2	3.50	3.80	0.138	0.150
E	5.00 BSC		0.197 BSC	
E2	3.50	3.80	0.138	0.150
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018

Carrier Tape & Reel Dimensions



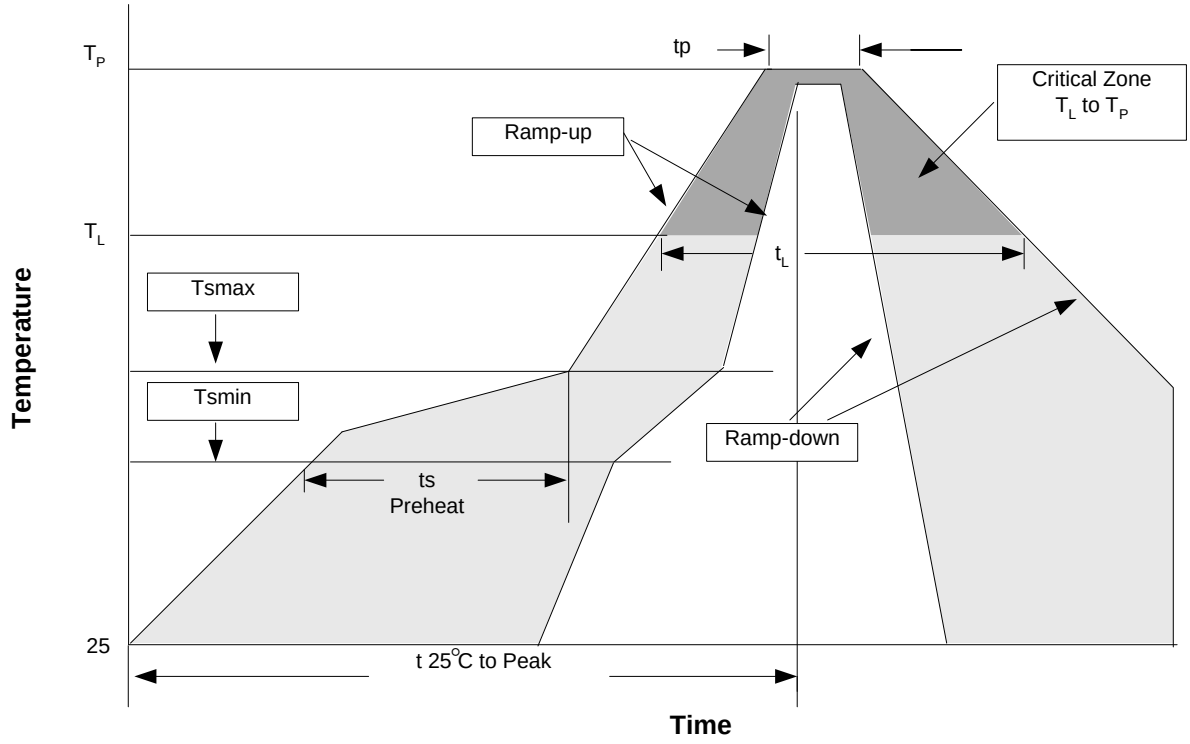
Application	A	H	T1	C	d	D	W	E1	F
TSSOP-28P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.90±0.20	10.2±0.20	1.50±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TQFN5x5-28	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	5.30±0.20	1.30±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
TSSOP- 28P	Tape & Reel	2000
TQFN5x5-28	Tape & Reel	2500

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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