D/A Converter Series for Electronic Adjustment

10bit 8ch/10ch D/A Converters

BU2505FV BU2506FV

General Description

The BU2505FV and BU2506FV ICs are 10bit R-2R type D/A converters with 10ch and 8ch outputs, respectively. Cascade connection is available, ensuring suitability for multi-channel applications. Each channel incorporates a full swing output type buffer amplifier with high speed output response characteristics, resulting in a greatly shortened D/A output settling time. The ICs also have digital input pins compatible with TTL levels, and the maximum value of the data transfer frequency is 10MHz. With the variable output range function, the upper and lower limits of the output voltage can be set separately from the power supply voltage.

Features

- Built-in Multi-channel R-2R Type 10bit D/A Converter (BU2506FV: 8 Channels, BU2505FV: 10 Channels)
- Built-in Full Swing Output Buffer Amplifier for All Channels
- RESET Terminal to fix the Output Voltage to the Lower Reference Level for All Channels
- Digital Inputs Compatible with TTL Levels
- 3-wire Serial Interface and RESET Signal to send a 14bit Format Word (4bit Address and 10bit Data)
- REVERSE Terminal to select LSB First or MSB First of 10bit Data
- Cascade Connection is Available

Applications

- Control of the Various Types of Consumer and Industrial Equipment

Key Specifications

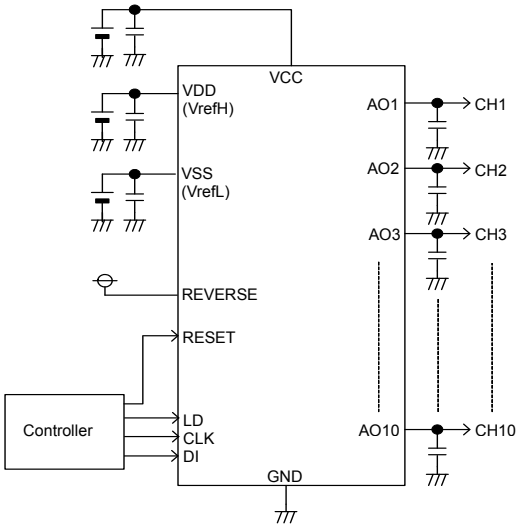
- Operating Supply Voltage Range : 4.5V to 5.5V
- Number of Channels :
  - BU2505FV : 10ch
  - BU2506FV : 8ch
- Differential Non Linearity Error : ±1.0LSB(Max)
- Integral Non Linearity Error : ±3.5LSB(Max)
- Data Transfer Frequency : 10MHz(Max)

Packages

	W(Typ) x D(Typ) x H(Max)
SSOP-B20	6.50mm x 6.40mm x 1.45mm

SSOP-B20

Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

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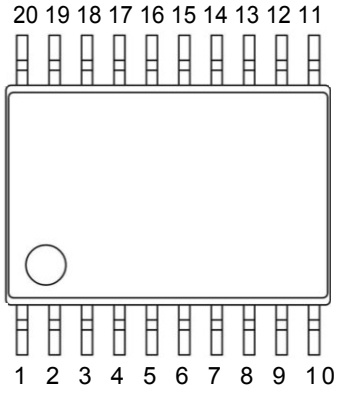
Pin Configurations

SSOP-B20
(TOP VIEW)



Pin Descriptions

No.	Terminal Name	Analog / Digital	I/O	Description		Equivalent circuit No.
				BU2505FV	BU2506FV	
1	VSS	Analog	-	D/A converter lower reference voltage (V_{refL}) input terminal		6
2	AO3	Analog	O	10bit D/A output(CH3)		4
3	AO4	Analog	O	10bit D/A output(CH4)		4
4	AO5	Analog	O	10bit D/A output(CH5)		4
5	REVERSE	Digital	I	Reverses the 10bit designated as data in the 14bit to select MSB first or LSB first.(Note 1)		2
6	RESET	Digital	I	Fixes the output voltage to the lower reference level for all channels.		2
7	AO6	Analog	O	10bit D/A output(CH6)		4
8	AO7	Analog	O	10bit D/A output(CH7)		4
9	AO8	Analog	O	10bit D/A output(CH8)		4
10	VDD	Analog	-	D/A converter upper reference voltage (V_{refH}) input terminal		5
11	VCC	-	-	Power supply		-
12	AO9(TEST1)	Analog	O	10bit D/A output(CH9)	test terminal (Note 2)	4
13	AO10(TEST2)	Analog	O	10bit D/A output(CH10)	test terminal (Note 2)	4
14	DO	Digital	O	Outputs the LSB data of 14bit shift resister.		3
15	LD	Digital	I	When the LD terminal is set to the high level voltage, 14bit data in the shift register is loaded on to the address decoder and a specified D/A output register.		1
16	CLK	Digital	I	Shift clock input terminal. At the rising edge of the CLK input, an input value on the DI terminal is input to the 14bit shift register.		1
17	DI	Digital	I	Serial data input terminal. Serial data length is 14bit (4bit address and 10bit data).		1
18	AO1	Analog	O	10bit D/A output(CH1)		4
19	AO2	Analog	O	10bit D/A output(CH2)		4
20	GND	-	-	GND terminal		-

(Note 1) It is selectable for the IC to receive 10bit data in LSB first order or MSB first order, depending on the condition of the REVERSE terminal. If the REVERSE terminal is set to the GND voltage, it is MSB first
(Note 2) The TEST1 and TEST2 terminals of the BU2506FV should be left open. These terminals are used for testing.

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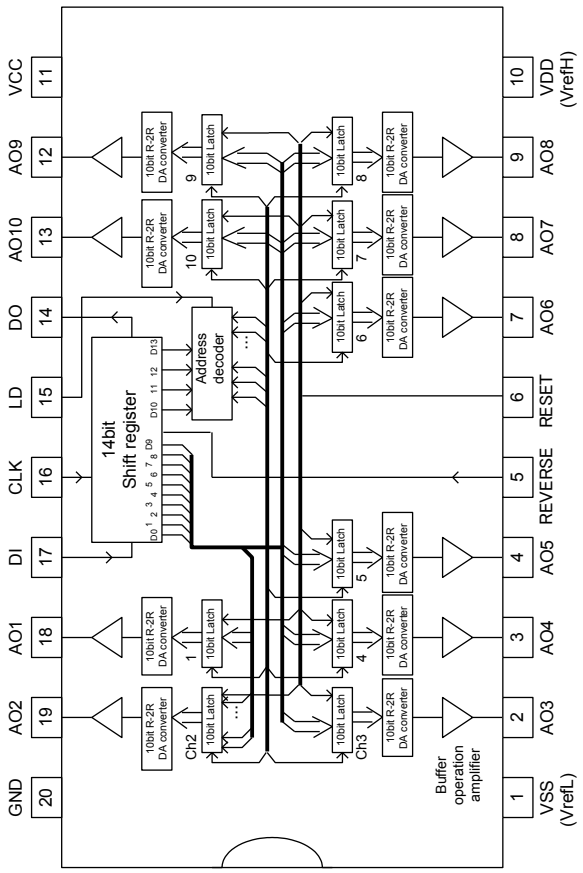
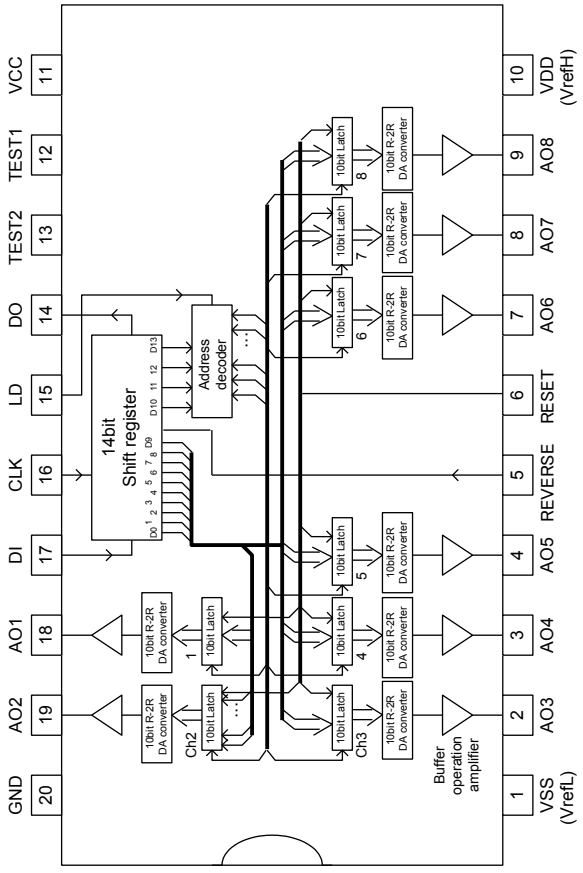
Block Diagrams

BU2505FV



BU2506FV



Absolute Maximum Ratings(T_A=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	6.0	V
D/A converter upper reference voltage	V_{DD}	6.0	V
Input voltage	V_{IN}	6.0	V
Output voltage	V_{OUT}	6.0	V
Power dissipation	P_D	0.75(Note 3)	W
Storage temperature range	T_{stg}	-55 to +125	°C

(Note 3) Derate by 7.5mW/°C when operating above T_A=25°C (when mounted on ROHM's standard board).
Mounted on a FR4 glass epoxy PCB 70mm x 70mm x 1.6mm (copper foil area less than 3%).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limit	Unit
Supply voltage range	V_{CC}	4.5 to 5.5	V
Operating temperature range	T_{opr}	-30 to +85	°C

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Electrical Characteristics(Unless otherwise specified, V_{CC}=5V, V_{refH}=5V, V_{refL}=0V, T_A=25°C)

Parameter		Symbol	Limit Min	Limit Typ	Limit Max	Unit	Conditions
<Digital unit>							
Supply current		I_{CC}	-	0.85	2.8	mA	At CLK=10MHz, I_{AO}=0μA
Input leak current		I_{ILK}	-5	-	+5	μA	V_{IN}=0V to V_{CC}
Input voltage L		V_{IL}	-	-	0.8	V	-
Input voltage H		V_{IH}	2.0	-	-	V	-
Output voltage L		V_{OL}	0	-	0.4	V	I_{OL}=+2.5mA
Output voltage H		V_{OH}	4.6	-	5	V	I_{OH}=-2.5mA
<Analog unit>							
Consumption current		I_{refH}	-	4.5	7.5	mA	Data condition : at maximum current
			-	3.7	6.2	mA	(Note 4)
D/A converter upper reference voltage setting range		V_{refH}	3.0	-	5	V	-
D/A converter lower reference voltage setting range		V_{refL}	0	-	1.5	V	
Buffer amplifier output voltage range		V_O	0.1	-	4.9	V	I_O=±100μA
			0.2	-	4.75		I_O=±1.0mA
Buffer amplifier output drive range		I_O	-2	-	+2	mA	High side saturation voltage =0.35V (on full scale setting, current sourcing) Low side saturation voltage =0.23V (on zero scale setting, current sinking)
Precision	Differential non-linearity error	DNL	-1.0	-	+1.0	LSB	V_{refH} =4.796V V_{refL}=0.7V V_{CC}=5.5V (4mV/LSB) At no load (I_O=+0mA)
	Integral non-linearity error	INL	-3.5	-	+3.5		
	Zero point error	S_{ZERO}	-25	-	+25	mV	
	Full scale error	S_{FULL}	-25	-	+25		
Buffer amplifier output impedance		R_O	-	5	15	Ω	-
Pull-up I/O internal resistance value (Note 5)		R_{up}	12.5	25	37.5	kΩ	Input voltage = 0V (The resistance value has input voltage dependence)

(Note 4) Under the condition that CH1 to CH8 are set to maximum current
(Note 5) The specification is applied to pin 5 (REVERSE) and pin 6 (RESET)

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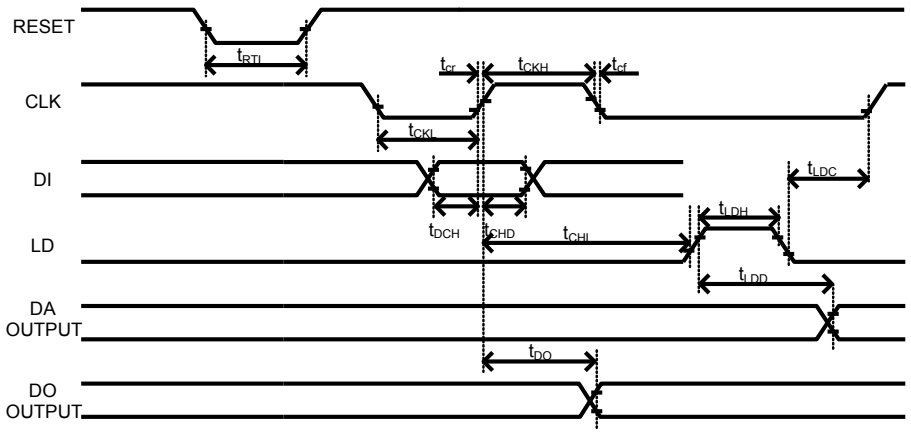
Timing Characteristics(Unless otherwise specified, V_{CC}=5V, V_{refH}=5V, V_{refL}=0V, T_A=25°C)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		The voltage levels of the measured time points are 20% or 80% of V_{CC}.
Reset L pulse width	t_{RTL}	50	-	-	ns	-
Clock L pulse width	t_{CKL}	50	-	-		-
Clock H pulse width	t_{CKH}	50	-	-		-
Clock rise time	t_{cr}	-	-	50		-
Clock fall time	t_{cf}	-	-	50		-
Data setup time	t_{DCH}	20	-	-		-
Data hold time	t_{CHD}	40	-	-		-
Load setup time	t_{CHL}	50	-	-		-
Load hold time	t_{LDC}	50	-	-		-
Load H pulse width	t_{LDH}	50	-	-		-
Data output delay time	t_{DO}	-	-	90		C_L=100pF
D/A output settling time	t_{LDD}	-	7	20	μs	C_L≤100pF(Note 6), V_O: 0.5V↔4.5V The time interval from the start time to change an output voltage to the time at which the output voltage reaches to its final value within 1/2 LSB.

(Note 6) A capacitor should be placed between the analog output and ground in order to eliminate noise.
A capacitance up to 100pF is recommended (including the capacitance of the wire).



Applicational information

LD input

The LD input is a level trigger signal. When LD=H, an internal shift register value is loaded into a latch. It doesn't have to be cared whether CLK is H or L when LD changes to H. However CLK must not be changed while LD is H. The shift register values pass through the latches if LD=H and CLK is toggled.

Power-on operation

The BU2505FV and the BU2506FV does not have a power-on reset function. Therefore, after power-on, data in the internal registers are unknown. When RESET changes from H to L, all latch outputs turn into L, although the shift registers are not reset.

Pull-down resister

Pin 5 and pin 6 are pulled up internally. If putting the external pull-down resister on them, the recommended value is less than 1kΩ.

Truth Table

	L	H
Pin 5: RESET	Reset	Normal
Pin 6: REVERSE	MSB first	LSB first

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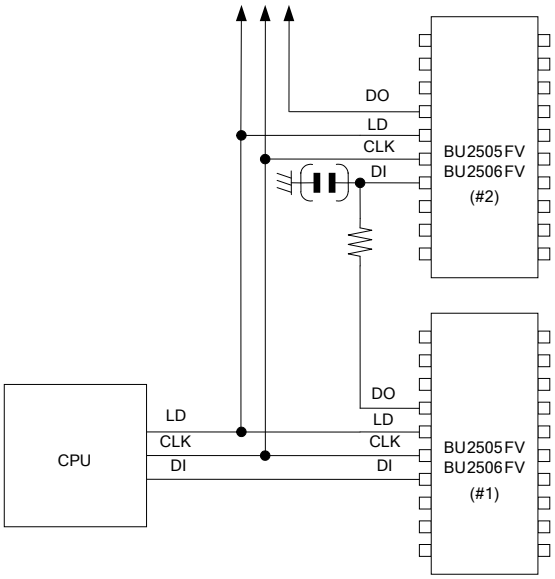
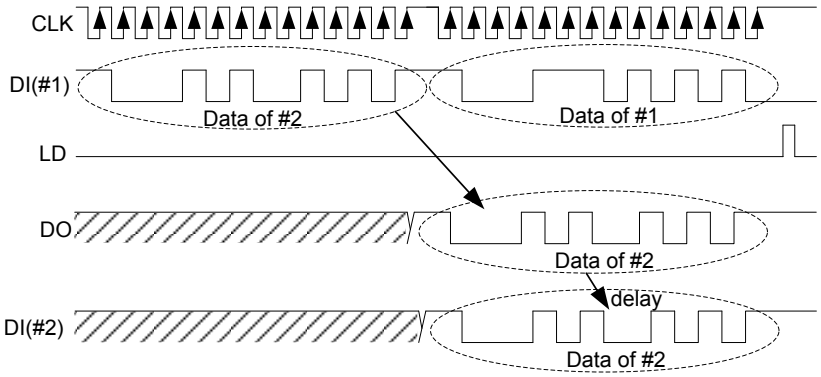
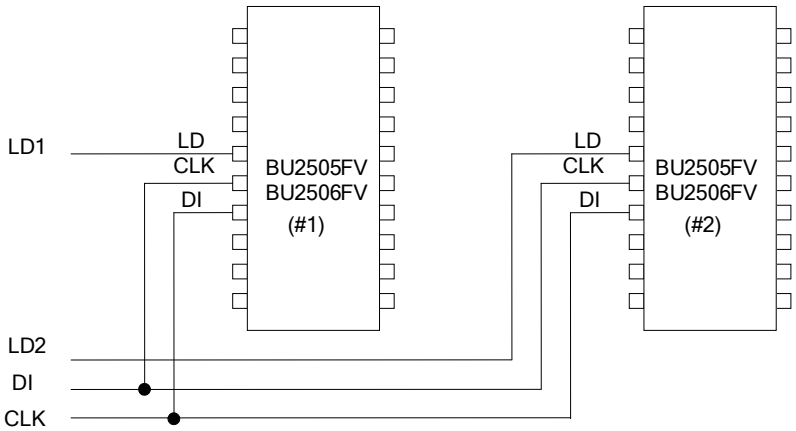
Cascade Connection

A data output terminal for cascade connection (DO) is available for reducing the number of ports of a CPU if more channels are needed. The DO terminal can be connected to a data input terminal (DI) of another IC.
However, DO signal transitions (of the IC #1 in the figure below) are triggered by the rising edge of the CLK signal. Also, DI signal transitions of another IC (#2) should follow the restriction of the data hold time. Therefore, some amount of the delay time is needed from DO of the IC #1 to DI of the IC #2. The delay time can be made with a circuit with a resister and a capacitor.
Also in some cases, a CLK signal frequency has to be decreased to ensure a margin of the data setup time.





If extra CPU ports are available, it is recommended to connect independent LD signals to each IC.
In this case, more ports of the CPU are needed for the LD signals, but the restrictions described above in the explanation of the cascade connection don't have to be considered.



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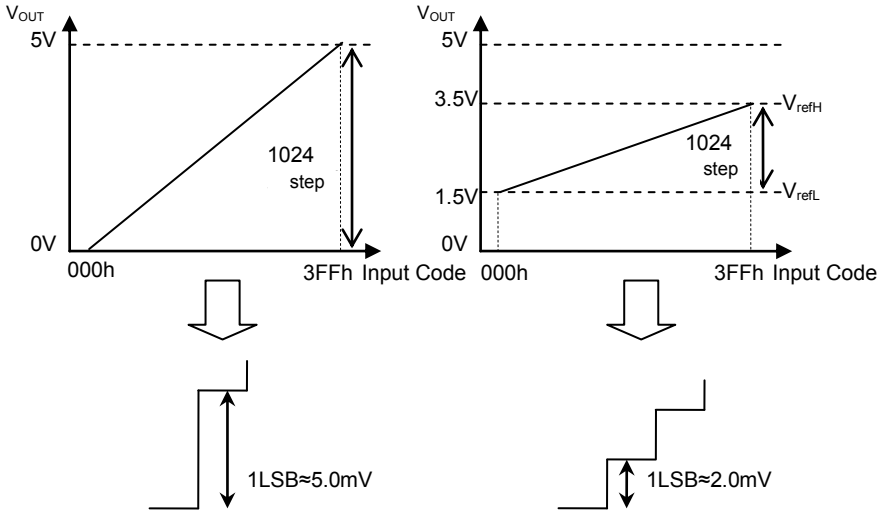
D/A Converter Variable Output Range Function

BU2505FV and BU2506FV have terminals with which the upper and lower limits of the output voltage range can be changed separately. The upper limit of the output voltage range is set with the V_{refH} terminal and the lower limit is set with V_{refL} terminal. In general usage, the V_{refH} terminal is connected to the VCC terminal and the V_{refL} terminal is connected to the GND terminal. When the power supply voltage on the VCC terminal is 5V, 1LSB is almost 5mV. In other cases, it is possible to achieve a finer resolution. For example, if V_{refH} = 3.5V and V_{refL} = 1.5V, then 1LSB is almost 2mV.



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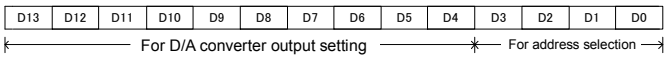
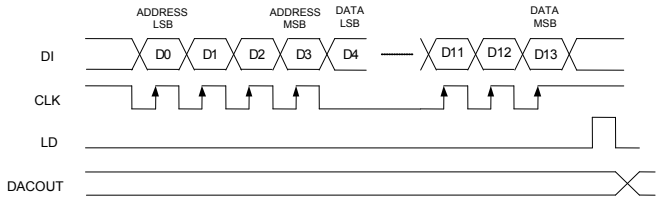
Command Transmission

1) REVERSE = open (or V_{CC} short-circuit) setting(Note 7)

(1) Data format



(2) Data timing diagram

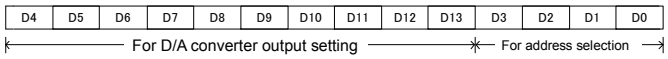


D3	D2	D1	D0	Address Selection
0	0	0	0	n/a
0	0	0	1	AO1
0	0	1	0	AO2
0	0	1	1	AO3
0	1	0	0	AO4
0	1	0	1	AO5
0	1	1	0	AO6
0	1	1	1	AO7
1	0	0	0	AO8
1	0	0	1	AO9 (Note 8)
1	0	1	0	AO10 (Note 8)
1	0	1	1	n/a
1	1	0	0	n/a
1	1	0	1	n/a
1	1	1	0	n/a
1	1	1	1	n/a

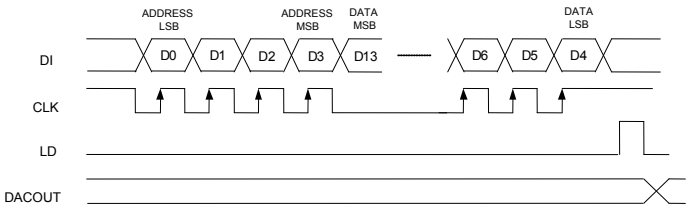
D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D/A output (V_{refH}=V_{DD}, V_{refL}=V_{SS})
0	0	0	0	0	0	0	0	0	0	V_{refL}
0	0	0	0	0	0	0	0	0	1	$(V_{refH}-V_{refL})/1024\times1+V_{refL}$
0	0	0	0	0	0	0	0	1	0	$(V_{refH}-V_{refL})/1024\times2+V_{refL}$
0	0	0	0	0	0	0	0	1	1	$(V_{refH}-V_{refL})/1024\times3+V_{refL}$
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	0	$(V_{refH}-V_{refL})/1024\times1022+V_{refL}$
1	1	1	1	1	1	1	1	1	1	$(V_{refH}-V_{refL})/1024\times1023+V_{refL}$

2) REVERSE = L setting(Note 7)

(1) Data format



(2) Data timing diagram



D3	D2	D1	D0	Address selection
0	0	0	0	n/a
0	0	0	1	AO1
0	0	1	0	AO2
0	0	1	1	AO3
0	1	0	0	AO4
0	1	0	1	AO5
0	1	1	0	AO6
0	1	1	1	AO7
1	0	0	0	AO8
1	0	0	1	AO9 (Note 8)
1	0	1	0	AO10 (Note 8)
1	0	1	1	n/a
1	1	0	0	n/a
1	1	0	1	n/a
1	1	1	0	n/a
1	1	1	1	n/a

D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D/A output (V_{refH}=V_{DD}, V_{refL}=V_{SS})
0	0	0	0	0	0	0	0	0	0	VrefL
1	0	0	0	0	0	0	0	0	0	$(V_{refH}-V_{refL})/1024\times1+V_{refL}$
0	1	0	0	0	0	0	0	0	0	$(V_{refH}-V_{refL})/1024\times2+V_{refL}$
1	1	0	0	0	0	0	0	0	0	$(V_{refH}-V_{refL})/1024\times3+V_{refL}$
:	:	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1	1	$(V_{refH}-V_{refL})/1024\times1022+V_{refL}$
1	1	1	1	1	1	1	1	1	1	$(V_{refH}-V_{refL})/1024\times1023+V_{refL}$

(Note 7) It is selectable for the IC to receive 10bit data in LSB first order or MSB first order, depending on the condition of the REVERSE terminal. If the REVERSE terminal is set to the GND voltage, it is MSB first

(Note 8) In the BU2506FV, this channel is for testing. Therefore, it must not be selected.

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Typical Performance Curves (reference data)

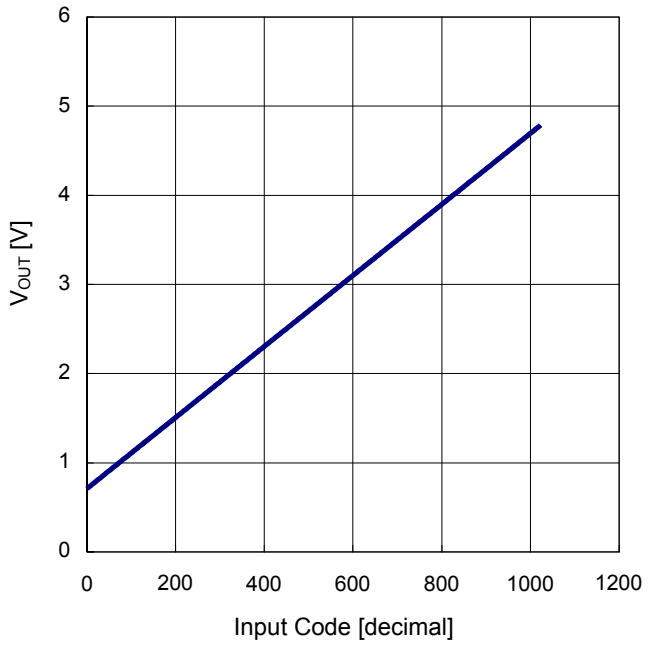

Figure 1. V_{OUT} vs Input Code
(Output voltage linearity, T_A=-30°C)

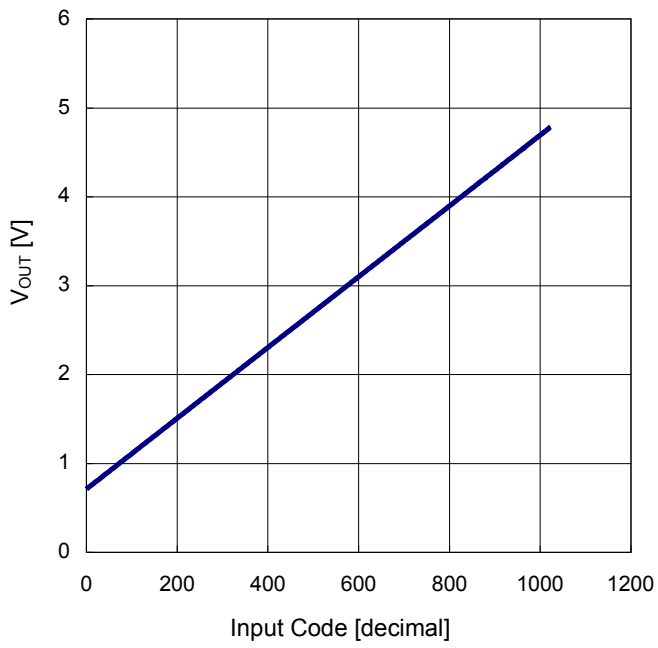

Figure 2. V_{OUT} vs Input Code
(Output voltage linearity, T_A=+25°C)

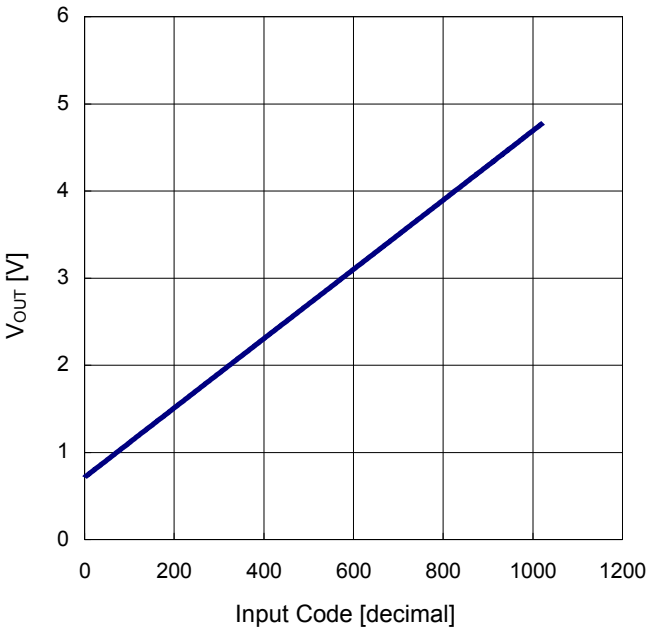

Figure 3. V_{OUT} vs Input Code
(Output voltage linearity, T_A=+85°C)

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Typical Performance Curves(reference data) - continued

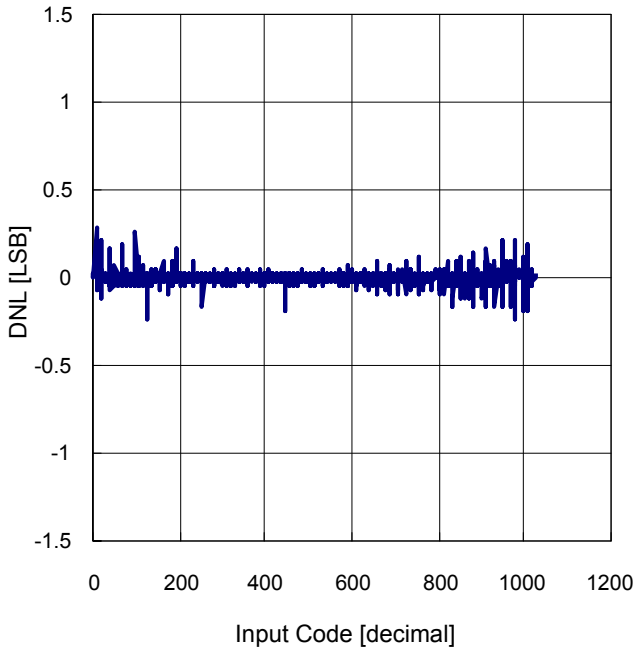

Figure 4. DNL vs Input Code
(Differential linearity error, T_A=-30°C)

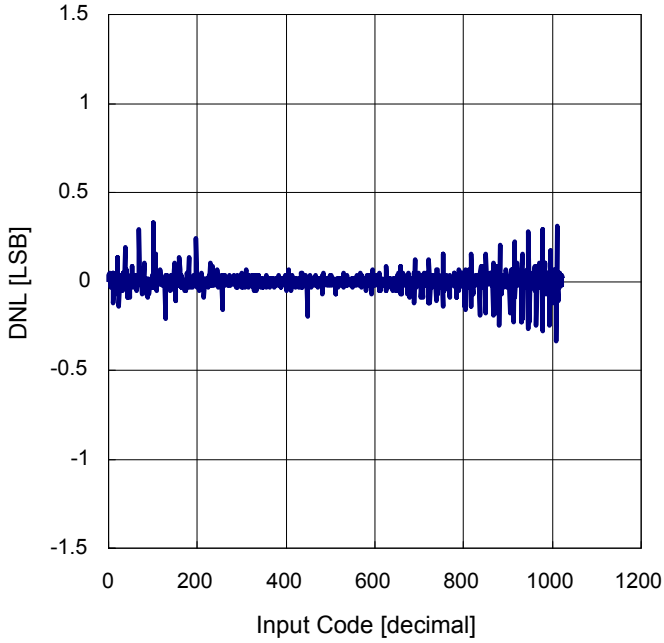

Figure 5. DNL vs Input Code
(Differential linearity error, T_A=+25°C)

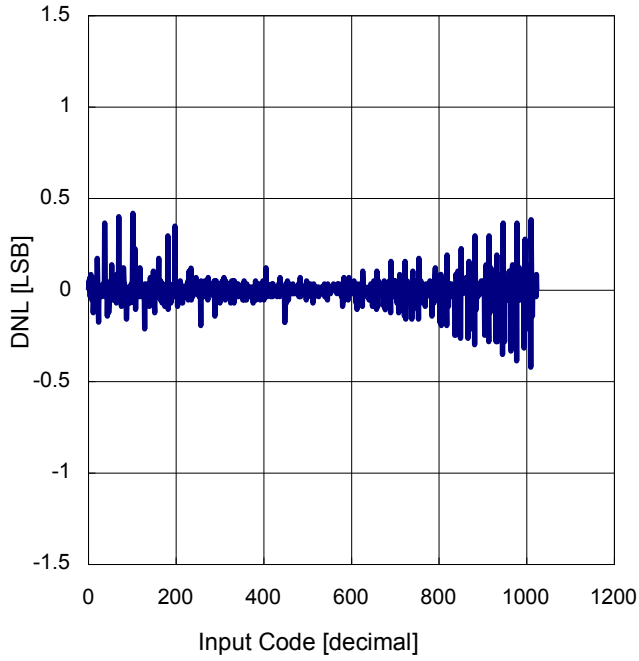

Figure 6. DNL vs Input Code
(Differential linearity error, T_A=+85°C)

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Typical Performance Curves(reference data) - continued

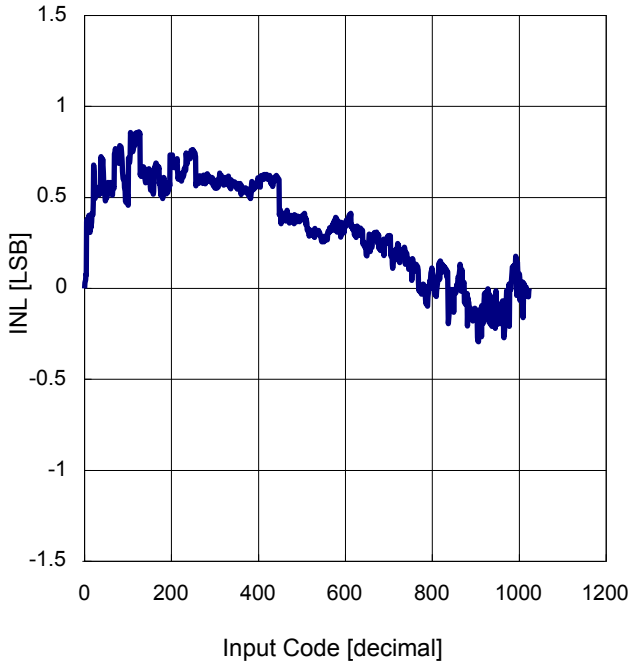

Figure 7. INL vs Input Code
(Integral linearity error, T_A=-30°C)

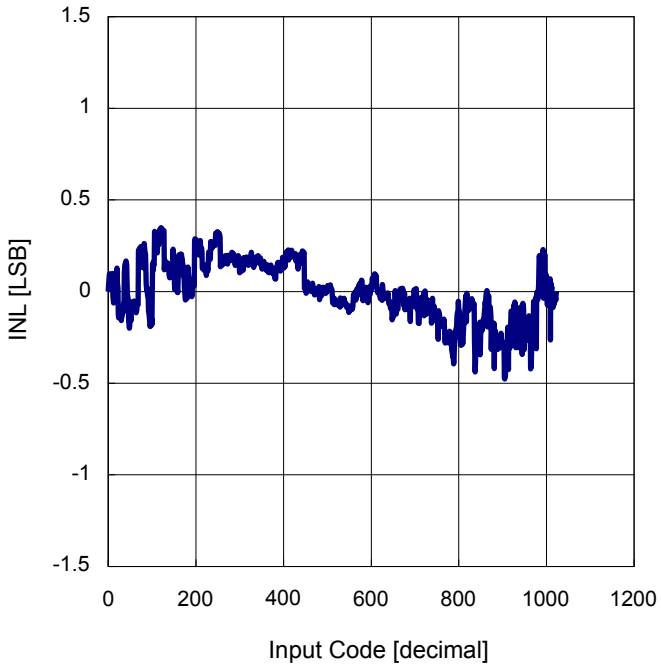

Figure 8. INL vs Input Code
(Integral linearity error, T_A=+25°C)

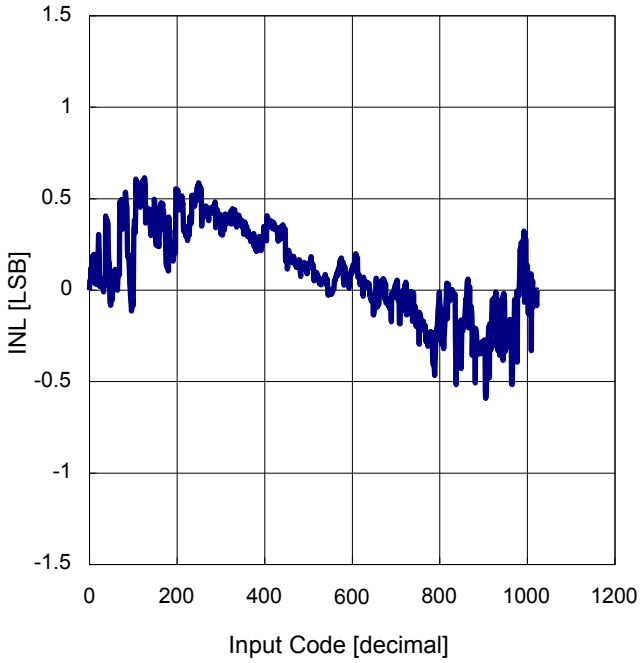

Figure 9. INL vs Input Code
(Integral linearity error, T_A=+85°C)

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Typical Performance Curves(reference data) - continued

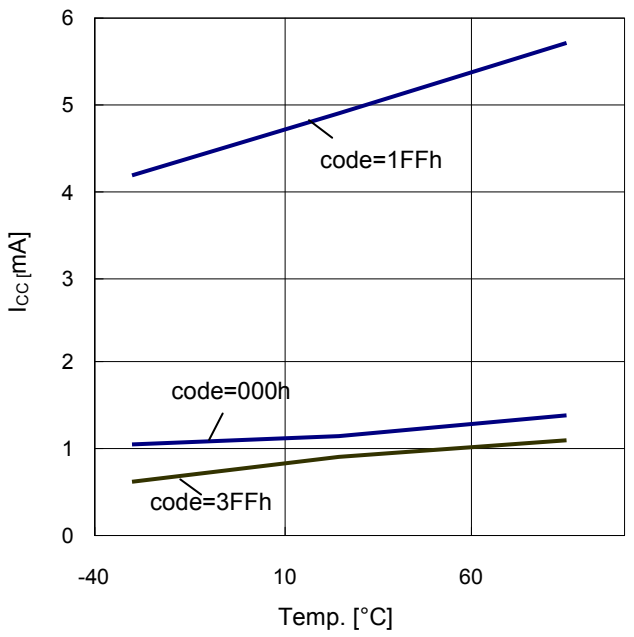

Figure 10. I_{CC} vs Temp
(Circuit current temperature characteristic)

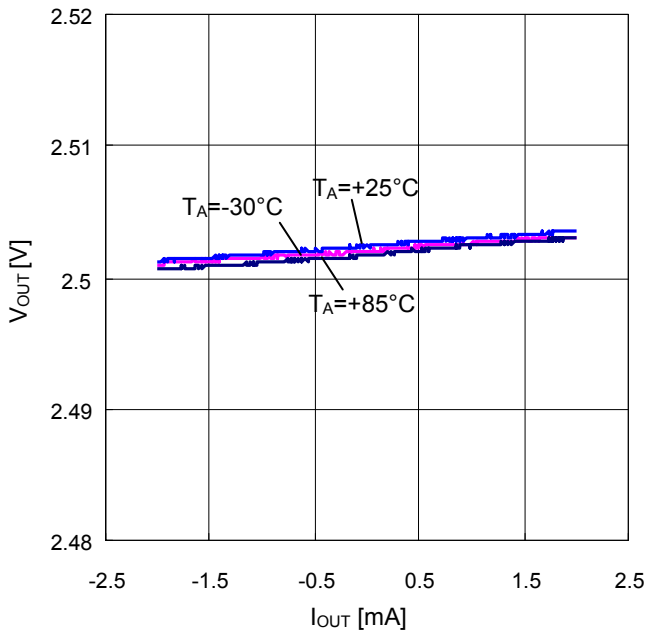

Figure 11. V_{OUT} vs I_{OUT}
(Output load fluctuation characteristic (input code: 1FFh))

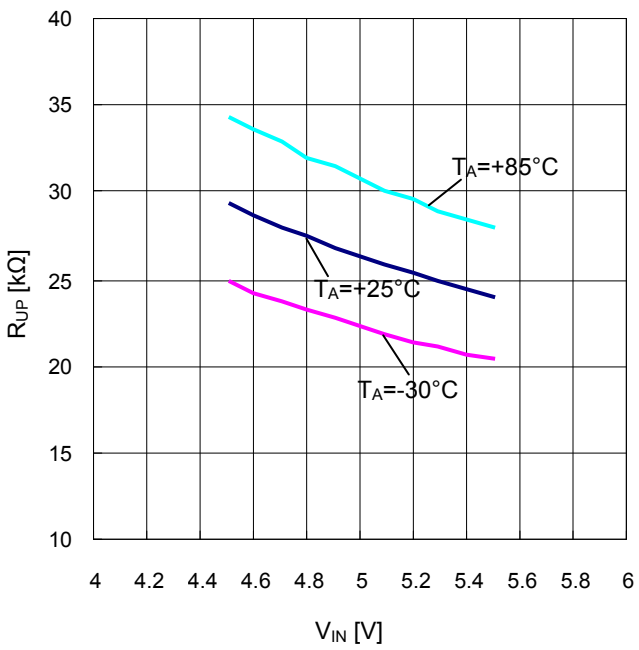

Figure 12. R_{UP} vs V_{IN}
(Built-in pull-up resistance characteristic)

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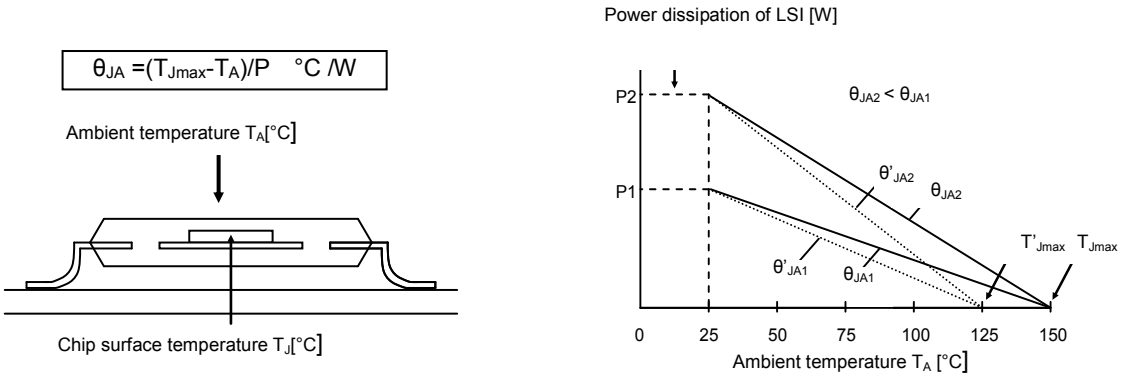
Power Dissipation

Power dissipation(total loss) indicates the power that can be consumed by IC at T_A=25°C (normal temperature).IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol θ_{JA}°C/W. The temperature of IC inside the package can be estimated by this thermal resistance. Figure 13(a) shows the model of thermal resistance of the package. Thermal resistance θ_{JA}, ambient temperature T_A, junction temperature T_{Jmax}, and power dissipation P_D can be calculated by the equation below

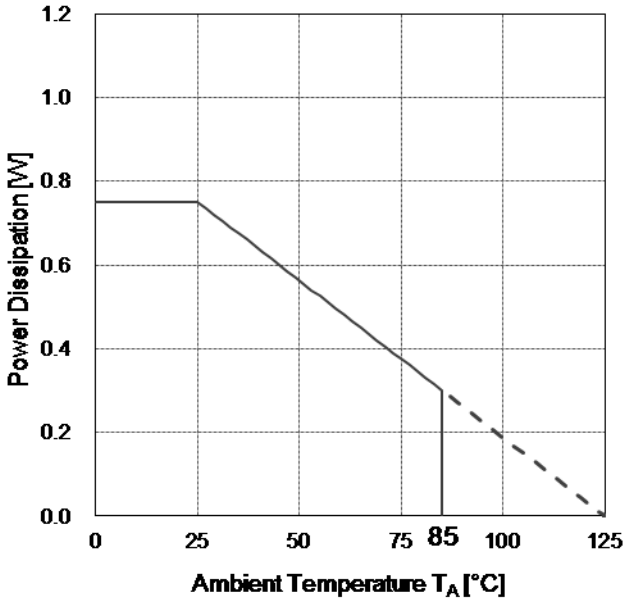
$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad °C/W$$

Derating curve in Figure 13(b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{JA}. Thermal resistance θ_{JA} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 14(a) show a derating curve for an example of BU2505FV and BU2506FV.



(a) Thermal Resistance (b) Derating Curve

Figure 13. Thermal resistance and derating



(a) BU2505FV・BU2506FV

Derating curve	UNIT
7.5	mW/°C

When using the IC above T_A=25°C, subtract the value above per °C
Mounted on a FR4 glass epoxy board 70mm x 70mm x 1.6mm (cooper foil area less than 3%).

Figure 14. Derating curve

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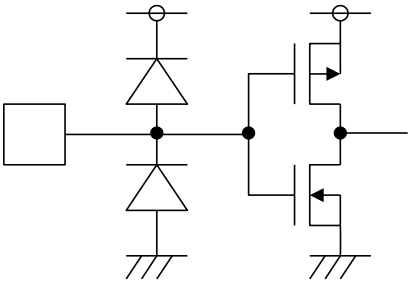
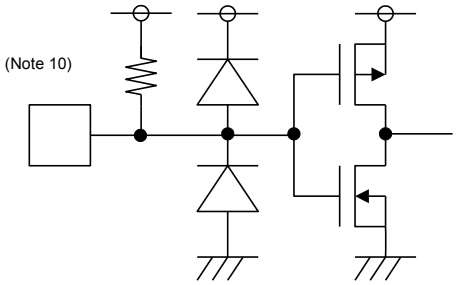
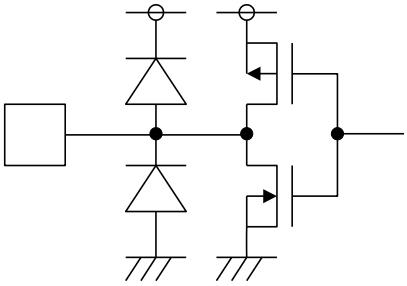
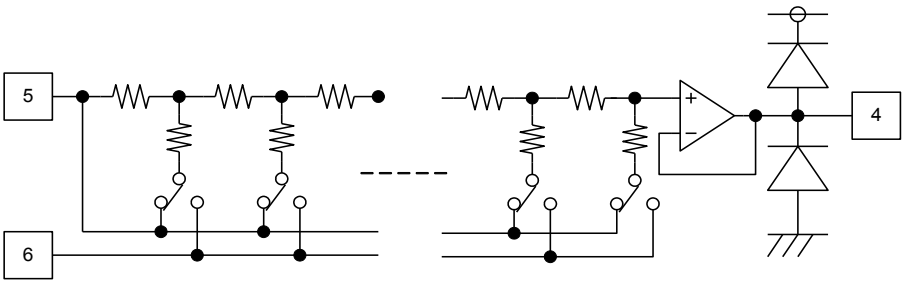
I/O Equivalent Circuit

No.(Note 9)	Equivalent circuit
1	
2	
3	
4 · 5 · 6	

(Note 9) Please refer to the equivalent circuit number in the Pin Descriptions table.
(Note 10) 25kΩ at V_{CC} = 5.0V (changes according to the applied voltage)

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

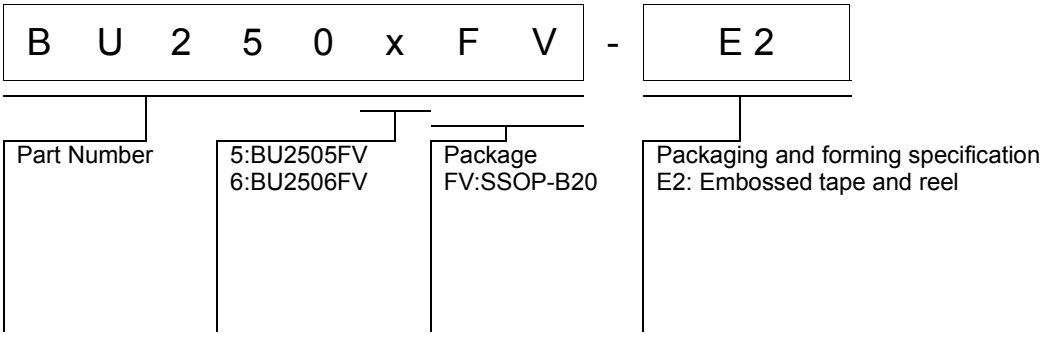
13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

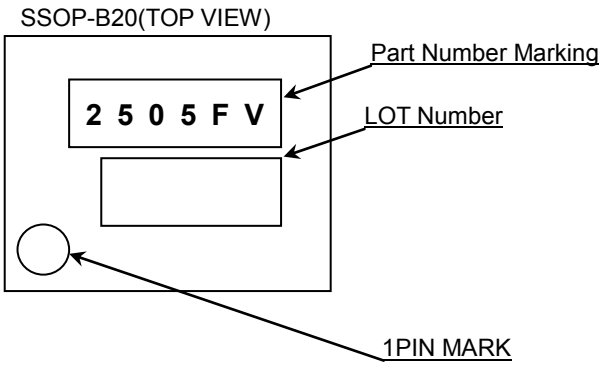
14. Area of Safe Operation (ASO)

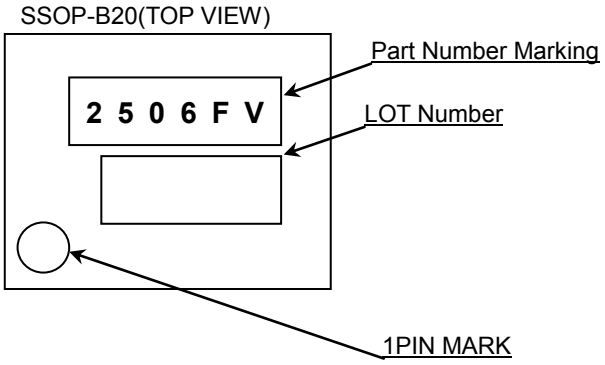
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

Ordering Information



Marking Diagrams





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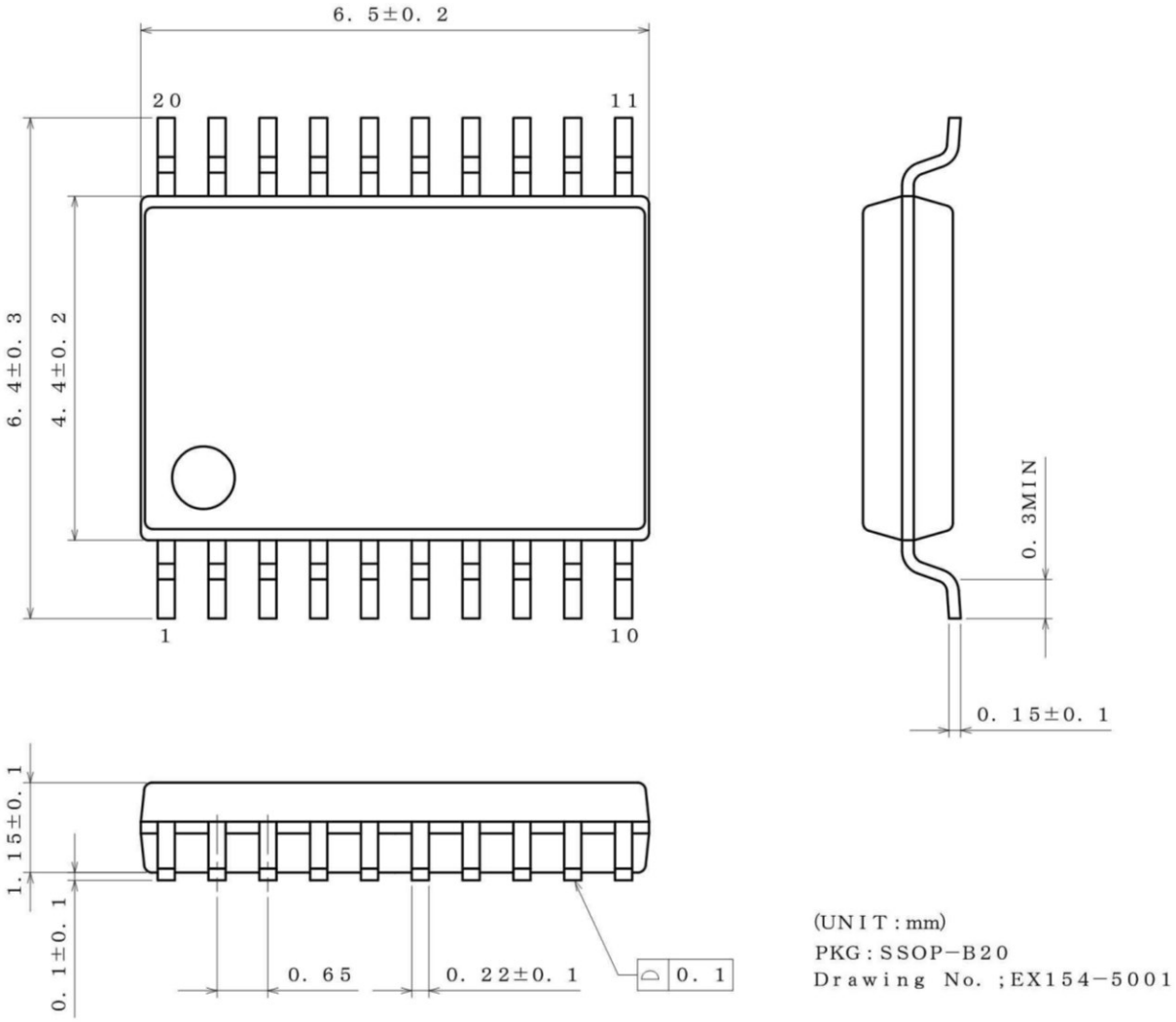
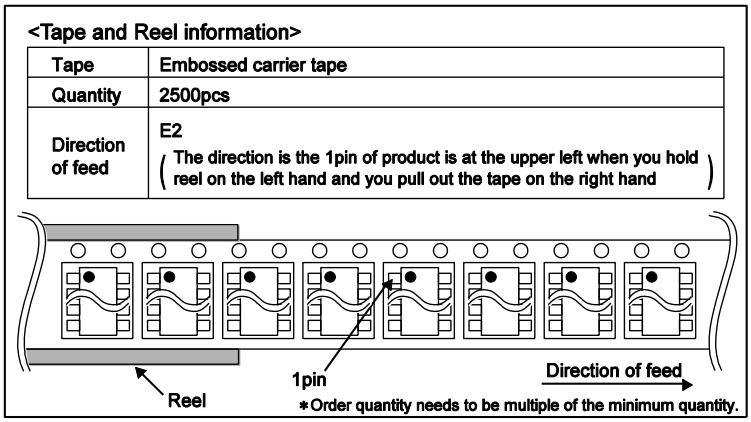
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B20





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Revision History

Date	Revision	Changes
11.Dec.2015	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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