

CD4016B Types

CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

■ CD4016B Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch on or off.

The CD4016 "B" Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

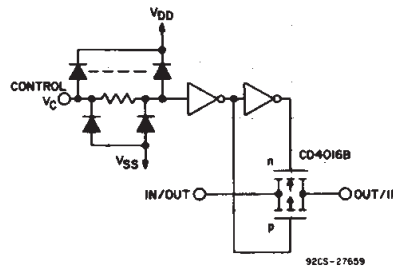
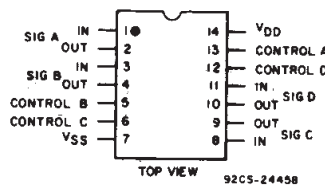
Features:

- 20-V digital or ± 10 -V peak-to-peak switching
- 280- Ω typical on-state resistance for 15-V operation
- Switch on-state resistance matched to within 10 Ω typ. over 15-V signal-input range
- High on/off output-voltage ratio: 65 dB typ. @ $f_{is} = 10$ kHz, $R_L = 10$ k Ω
- High degree of linearity: <0.5% distortion typ. @ $f_{is} = 1$ kHz, $V_{is} = 5$ V_{p-p}, $V_{DD} - V_{SS} \geq 10$ V, $R_L = 10$ k Ω
- Extremely low off-state leakage resulting in very low offset current and high effective off-state resistance: 100 pA typ. @ $V_{DD} - V_{SS} = 18$ V, $T_A = 25^\circ\text{C}$
- Extremely high control input impedance (control circuit isolated from signal circuit): 1012 Ω typ.
- Low crosstalk between switches: -50 dB typ. @ $f_{is} = 0.9$ MHz, $R_L = 1$ k Ω
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- Maximum control input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V at 25 $^\circ\text{C}$
- 5-V, 10-V, and 15-V parametric ratings

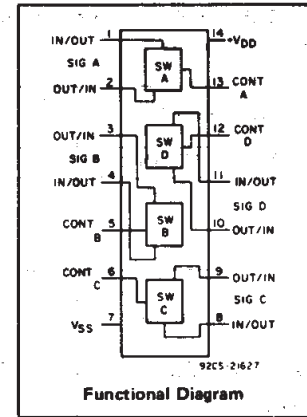
Applications:

- Analog signal switching/multiplexing
 - Signal gating ■ Modulator
 - Squelch control ■ Demodulator
 - Chopper ■ Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

Terminal Assignment



Schematic diagram - 1 of 4 identical sections.



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For $T_A =$ Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE RANGE, (V_{DD}) Voltages referenced to V_{SS} Terminal) -0.5V to +20V
- INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5$ V
- DC INPUT CURRENT, ANY ONE INPUT ± 10 mA
- POWER DISSIPATION PER PACKAGE (P_D):
 - For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW
 - For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 - FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
- OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$
- STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$
- LEAD TEMPERATURE (DURING SOLDERING):
 - At distance $1/16 \pm 1/32$ inch (1.59 \pm 0.79mm) from case for 10s max $+265^\circ\text{C}$

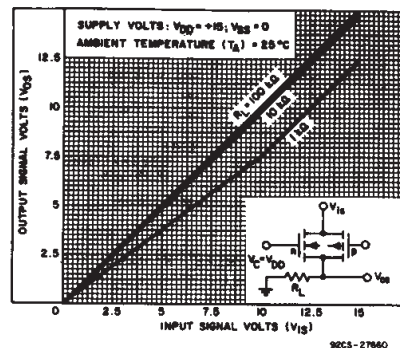


Fig. 1— Typ. on-state characteristics for 1 of 4 switches with $V_{DD} = +15$ V, $V_{SS} = 0$ V.

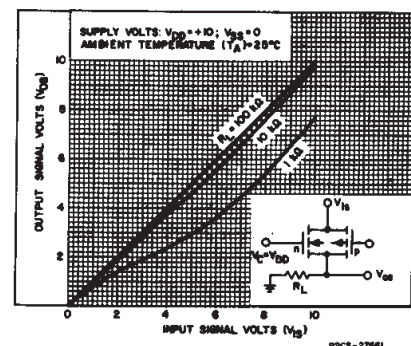


Fig. 2— Typ. on-state characteristics for 1 of 4 switches with $V_{DD} = +10$ V, $V_{SS} = 0$ V.

CD4016B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
		V _{IN} (V)	V _{DD} (V)					+25		
				-55	-40	+85	+125	Typ.		Max.
Quiescent Device Current, I _{DD}		0,5	5	0,25	0,25	7,5	7,5	0,01	0,25	μA
		0,10	10	0,5	0,5	15	15	0,01	0,5	
		0,15	15	1	1	30	30	0,01	1	
		0,20	20	5	5	150	150	0,02	5	
Signal Inputs (V _{is}) and Output (V _{os})										
On-State Resistance, r _{on} Max.	V _C = V _{DD} R _L = 10 kΩ Returned to V _{DD} - V _{SS} 2	V _{is} = V _{DD} or V _{SS}	10	600	610	840	960	-	660	Ω
		V _{is} = 4.75 to 5.75 V	10	1870	1900	2380	2600	-	2000	
Δ On-State Resistance Between Any 2 Switches, Δr _{on}	R _L = 10 kΩ, V _C = V _{DD}	V _{is} = V _{DD} or V _{SS}	15	360	370	520	600	-	400	Ω
		V _{is} = 7.25 to 7.75 V	15	775	790	1080	1230	-	850	
			5	-	-	-	-	15	-	
Total Harmonic Distortion, THD	V _C = V _{DD} = 5 V, V _{SS} = -5 V, V _{is} (p-p) = 5 V (Sine wave centered on 0 V) R _L = 10 kΩ, f _{is} = 1 kHz sine wave		-	-	-	-	0.4	-	%	
-3dB Cutoff Frequency (Switch on)	V _C = V _{DD} = 5 V, V _{SS} = -5 V, V _{is} (p-p) = 5 V (Sine wave centered on 0 V) R _L = 1 kΩ,		-	-	-	-	40	-	MHz	
-50dB Feed-through Frequency (Switch off)	V _C = V _{SS} = -5 V, V _{is} (p-p) = 5 V (Sine wave centered on 0 V) R _L = 1 kΩ		-	-	-	-	1.25	-	MHz	
Input/Output Leakage Current (Switch off) I _{is} Max.	V _C = 0 V V _{is} = 18 V, V _{os} = 0 V; V _{is} = 0 V, V _{os} = 18 V	18	±0.1	±0.1	±1	±1	10 ⁻⁴	±0.1	μA	
-50 dB Crosstalk Frequency	V _C (A) = V _{DD} = +5 V, V _C (B) = V _{SS} = -5 V, V _{is} (A) = 5 V p-p, 50 Ω source R _L = 1 kΩ		-	-	-	-	0.9	-	MHz	
Propagation Delay (Signal Input to Signal Output) t _{pd}	R _L = 200 kΩ V _C = V _{DD} , V _{SS} = GND, C _L = 50 pF V _{is} = Square Wave 0 to V _{DD} t _r , t _f = 20 ns	5	-	-	-	-	40	100	ns	
		10	-	-	-	-	20	40		
		15	-	-	-	-	15	30		
Capacitance: Input, C _{is} Output, C _{os} Feedthrough, C _{ios}	V _{DD} = +5 V V _C = V _{SS} = -5 V		-	-	-	-	4	-	pF	
			-	-	-	-	4	-		
			-	-	-	-	0.2	-		

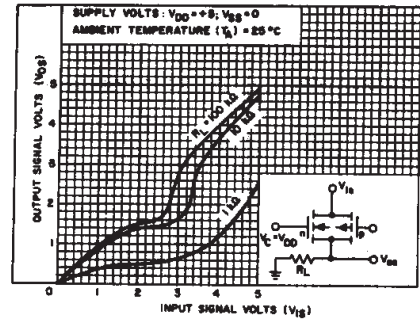


Fig. 3—Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = 0 V.

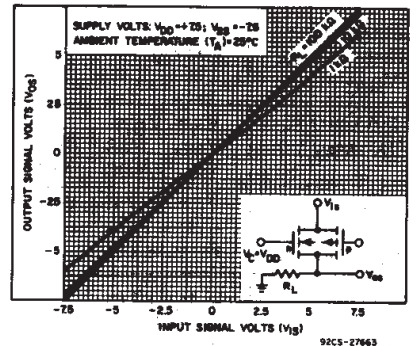


Fig. 4—Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +7.5 V, V_{SS} = -7.5 V.

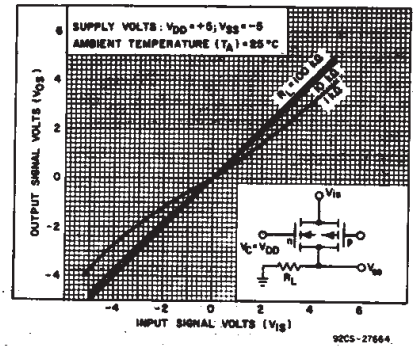


Fig. 5—Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

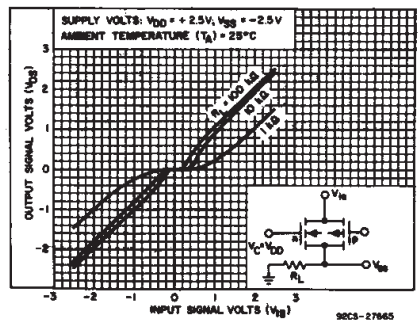


Fig. 6—Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +2.5 V, V_{SS} = -2.5 V.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4016B Types

ELECTRICAL CHARACTERISTICS (cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
		V _{DD} (V)		+25					
		-55	-40	+85	+125	Typ.	Max.		
Control (V_C)									
Control Input Low Voltage, V _{ILC} (Max.)	I _{is} < 10 μA V _{is} = V _{SS} , V _{OS} = V _{DD} and V _{is} = V _{DD} , V _{OS} = V _{SS}	5, 10, 15	0.9	0.9	0.4	0.4	-	0.7	V
Control Input High Voltage, V _{IHC}	See Fig. 10	5, 10, 15	3.5 (Min.) 7 (Min.) 11 (Min.)				-	-	V
Input Current, I _{IN} (Max.)	V _{is} ≤ V _{DD} V _{DD} - V _{SS} = 18 V V _{CC} ≤ V _{DD} - V _{SS}	18	±0.1	±0.1	±1	±1	±10 ⁻⁵	±0.1	μA
Crosstalk (Control Input to Signal Output)	V _C = 10 V (Sq. Wave) t _r , t _f = 20 ns R _L = 10 kΩ	10	-	-	-	-	50	-	mV
Turn-On Propagation Delay	t _r , t _f = 20 ns C _L = 50 pF R _L = 1 kΩ	5, 10, 15	-	-	-	-	35, 20, 15	70, 40, 30	ns
Maximum Control Input Repetition Rate	V _{is} = V _{DD} , V _{SS} = GND, R _L = 1 kΩ to gnd, C _L = 50 pF, V _C = 10 V (Square wave centered on 5 V) t _r , t _f = 20 ns, V _{os} = ½ V _{os} @ 1 kHz	10	-	-	-	-	10	-	MHz
Input Capacitance, C _{IN}			-	-	-	-	5	7.5	μF

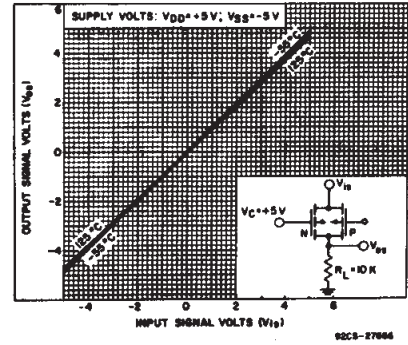


Fig. 7—Typ. on-state characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

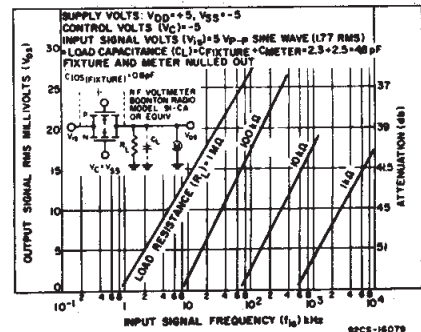


Fig. 8—Typ. feedthrough vs. frequency—switch off.

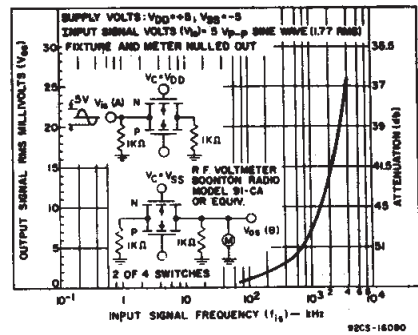


Fig. 9—Typical crosstalk between switch circuits in the same package.

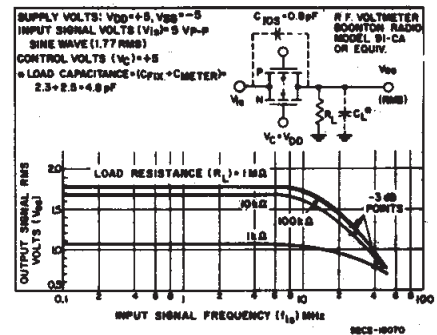


Fig. 11—Typical frequency response—switch on.

V _{DD} (V)	V _{is} (V)	Switch Input I _{is} (mA)						Switch Output V _{os} (V)	
		-55°C	-40°C	25°C*	25°C▲	+85°C	+125°C	Min.	Max.
5	0	0.25	0.2	0.2	0.16	0.12	0.14	-	0.4
5	5	-0.25	-0.2	-0.2	-0.16	-0.12	-0.14	4.6	-
10	0	0.62	0.5	0.5	0.4	0.3	0.35	-	0.5
10	10	-0.62	-0.5	-0.5	-0.4	-0.3	-0.35	9.5	-
15	0	1.8	1.4	1.5	1.2	1	1.1	-	1.5
15	15	-1.8	-1.4	-1.5	-1.2	-1	-1.1	13.5	-

* Plastic package

▲ Ceramic package

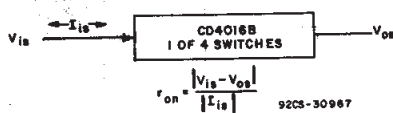


Fig. 10—Determination of r_{on} as a test condition for control input high voltage (V_{IHC}) specification.

CD4016B Types

TYPICAL ON-STATE RESISTANCE CHARACTERISTICS, $T_A = 25^\circ\text{C}$

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			$R_L = 1k\Omega$		$R_L = 10k\Omega$		$R_L = 100k\Omega$	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)	VALUE (Ω)	V_{IS} (V)
r_{on}	+15	0	200	+15	200	+15	180	+15
r_{on} (max.)	+15	0	200	0	200	0	200	0
r_{on}	+10	0	290	+10	250	+10	240	+10
r_{on} (max.)	+10	0	290	0	250	0	300	0
r_{on}	+5	0	860	+5	470	+5	450	+5
r_{on} (max.)	+5	0	600	0	580	0	800	0
r_{on}	+7.5	-7.5	200	+7.5	200	+7.5	180	+7.5
r_{on} (max.)	+7.5	-7.5	290	± 0.25	280	± 25	400	± 0.25
r_{on}	+5	-5	260	+5	250	+5	240	+5
r_{on} (max.)	+5	-5	310	-5	250	-5	240	-5
r_{on}	+2.5	-2.5	590	+2.5	450	+2.5	490	+2.5
r_{on} (max.)	+2.5	-2.5	720	-2.5	520	-2.5	520	-2.5
r_{on}	+2.5	-2.5	232k	± 0.25	300k	± 0.25	870k	± 0.25

* Variation from perfect switch, $r_{on} = 0 \Omega$.

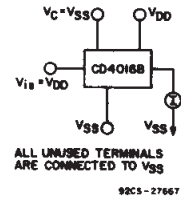


Fig. 12 – Off-state switch input or output leakage current test circuit.

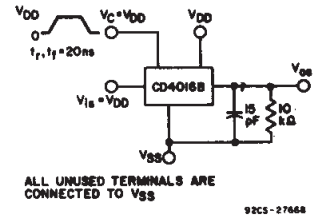
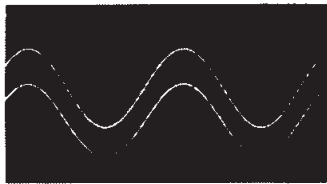


Fig. 13 – Test circuit for square-wave response.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
 $V_{DD} = V_C = +7.5V, V_{SS} = -7.5V, R_L = 10K\Omega$
 $C_L = 15 pF$
 $f_{IS} = 1 KHz, V_{IS} = 5V p-p$
 DISTORTION = 0.2 %

92CS-27612

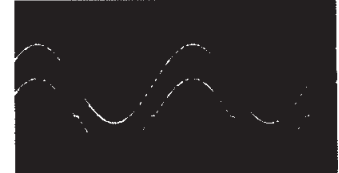
Fig. 14 – Typical sine wave response of $V_{DD} = +7.5 V, V_{SS} = -7.5 V$.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
 $V_{DD} = V_C = +5V, V_{SS} = -5V, R_L = 10K\Omega$
 $C_L = 15 pF$
 $f_{IS} = 1 KHz, V_{IS} = 5V p-p$
 DISTORTION = 0.4 %

92CS-27613

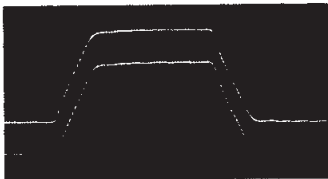
Fig. 15 – Typical sine wave response of $V_{DD} = +5 V, V_{SS} = -5 V$.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
 $V_{DD} = V_C = +2.5V, V_{SS} = -2.5V, R_L = 10K\Omega$
 $C_L = 15 pF$
 $f_{IS} = 1 KHz, V_{IS} = 5V p-p$
 DISTORTION = 3 %

92CS-27614

Fig. 16 – Typical sine wave response of $V_{DD} = +2.5 V, V_{SS} = -2.5 V$.



SCALE: X = 100 ns/DIV
 Y = 5.0 V/DIV

92CS-27615

Fig. 17 – Typical square wave response at $V_{DD} = V_C = +15 V, V_{SS} = Gnd$.



SCALE: X = 100 ns/DIV
 Y = 5.0 V/DIV

92CS-27616

Fig. 18 – Typical square wave response at $V_{DD} = V_C = +10 V, V_{SS} = Gnd$.



SCALE: X = 100 ns/DIV
 Y = 2 V/DIV

92CS-27617

Fig. 19 – Typical square wave response at $V_{DD} = V_C = +5 V, V_{SS} = Gnd$.

CD4016B Types

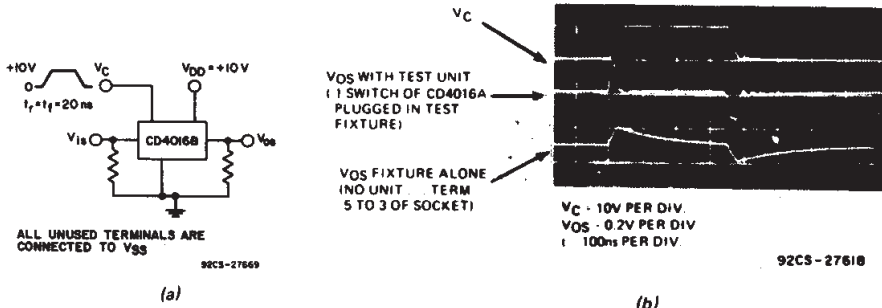


Fig. 20 - Crosstalk-control input to signal output.

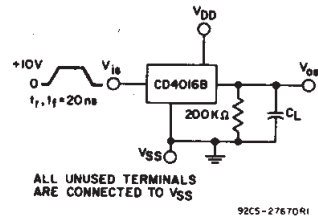


Fig. 21 - Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

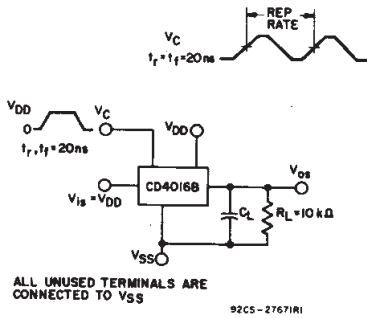


Fig. 22 - Max. control-input repetition rate.

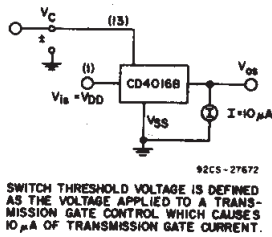


Fig. 23 - Switch threshold voltage.

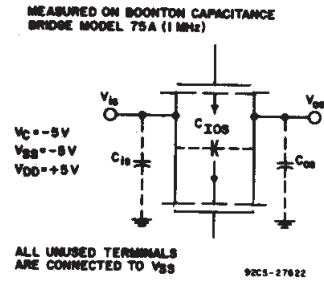


Fig. 24 - Capacitance C_{IOs} and C_{OS} .

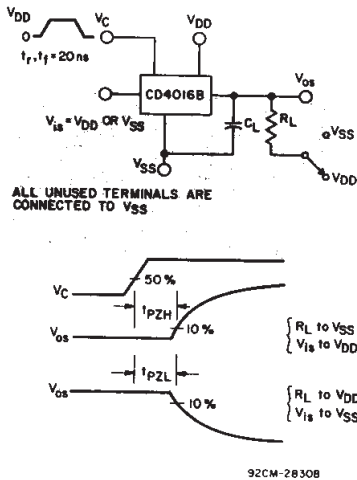
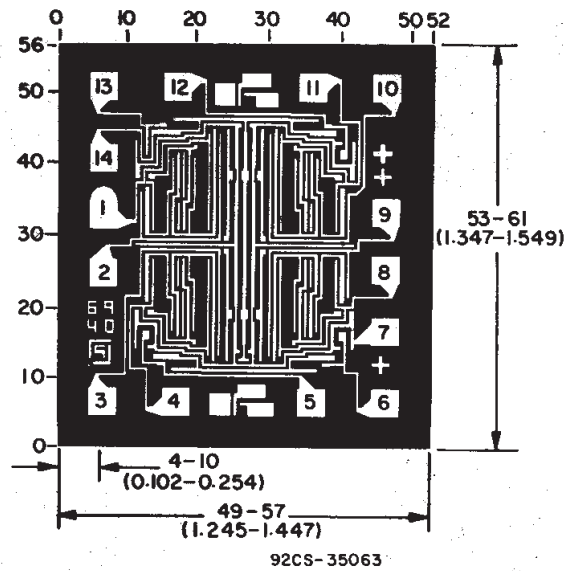


Fig. 25 - Turn-On propagation delay-control input.

Dimensions and pad layout for CD4016BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9064001CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A	Samples
CD4016BE	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD4016BE	Samples
CD4016BEE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD4016BE	Samples
CD4016BF	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD4016BF	Samples
CD4016BF3A	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A	Samples
CD4016BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016B	Samples
CD4016BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B	Samples
CD4016BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4016B, CD4016B-MIL :

- Catalog: [CD4016B](#)
- Military: [CD4016B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4016BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4016BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4016BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4016BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4016BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4016BMT	SOIC	D	14	250	210.0	185.0	35.0
CD4016BNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4016BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

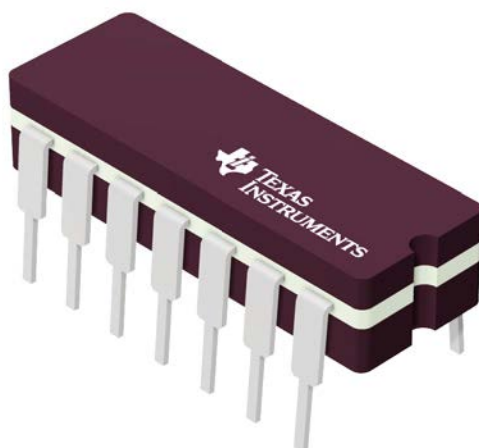
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

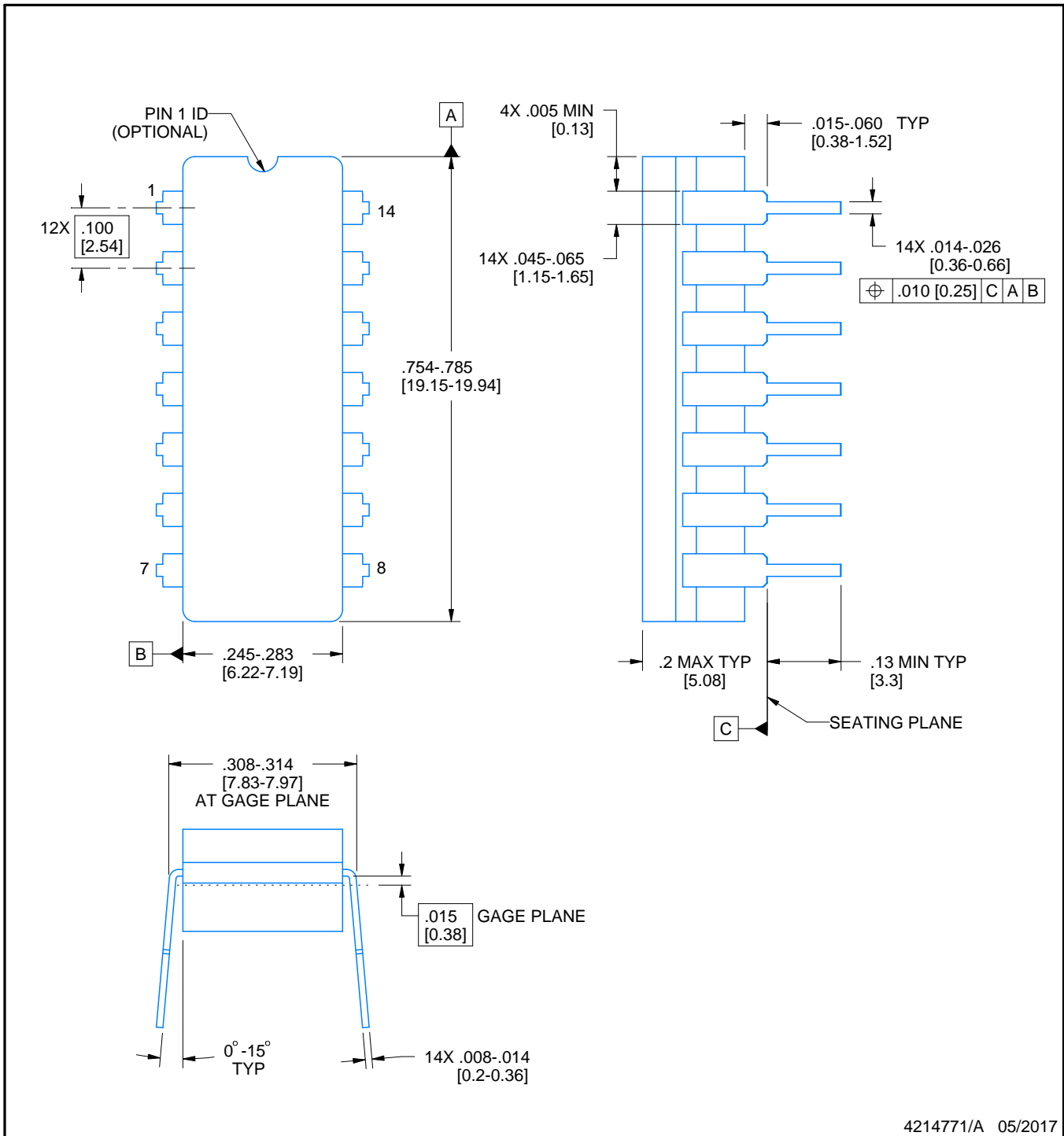
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



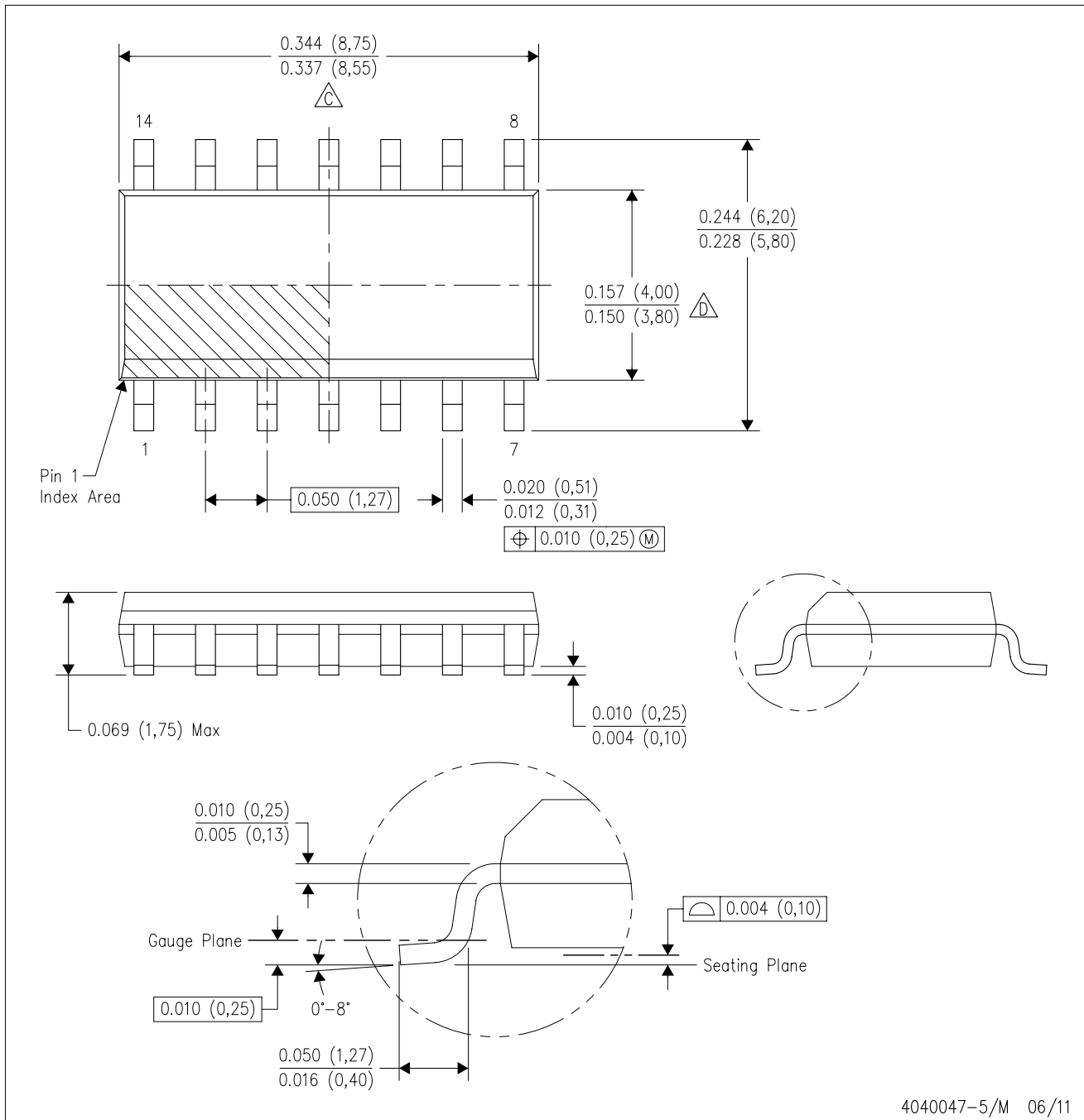
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

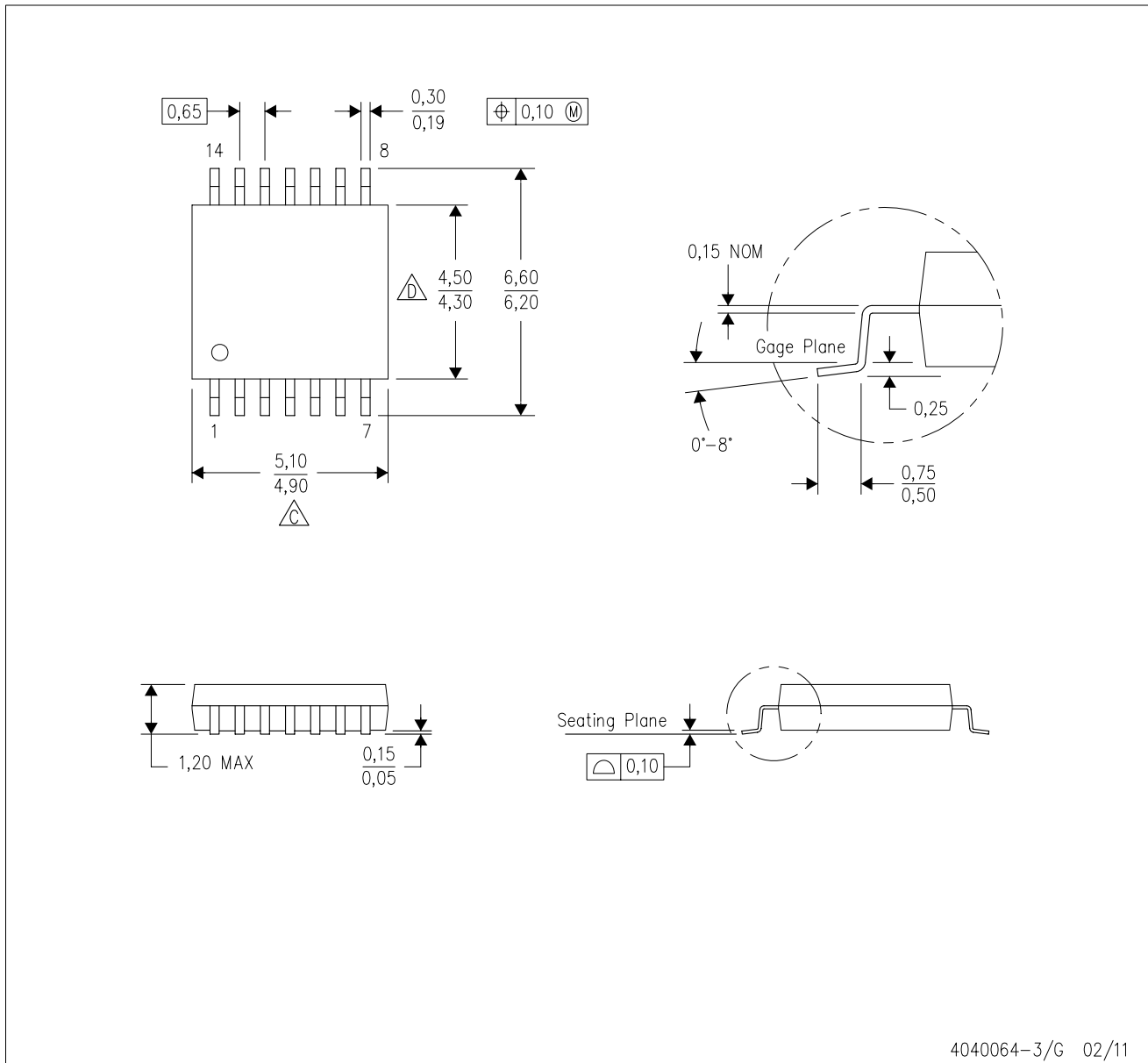
PLASTIC SMALL OUTLINE





- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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