

## CD4538BM/CD4538BC Dual Precision Monostable

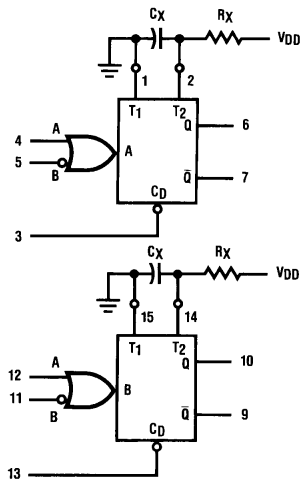
### General Description

The CD4538B is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active low and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components  $R_X$  and  $C_X$ . The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

### Features

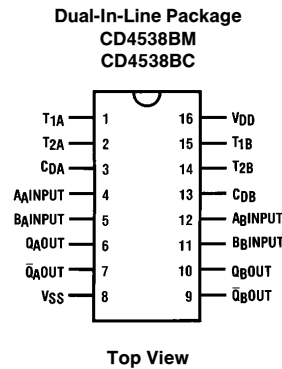
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45  $V_{CC}$  (typ.)
- Low power Fan out of 2 driving 74L or 1 driving 74LS
- New formula:  $PW_{OUT} = RC$  (PW in seconds, R in Ohms, C in Farads)
- $\pm 1.0\%$  pulse-width variation from part to part (typ.)
- Wide pulse-width range 1  $\mu s$  to  $\infty$
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current 5 nA (typ.) @ 5  $V_{DC}$
- Pin compatible to CD4528B

### Block and Connection Diagrams



$R_X$  and  $C_X$  are External Components  
 $V_{DD}$  = Pin 16  
 $V_{SS}$  = Pin 8

TL/F/6000-1



TL/F/6000-2

Order Number CD4538B

### Truth Table

Clear	Inputs		Outputs	
	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎓	⎓
H	↑	H	⎓	⎓

- H = High Level
- L = Low Level
- ↑ = Transition from Low to High
- ↓ = Transition from High to Low
- ⎓ = One High Level Pulse
- ⎓ = One Low Level Pulse
- X = Irrelevant

## Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage ( $V_{DD}$ )	-0.5 to +18 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{DD}$ + 0.5 $V_{DC}$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

## Recommended Operating Conditions (Note 2)

DC Supply Voltage ( $V_{DD}$ )	3 to 15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$ $V_{DC}$
Operating Temperature Range ( $T_A$ )	
CD4538BM	-55°C to +125°C
CD4538BC	-40°C to +85°C

## DC Electrical Characteristics CD4538BM (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V$		5		0.005	5		150	$\mu A$
		$V_{DD} = 10V$		10		0.010	10		300	$\mu A$
		$V_{DD} = 15V$		20		0.015	20		600	$\mu A$
$V_{OL}$	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
$V_{OH}$	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
$V_{IL}$	Low Level Input Voltage	$ I_O  < 1 \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or 9.0V		3.0		4.50	3.0		3.0	V
$V_{IH}$	High Level Input Voltage	$ I_O  < 1 \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or 9.0V	7.0		7.0	5.50		7.0		V
$I_{OL}$	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
$I_{OH}$	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
$I_{IN}$	Input Current, Pin 2 or 14	$V_{DD} = 15V, V_{IN} = 0V$ or 15V		$\pm 0.02$		$\pm 10^{-5}$	$\pm 0.05$		$\pm 0.5$	$\mu A$
$I_{IN}$	Input Current Other Inputs	$V_{DD} = 15V, V_{IN} = 0V$ or 15V		$\pm 0.1$		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1.0$	$\mu A$

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

**Note 3:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

## DC Electrical Characteristics CD4538BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units	
			Min	Max	Min	Typ	Max	Min	Max		
I <sub>DD</sub>	Quiescent Device Current	V <sub>DD</sub> = 5V	V <sub>IH</sub> = V <sub>DD</sub> V <sub>IL</sub> = V <sub>SS</sub> All Outputs Open		20		0.005	20		150	μA
		V <sub>DD</sub> = 10V			40		0.010	40		300	μA
		V <sub>DD</sub> = 15V			80		0.015	80		600	μA
V <sub>OL</sub>	Low Level Output Voltage	V <sub>DD</sub> = 5V	I <sub>O</sub>   < 1 μA V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = V <sub>SS</sub>		0.05		0	0.05		0.05	V
		V <sub>DD</sub> = 10V			0.05		0	0.05		0.05	V
		V <sub>DD</sub> = 15V			0.05		0	0.05		0.05	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>DD</sub> = 5V	I <sub>O</sub>   < 1 μA V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = V <sub>SS</sub>	4.95		4.95	5		4.95		V
		V <sub>DD</sub> = 10V		9.95		9.95	10		9.95		V
		V <sub>DD</sub> = 15V		14.95		14.95	15		14.95		V
V <sub>IL</sub>	Low Level Input Voltage	I <sub>O</sub>   < 1 μA	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V V <sub>DD</sub> = 10V, V <sub>O</sub> = 1.0V or 9.0V V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V								
		V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V			1.5		2.25	1.5		1.5	V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 1.0V or 9.0V			3.0		4.50	3.0		3.0	V
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V			4.0		6.75	4.0		4.0	V
V <sub>IH</sub>	High Level Input Voltage	I <sub>O</sub>   < 1 μA	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V V <sub>DD</sub> = 10V, V <sub>O</sub> = 1.0V or 9.0V V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V								
		V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V		3.5		3.5	2.75		3.5		V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 1.0V or 9.0V		7.0		7.0	5.50		7.0		V
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V		11.0		11.0	8.25		11.0		V
I <sub>OL</sub>	Low Level Output Current (Note 3)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.4V	V <sub>IH</sub> = V <sub>DD</sub> V <sub>IL</sub> = V <sub>SS</sub>	0.52		0.44	0.88		0.36		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 0.5V		1.3		1.1	2.25		0.9		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V		3.6		3.0	8.8		2.4		mA
I <sub>OH</sub>	High Level Output Current (Note 3)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 4.6V	V <sub>IL</sub> = V <sub>SS</sub>	−0.52		−0.44	−0.88		−0.36		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 9.5V		−1.3		−1.1	−2.25		−0.9		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 13.5V		−3.6		−3.0	−8.8		−2.4		mA
I <sub>IN</sub>	Input Current, Pin 2 or 14	V <sub>DD</sub> = 15V, V <sub>IN</sub> = 0V or 15V		±0.02		±10 <sup>−5</sup>	±0.05		±0.5	μA	
I <sub>IN</sub>	Input Current Other Inputs	V <sub>DD</sub> = 15V, V <sub>IN</sub> = 0V or 15V		±0.3		±10 <sup>−5</sup>	±0.3		±1.0	μA	

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:** V<sub>SS</sub> = 0V unless otherwise specified.

**Note 3:** I<sub>OH</sub> and I<sub>OL</sub> are tested one output at a time.

## AC Electrical Characteristics\* $T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , and $t_r = t_f = 20\text{ ns}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{TLH}$ , $t_{THL}$	Output Transition Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns ns ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Time	Trigger Operation— A or B to Q or $\bar{Q}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ Reset Operation— $C_D$ to Q or $\bar{Q}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		300 150 100 250 125 95	600 300 220 500 250 190	ns ns ns ns ns ns
$t_{WL}$ , $t_{WH}$	Minimum Input Pulse Width A, B, or $C_D$	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		35 30 25	70 60 50	ns ns ns
$t_{RR}$	Minimum Retrigger Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		0	0 0 0	ns ns ns
$C_{IN}$	Input Capacitance	Pin 2 or 14 Other Inputs		10 5	7.5	pF pF
$PW_{OUT}$	Output Pulse Width (Q or $\bar{Q}$ ) (Note: For Typical Distribution, see Figure 9)	$R_X = 100\text{ k}\Omega$ $C_X = 0.002\text{ }\mu\text{F}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$  $R_X = 100\text{ k}\Omega$ $C_X = 0.1\text{ }\mu\text{F}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$  $R_X = 100\text{ k}\Omega$ $C_X = 10.0\text{ }\mu\text{F}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	208 211 216  8.83 9.02 9.20  0.87 0.89 0.91	226 230 235  9.60 9.80 10.00  0.95 0.97 0.99	244 248 254  10.37 10.59 10.80  1.03 1.05 1.07	$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$  ms ms ms  s s s
Pulse Width Match between Circuits in the Same Package $C_X = 0.1\text{ }\mu\text{F}$ , $R_X = 100\text{ k}\Omega$		$R_X = 100\text{ k}\Omega$ $C_X = 0.1\text{ }\mu\text{F}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		$\pm 1$ $\pm 1$ $\pm 1$		% % %
<b>Operating Conditions</b>						
$R_X$	External Timing Resistance		5.0		**	$\text{k}\Omega$
$C_X$	External Timing Capacitance		0		No Limit	pF

\*AC parameters are guaranteed by DC correlated testing.

\*\*The maximum usable resistance  $R_X$  is a function of the leakage of the Capacitor  $C_X$ , leakage of the CD4538B, and leakage due to board layout, surface resistance, etc.

## Logic Diagram

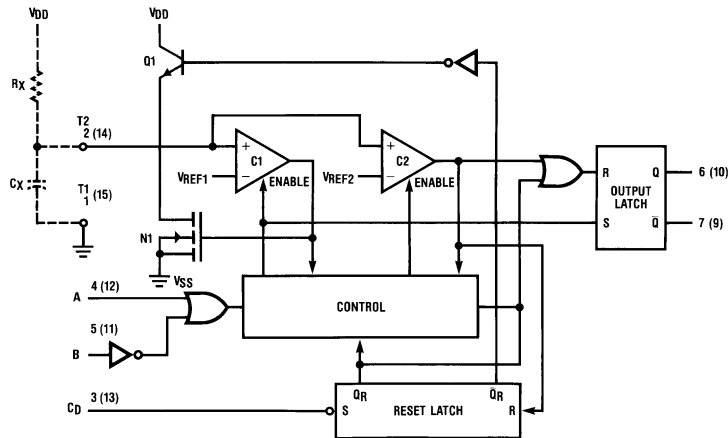


FIGURE 1

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## Theory of Operation

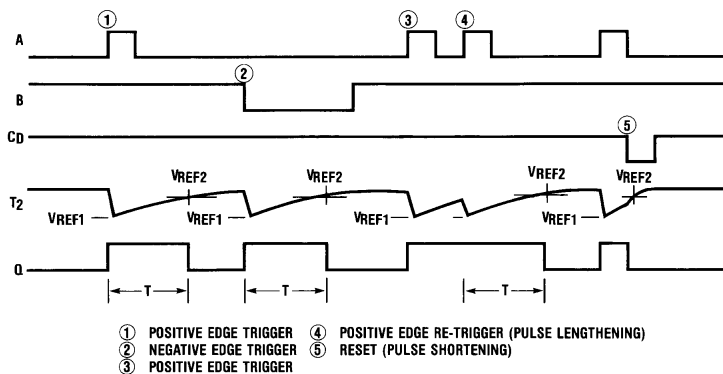


FIGURE 2

TL/F/6000-4

## Trigger Operation

The block diagram of the CD4538B is shown in *Figure 1*, with circuit operation following.

As shown in *Figures 1* and *2*, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor  $C_X$  completely charged to  $V_{DD}$ . When the trigger input A goes from  $V_{SS}$  to  $V_{DD}$  (while inputs B and  $C_D$  are held to  $V_{DD}$ ) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1. At the same time the output latch is set. With transistor N1 on, the capacitor  $C_X$  rapidly discharges toward  $V_{SS}$  until  $V_{REF1}$  is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor  $C_X$  begins to charge through the timing resistor,  $R_X$ , toward  $V_{DD}$ . When the voltage across  $C_X$  equals  $V_{REF2}$ , comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from  $V_{DD}$  to  $V_{SS}$  (while input A is at  $V_{SS}$  and input  $C_D$  is at  $V_{DD}$ ).

It should be noted that in the quiescent state  $C_X$  is fully charged to  $V_{DD}$ , causing the current through resistor  $R_X$  to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the CD4538B is that the output latch is set

via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of  $C_X$ ,  $R_X$ , or the duty cycle of the input waveform.

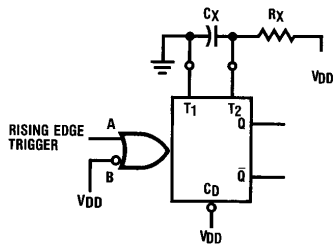
## Retrigger Operation

The CD4538B is retriggered if a valid trigger occurs followed by another valid trigger before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from  $V_{REF1}$ , but has not yet reached  $V_{REF2}$ , will cause an increase in output pulse width T. When a valid retrigger is initiated, the voltage at T2 will again drop to  $V_{REF1}$  before progressing along the RC charging curve toward  $V_{DD}$ . The Q output will remain high until time T, after the last valid retrigger.

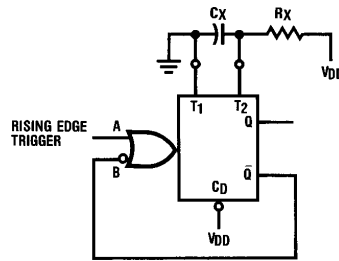
## Reset Operation

The CD4538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on  $C_D$  sets the reset latch and causes the capacitor to be fast charged to  $V_{DD}$  by turning on transistor Q1. When the voltage on the capacitor reaches  $V_{REF2}$ , the reset latch will clear and then be ready to accept another pulse. If the  $C_D$  input is held low, any trigger inputs that occur will be inhibited and the Q and  $\bar{Q}$  outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the  $C_D$  input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

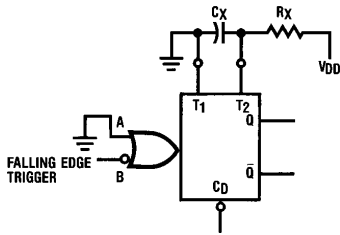
## Typical Applications



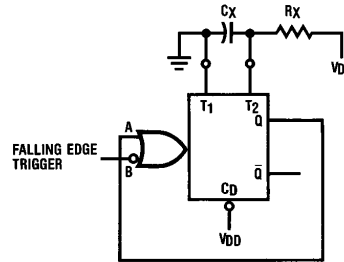
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TL/F/6000-6



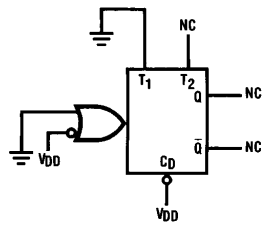
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FIGURE 3. Retriggerable Monostables Circuitry

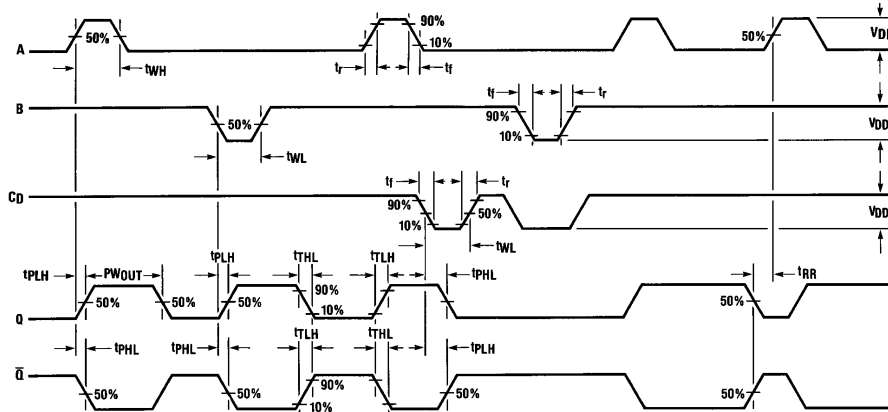
FIGURE 4. Non-Retriggerable Monostables Circuitry



TL/F/6000-9

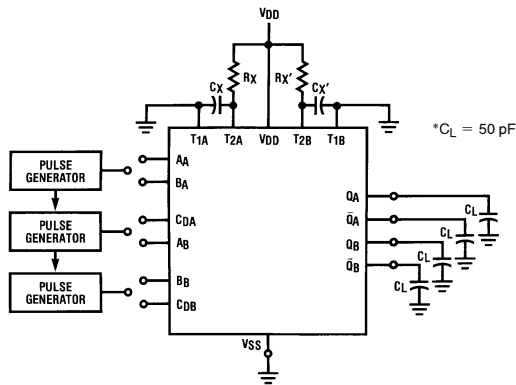
FIGURE 5. Connection of Unused Sections

## Typical Applications (Continued)



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FIGURE 6. Switching Test Waveforms



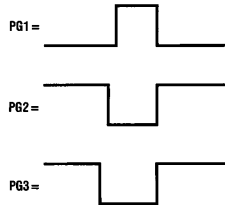
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### Input Connections

Characteristics	CD	A	B
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ $PW_{OUT}$ , $t_{WH}$ , $t_{WL}$	V <sub>DD</sub>	PG1	V <sub>DD</sub>
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ $PW_{OUT}$ , $t_{WH}$ , $t_{WL}$	V <sub>DD</sub>	V <sub>SS</sub>	PG2
$t_{PLH(R)}$ , $t_{PHL(R)}$ , $t_{WH}$ , $t_{WL}$	PG3	PG1	PG2

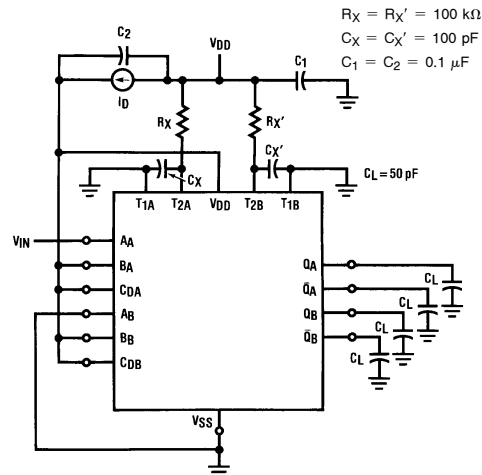
\*Includes capacitance of probes, wiring, and fixture parasitic

**Note:** Switching test waveforms for PG1, PG2, PG3 are shown in Figure 6.

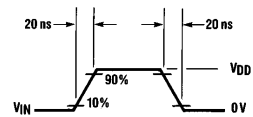


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FIGURE 7. Switching Test Circuit



TL/F/6000-12

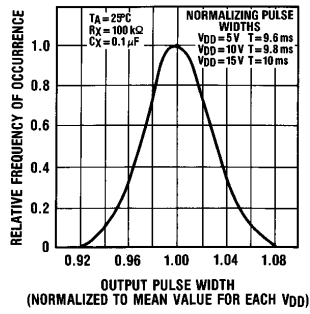


Duty Cycle = 50%

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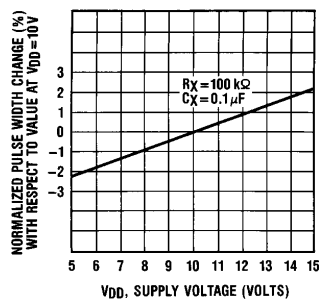
FIGURE 8. Power Dissipation Test Circuit and Waveforms

## Typical Applications (Continued)



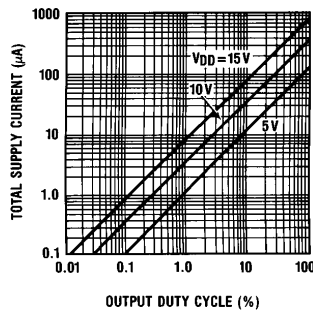
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FIGURE 9. Typical Normalized Distribution of Units for Output Pulse Width



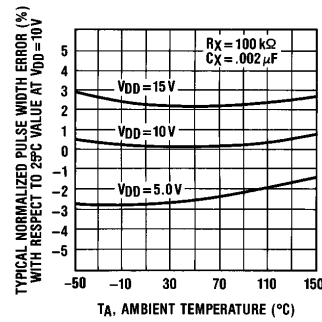
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FIGURE 10. Typical Pulse Width Variation as a Function of Supply Voltage  $V_{DD}$



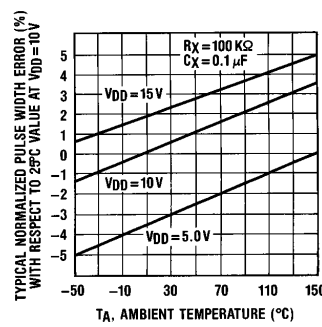
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FIGURE 11. Typical Total Supply Current Versus Output Duty Cycle,  $R_X = 100\text{ k}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $C_X = 100\text{ pF}$ , One Monostable Switching Only



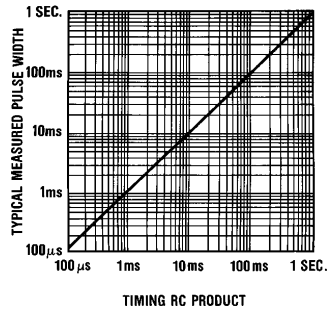
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FIGURE 12. Typical Pulse Width Error Versus Temperature



TL/F/6000-18

FIGURE 13. Typical Pulse Width Error Versus Temperature

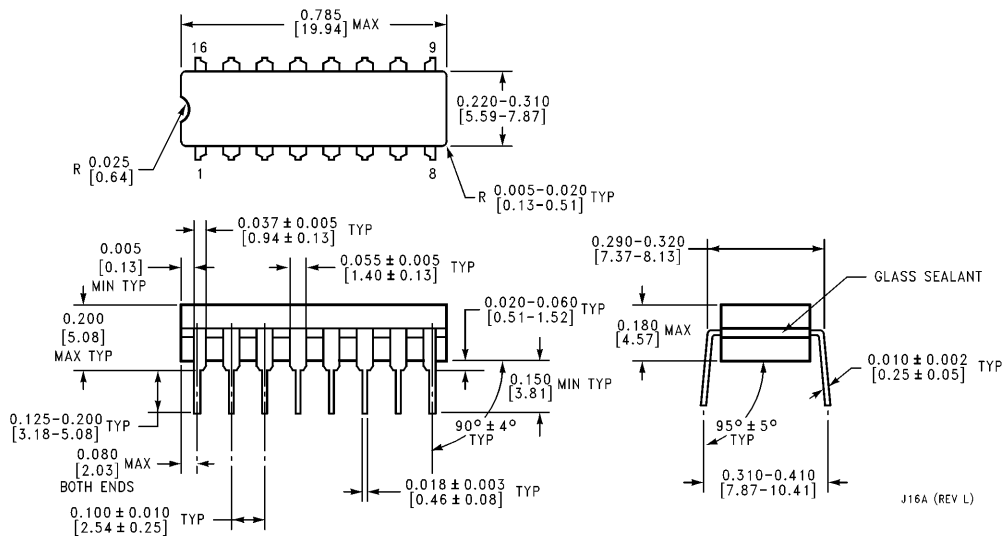


TL/F/6000-20

FIGURE 14. Typical Pulse Width Versus Timing RC Product



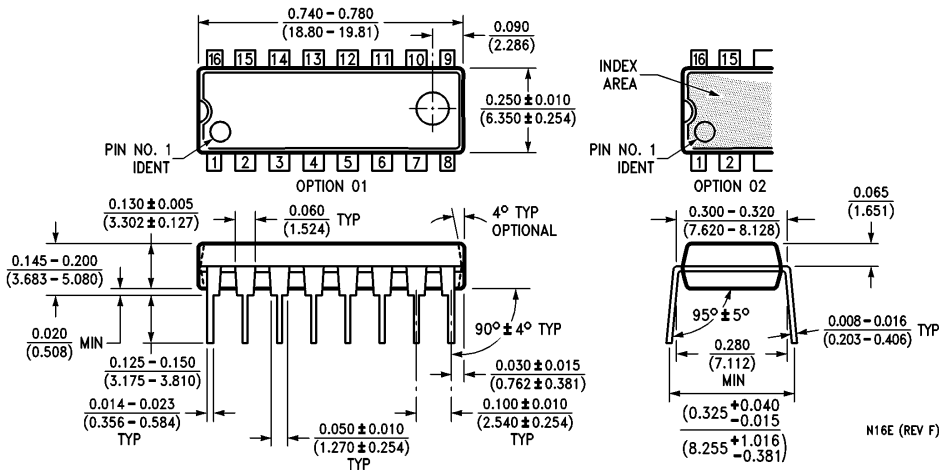
**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number CD4538BMJ or CD4538BCJ**  
**NS Package Number J16A**

J16A (REV L)

**Physical Dimensions** inches (millimeters) (Continued)



**Molded Dual-In-Line Package (N)**  
**Order Number CD4538BMN or CD4538BCN**  
**NS Package Number N16E**

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