

# CD54HCT573, CD74HCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS455C – FEBRUARY 2001 – REVISED MAY 2004

- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Wide Operating Temperature Range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Balanced Propagation Delays and Transition Times
- Standard Outputs Drive Up To 10 LS-TTL Loads
- Significant Power Reduction Compared to LS-TTL Logic ICs
- Inputs Are TTL-Voltage Compatible

## description/ordering information

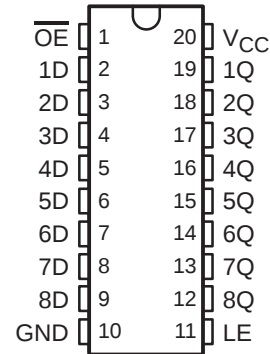
The 'HCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{\text{OE}}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{\text{OE}}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

CD54HCT573 . . . F PACKAGE  
CD74HCT573 . . . DB, E, OR M PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

| $T_A$                                          | PACKAGE <sup>†</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|------------------------------------------------|----------------------|---------------|-----------------------|------------------|
| $-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ | PDIP – E             | Tube          | CD74HCT573E           | CD74HCT573E      |
|                                                | SSOP – DB            | Tape and reel | CD74HCT573DBR         | HK573            |
|                                                | SOIC – M             | Tube          | CD74HCT573M           | HCT573M          |
|                                                |                      | Tape and reel | CD74HCT573M96         |                  |
|                                                | CDIP – F             | Tube          | CD54HCT573F3A         | CD54HCT573F3A    |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

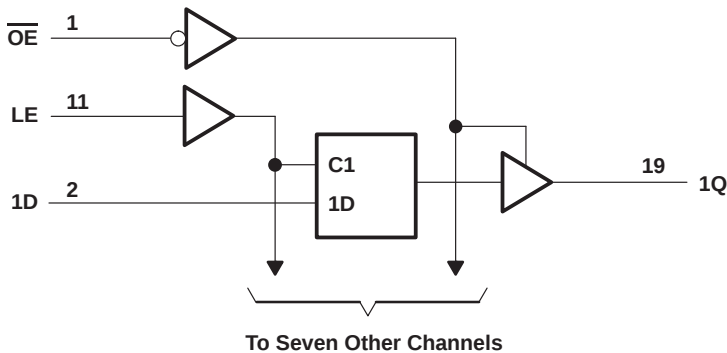
**CD54HCT573, CD74HCT573**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

SCLS455C – FEBRUARY 2001 – REVISED MAY 2004

FUNCTION TABLE  
(each latch)

| INPUTS          |    |   | OUTPUT |
|-----------------|----|---|--------|
| $\overline{OE}$ | LE | D | Q      |
| L               | H  | H | H      |
| L               | H  | L | L      |
| L               | L  | X | $Q_0$  |
| H               | X  | X | Z      |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                      |                |
|--------------------------------------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                                                       | –0.5 V to 7 V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)           | ±20 mA         |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)          | ±20 mA         |
| Continuous output drain current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ )          | ±35 mA         |
| Continuous output source or sink current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) | ±25 mA         |
| Continuous current through $V_{CC}$ or GND                                           | ±50 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package                    | 70°C/W         |
| E package                                                                            | 69°C/W         |
| M package                                                                            | 58°C/W         |
| Storage temperature range, $T_{stg}$                                                 | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# CD54HCT573, CD74HCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

|                 |                                    | T <sub>A</sub> = 25°C |                 | T <sub>A</sub> = -55°C TO 125°C |                 | T <sub>A</sub> = -40°C TO 85°C |                 | UNIT |
|-----------------|------------------------------------|-----------------------|-----------------|---------------------------------|-----------------|--------------------------------|-----------------|------|
|                 |                                    | MIN                   | MAX             | MIN                             | MAX             | MIN                            | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     | 4.5                   | 5.5             | 4.5                             | 5.5             | 4.5                            | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | 2                     |                 | 2                               |                 | 2                              |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            |                       | 0.8             |                                 | 0.8             |                                | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      |                       | V <sub>CC</sub> |                                 | V <sub>CC</sub> |                                | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                     |                       | V <sub>CC</sub> |                                 | V <sub>CC</sub> |                                | V <sub>CC</sub> | V    |
| Δt/Δv           | Input transition rise or fall rate |                       | 500             |                                 | 500             |                                | 500             | ns   |

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                     | TEST CONDITIONS                                                            |                          | V <sub>CC</sub> | T <sub>A</sub> = 25°C |      | T <sub>A</sub> = -55°C TO 125°C |     | T <sub>A</sub> = -40°C TO 85°C |      | UNIT |
|-------------------------------|----------------------------------------------------------------------------|--------------------------|-----------------|-----------------------|------|---------------------------------|-----|--------------------------------|------|------|
|                               |                                                                            |                          |                 | MIN                   | MAX  | MIN                             | MAX | MIN                            | MAX  |      |
| V <sub>OH</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                        | I <sub>OH</sub> = -20 μA | 4.5 V           | 4.4                   |      | 4.4                             |     | 4.4                            |      | V    |
|                               |                                                                            | I <sub>OH</sub> = -6 mA  |                 | 3.98                  |      | 3.7                             |     | 3.84                           |      |      |
| V <sub>OL</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                        | I <sub>OL</sub> = 20 μA  | 4.5 V           |                       | 0.1  |                                 | 0.1 |                                | 0.1  | V    |
|                               |                                                                            | I <sub>OL</sub> = 6 mA   |                 |                       | 0.26 |                                 | 0.4 |                                | 0.33 |      |
| I <sub>I</sub>                | V <sub>I</sub> = V <sub>CC</sub> or 0                                      |                          | 5.5 V           |                       | ±0.1 |                                 | ±1  |                                | ±1   | μA   |
| I <sub>OZ</sub>               | V <sub>O</sub> = V <sub>CC</sub> or 0                                      |                          | 5.5 V           |                       | ±0.5 |                                 | ±10 |                                | ±5   | μA   |
| I <sub>CC</sub>               | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0                  |                          | 5.5 V           |                       | 8    |                                 | 160 |                                | 80   | μA   |
| ΔI <sub>CC</sub> <sup>†</sup> | One input at V <sub>CC</sub> - 2.1 V, Other inputs at 0 or V <sub>CC</sub> |                          | 4.5 V to 5.5 V  |                       | 360  |                                 | 490 |                                | 450  | μA   |
| C <sub>i</sub>                |                                                                            |                          |                 |                       | 10   |                                 | 10  |                                | 10   | pF   |
| C <sub>O</sub>                |                                                                            |                          |                 |                       | 20   |                                 | 20  |                                | 20   | pF   |

<sup>†</sup> Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

| INPUT                  | UNIT LOAD |
|------------------------|-----------|
| $\overline{\text{OE}}$ | 1.25      |
| Any D                  | 0.3       |
| LE                     | 0.65      |

Unit load is ΔI<sub>CC</sub> limit specified in electrical characteristics table (e.g., 360 μA max at 25°C).

# CD54HCT573, CD74HCT573

## OCTAL TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 4.5\text{ V}$  (unless otherwise noted) (see Figure 1)

|          |                             | $T_A = 25^\circ\text{C}$ |     | $T_A = -55^\circ\text{C}$<br>TO $125^\circ\text{C}$ |     | $T_A = -40^\circ\text{C}$<br>TO $85^\circ\text{C}$ |     | UNIT |
|----------|-----------------------------|--------------------------|-----|-----------------------------------------------------|-----|----------------------------------------------------|-----|------|
|          |                             | MIN                      | MAX | MIN                                                 | MAX | MIN                                                | MAX |      |
| $t_w$    | Pulse duration, LE high     | 16                       |     | 24                                                  |     | 20                                                 |     | ns   |
| $t_{su}$ | Setup time, data before LE↓ | 13                       |     | 20                                                  |     | 16                                                 |     | ns   |
| $t_h$    | Hold time, data after LE↓   | 10                       |     | 15                                                  |     | 13                                                 |     | ns   |

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 4.5\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)        | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE    | T <sub>A</sub> = 25°C |     | T <sub>A</sub> = −55°C<br>TO 125°C |     | T <sub>A</sub> = −40°C<br>TO 85°C |     | UNIT |
|------------------|------------------------|----------------|------------------------|-----------------------|-----|------------------------------------|-----|-----------------------------------|-----|------|
|                  |                        |                |                        | MIN                   | MAX | MIN                                | MAX | MIN                               | MAX |      |
| t <sub>pd</sub>  | D                      | Q              | C <sub>L</sub> = 50 pF | 35                    |     | 53                                 |     | 44                                |     | ns   |
|                  | LE                     |                |                        | 35                    |     | 53                                 |     | 44                                |     |      |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | Q              | C <sub>L</sub> = 50 pF | 35                    |     | 53                                 |     | 44                                |     | ns   |
| t <sub>dis</sub> | $\overline{\text{OE}}$ | Q              | C <sub>L</sub> = 50 pF | 35                    |     | 53                                 |     | 44                                |     | ns   |
| t <sub>t</sub>   |                        | Q              | C <sub>I</sub> = 50 pF | 12                    |     | 18                                 |     | 15                                |     | ns   |

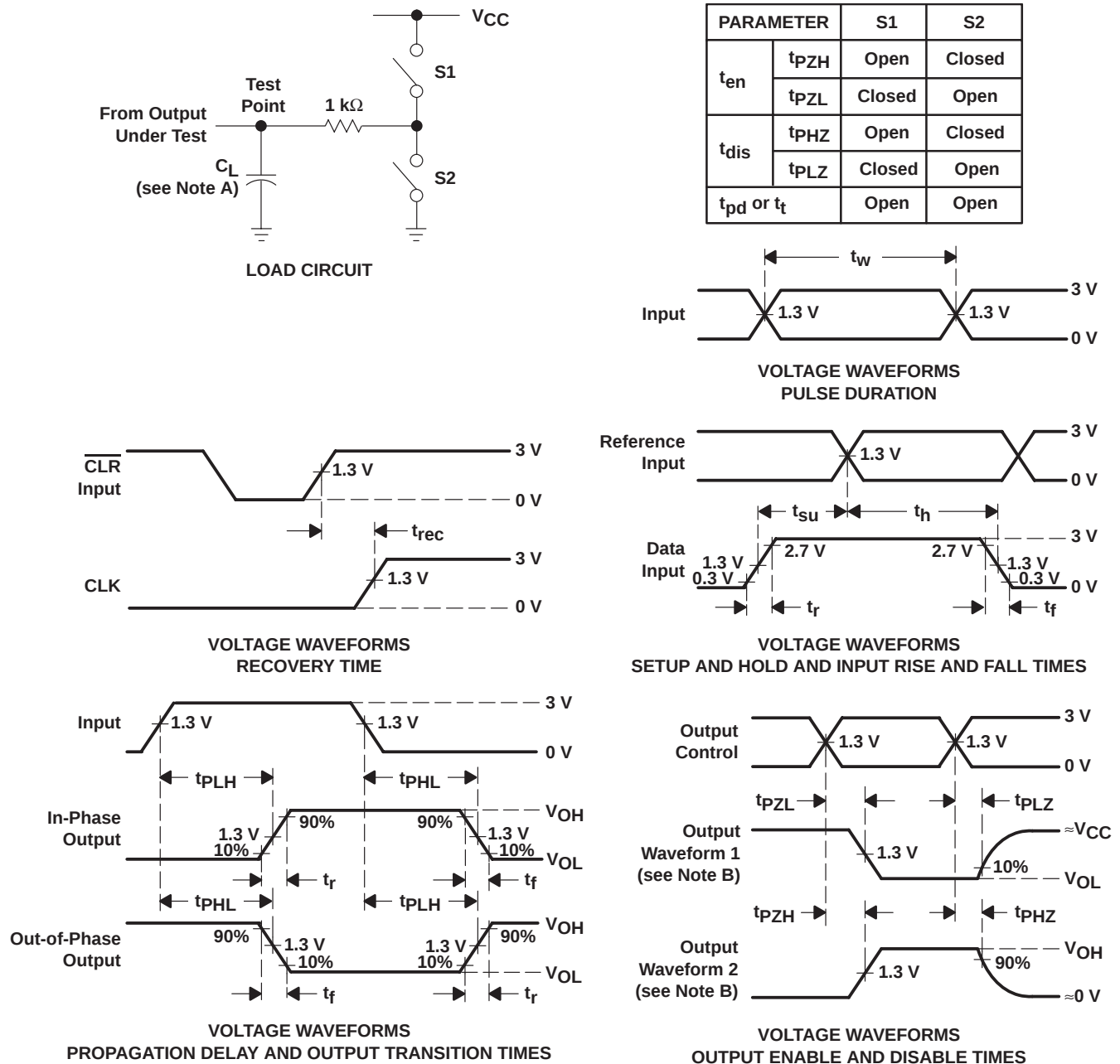
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TYP | UNIT |
|-----------|-------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | 53  | pF   |

# CD54HCT573, CD74HCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - The outputs are measured one at a time, with one input transition per measurement.
  - $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .
  - $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)         | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 5962-8685601RA   | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8685601RA<br>CD54HCT573F3A | <a href="#">Samples</a> |
| CD54HCT573F      | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | CD54HCT573F                     | <a href="#">Samples</a> |
| CD54HCT573F3A    | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-8685601RA<br>CD54HCT573F3A | <a href="#">Samples</a> |
| CD74HCT573DBR    | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HK573                           | <a href="#">Samples</a> |
| CD74HCT573E      | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HCT573E                     | <a href="#">Samples</a> |
| CD74HCT573EE4    | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HCT573E                     | <a href="#">Samples</a> |
| CD74HCT573M      | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT573M                         | <a href="#">Samples</a> |
| CD74HCT573M96    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT573M                         | <a href="#">Samples</a> |
| CD74HCT573M96G4  | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT573M                         | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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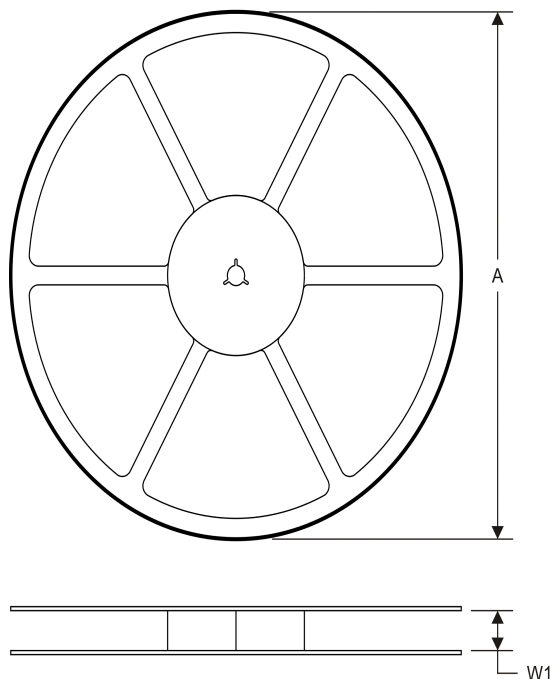
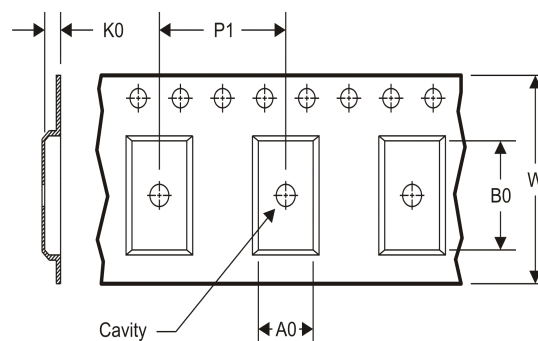
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**OTHER QUALIFIED VERSIONS OF CD54HCT573, CD74HCT573 :**

- Catalog: [CD74HCT573](#)
- Military: [CD54HCT573](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


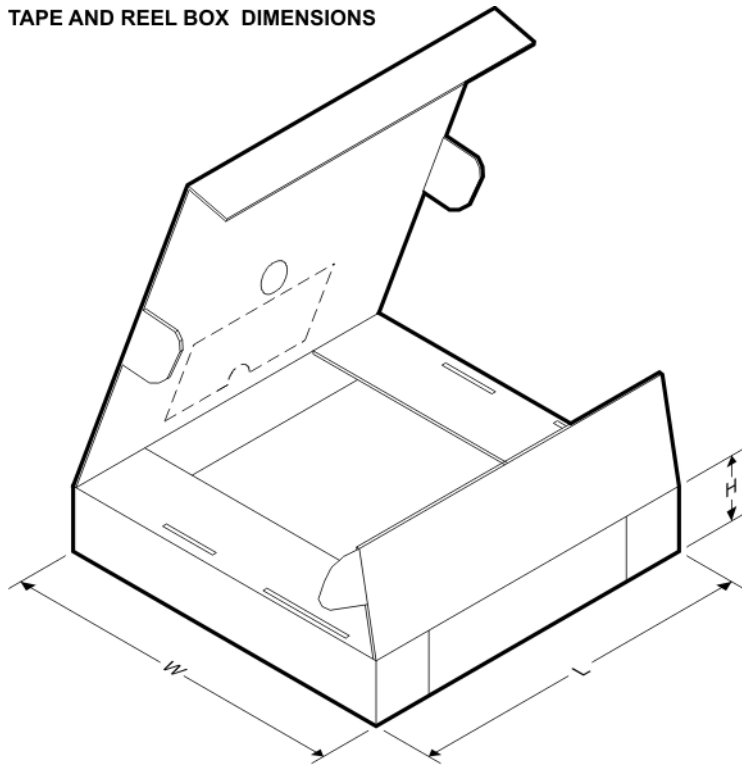
|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HCT573DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| CD74HCT573M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



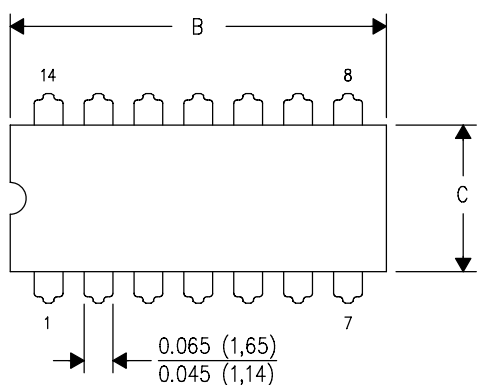
\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HCT573DBR | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| CD74HCT573M96 | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

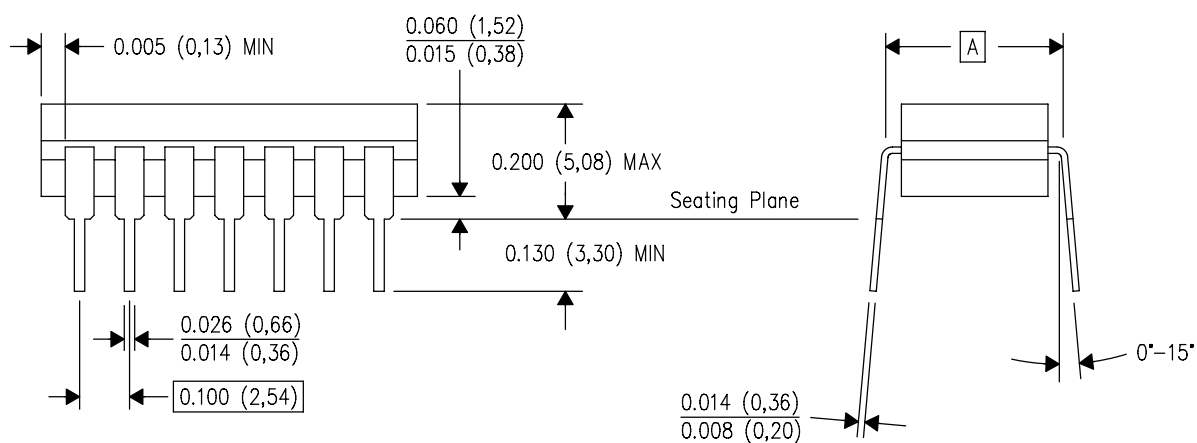
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



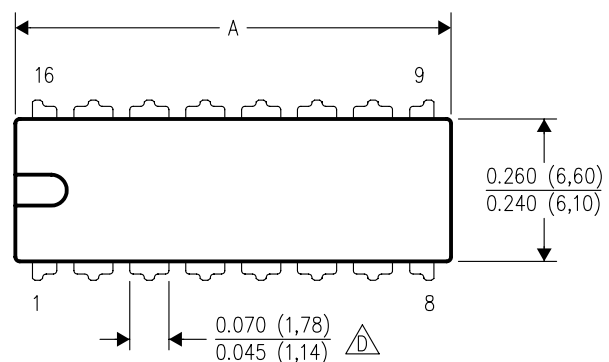
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

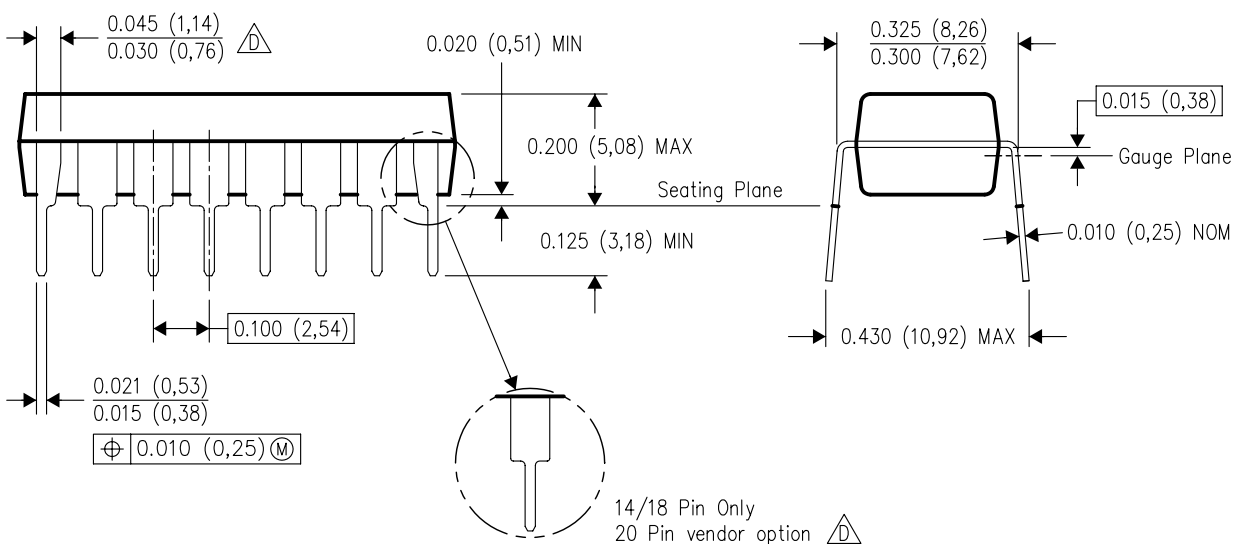
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

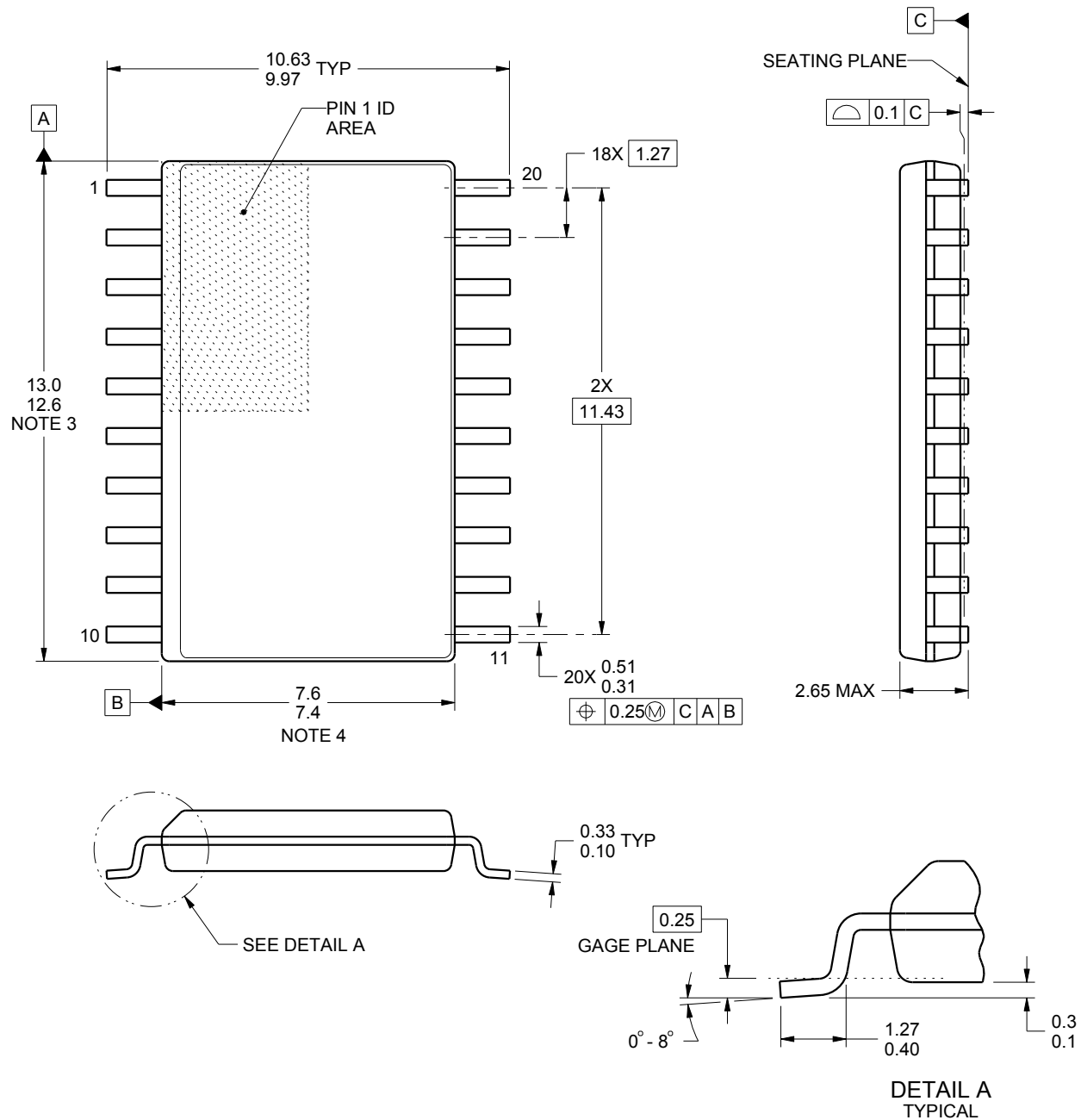
- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

**DW0020A**

## PACKAGE OUTLINE

**SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

NOTES:

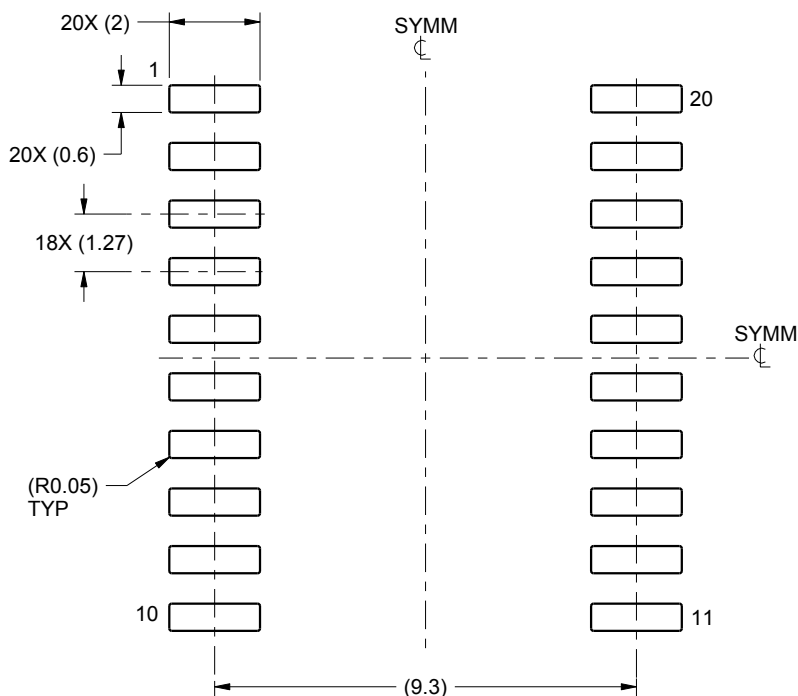
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

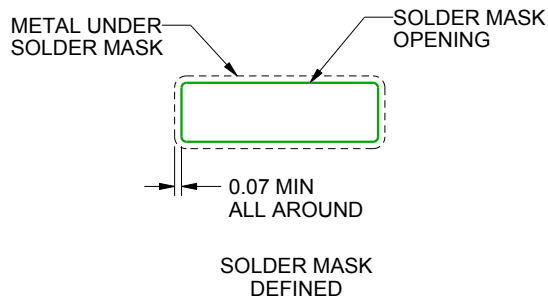
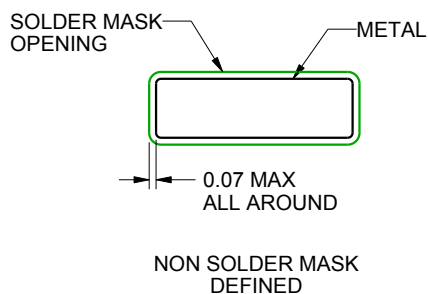
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

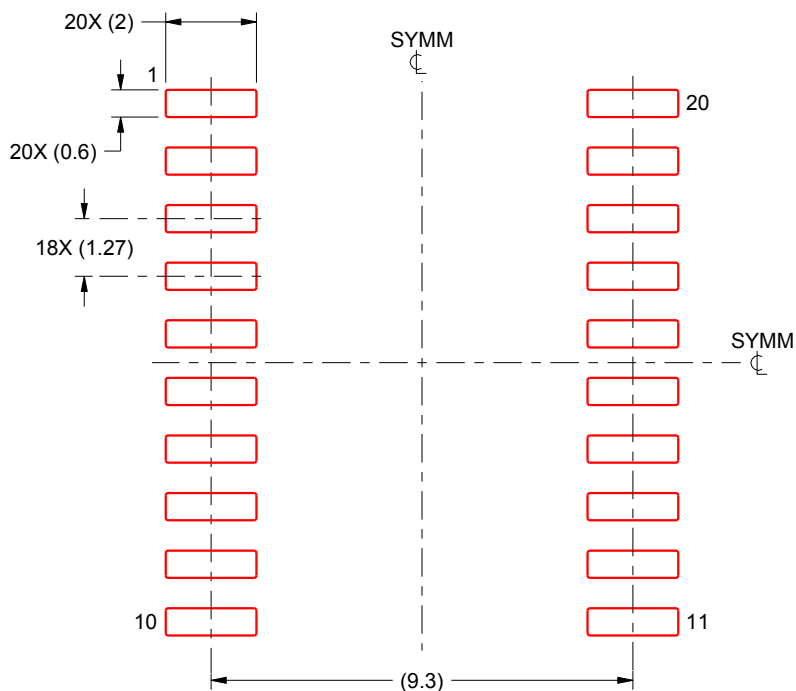
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

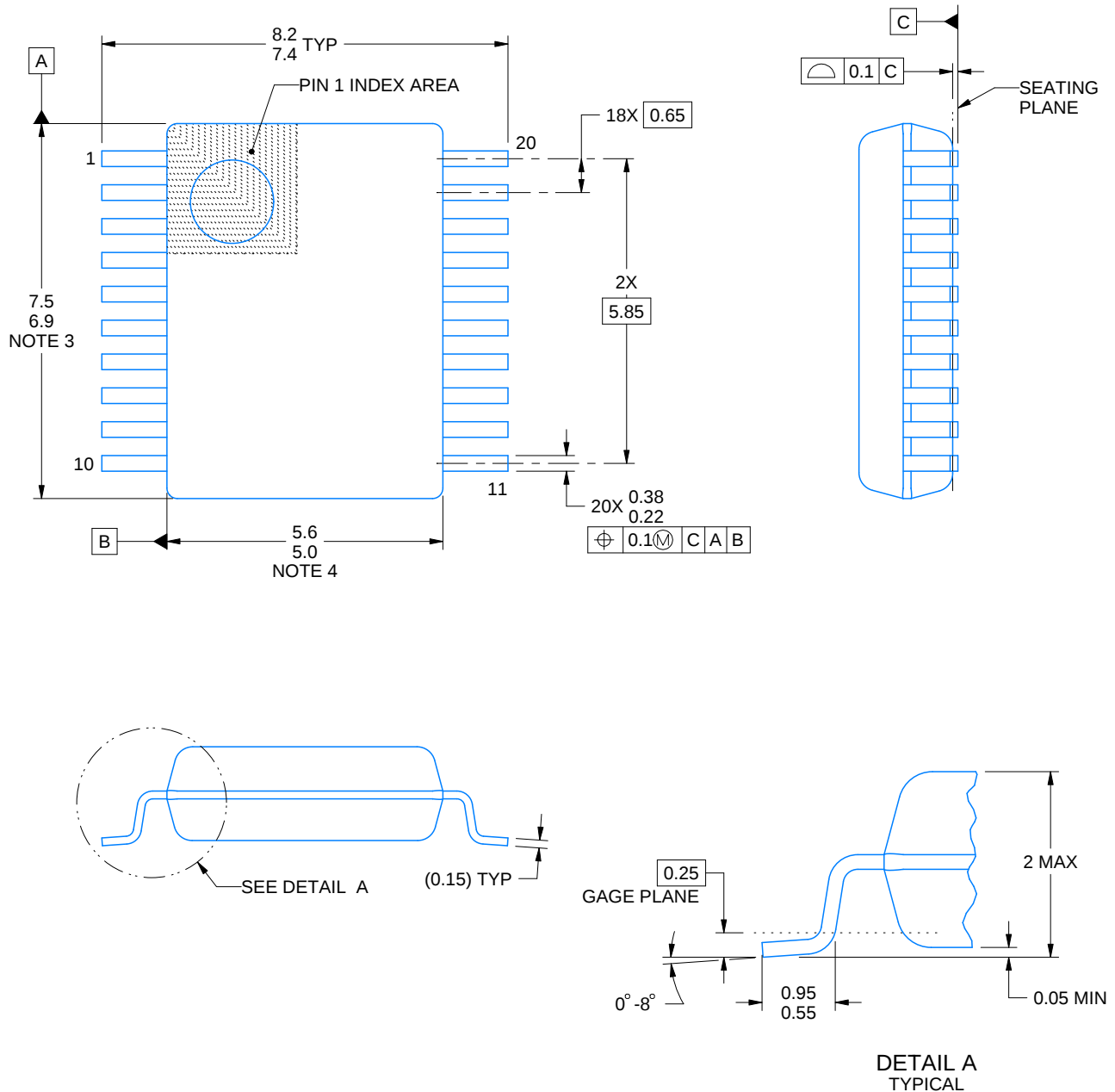
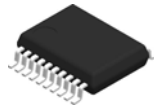


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

## NOTES:

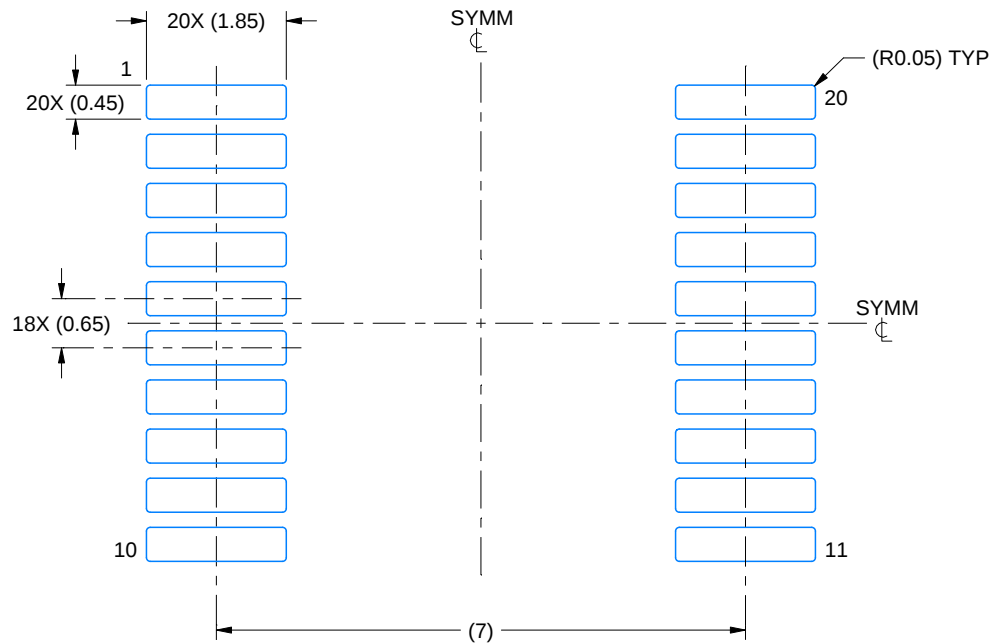
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

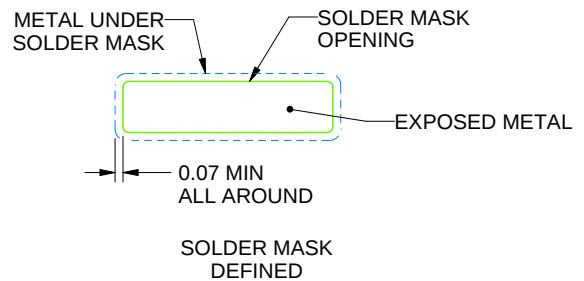
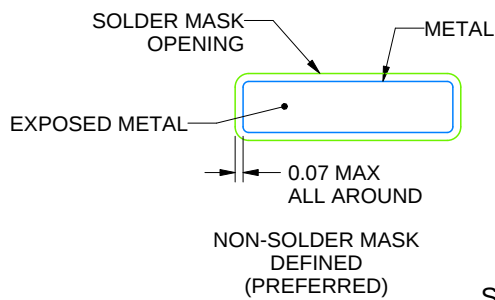
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

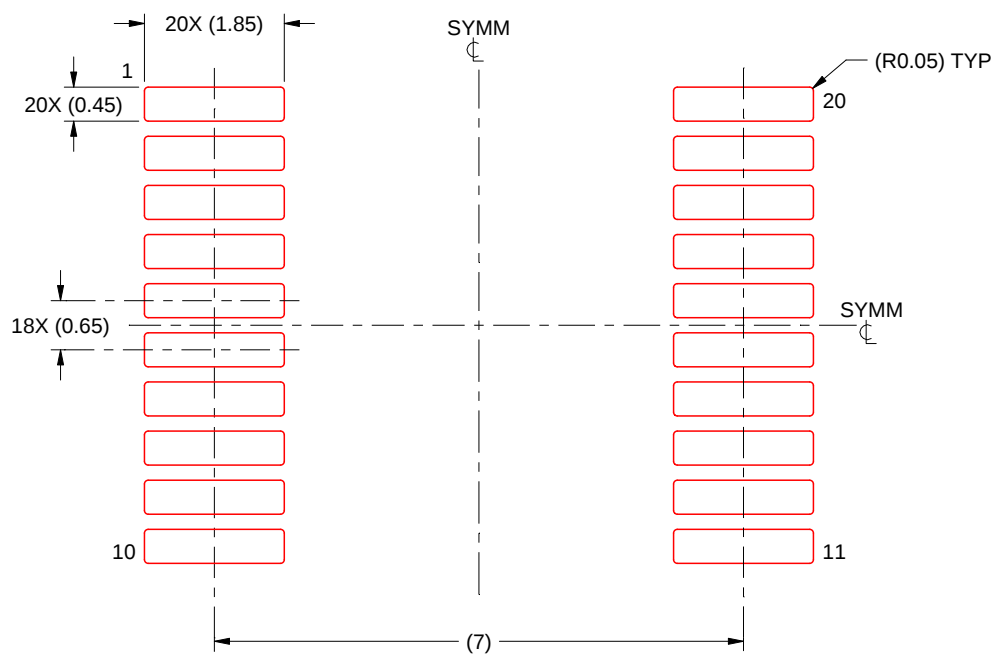
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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