

# DBL 494

## PULSE WIDTH MODULATION

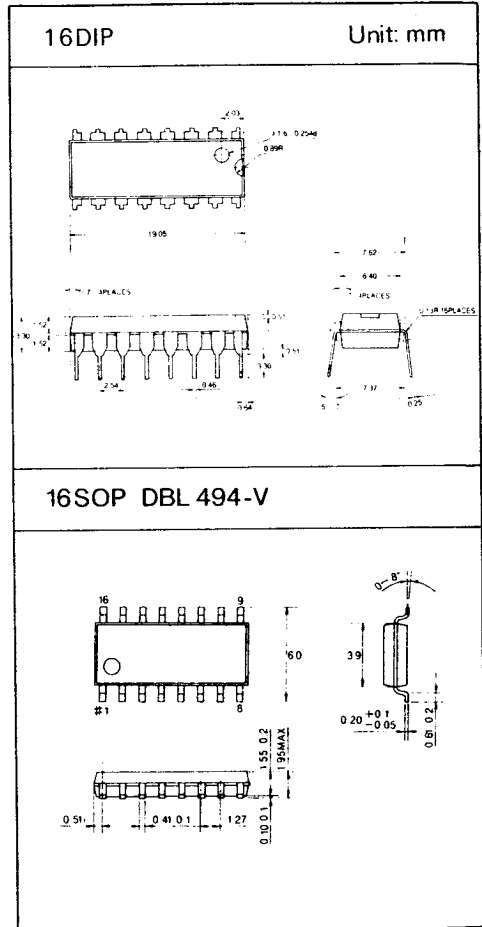
The DBL494 is a monolithic integrated circuit which includes all the necessary building blocks for the design of pulse width modulated(PWM) switching power supplies, including push-pull, bridge and series configuration. The device can operate at switching frequencies between 1KHz and 300KHz and output voltages up to 40 V. The DBL494 is specified over an operating temperature range of 0°C to 70°C

### FEATURES

- Uncommitted output transistors capable of 200mA source or sink.
- Internal protection from double pulsing of outputs with narrow pulse widths or with supply voltages belows specified limits.
- Dead time control comparator
- Output control selects single-ended or push-pull operation
- Easily synchronized(slaved) to other circuits.

### MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Supply Voltage	$V_{CC}$	42	V
Voltage From Any Pin to Ground (except pin 8 and pin 11)	$V_{IN}$	$V_{CC} + 0.3$	V
Output Collector Voltage	$V_{C1}, V_{C2}$	42	V
Peak Collector Current	$I_{C1}, I_{C2}$	250	mA
Power Dissipation	$P_D$	1500	mW
Operating Temperature	$T_{opr}$	0 ~ +70	°C
Storage Temperature	$T_{stg}$	-65 ~ +150	°C

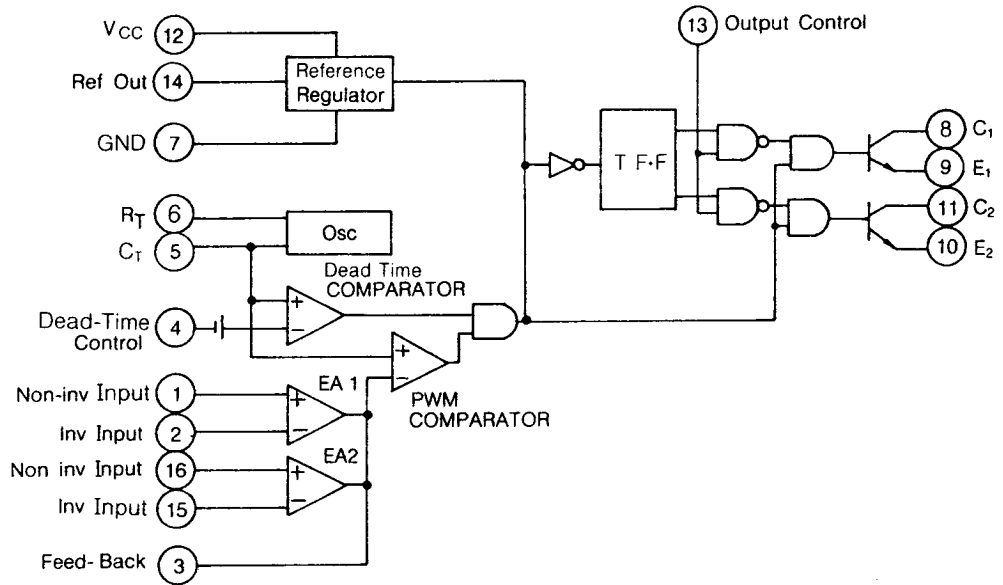


# DBL 494

## RECOMMENDED OPERATING CONDITION

Characteristic	Symbol	Min.	Max.	Unit
Supply Voltage	$V_{CC}$	7	40	V
Voltage on Any Pin Except Pin 8 and 11(Referenced to Ground)	$V_{IN}$	-0.3	$V_{CC} + 0.3$	V
Output Voltage	$V_{C1}, V_{C2}$	-0.3	40	V
Output Collector Current	$I_{C1}, I_{C2}$	-	200	mA
Timing Capacitor	$C_t$	470	-	PF
		-	10	$\mu F$
Timing Resistor	$R_t$	1.8	500	K $\Omega$
Oscillator Frequency	fosc	1	300	KHz

## BLOCK DIAGRAM



# DBL 494

## ELECTRICAL CHARACTERISTICS

(Unless otherwise specified,  $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{CC} = 15\text{V}$ ,  $f = 10\text{kHz}$ )

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Reference Section						
Reference Voltage	$V_{REF}$	$I_{REF} = 10\text{mA}$	4.75	5	5.25	V
Line Regulation	$V_{LINE}$	$7\text{V} < V_{CC} < 40\text{V}$	—	2	25	mV
Load Regulation	$V_{LOAD}$	$1\text{mA} < I_{REF} < 10\text{mA}$	—	1	15	mV
Temperature Coefficient		$0^\circ\text{C} < T_a < 70^\circ\text{C}$	—	0.01	0.03	%/ $^\circ\text{C}$

### Oscillator Section

Oscillator Frequency	fosc	$C_t = 0.01\mu\text{F}$ , $R_t = 12\text{K}\Omega$	—	10	—	KHz
Oscillator Frequency Change Over Operating Temperature Range	$\Delta f_{osc}$	$C_t = 0.01\mu\text{F}$ , $R_t = 12\text{K}\Omega$	—	—	2	%

### Dead-Time Control Section

Input Bias Current(Pin4)	$I_{IB(DT)}$	$V_{CC} = 15\text{V}$ , $0\text{V} < V_4 < 5.25\text{V}$	—	-2	-10	$\mu\text{A}$
Maximum Duty cycle, Each Output	DC(MAX)	$V_{CC} = 15\text{V}$ , Pin 4 = 0V, Output Control Pin = $V_{REF}$	43	—	45	%
Input Threshold Voltage	Zero Duty	$V_{TH}$	—	3	3.3	V
	Max Duty		0	—	—	

### Error Amplifier Section

Input Offset Voltage	$V_{IOS}$	$V_3 = 2.5\text{V}$	—	2	10	mV
Input Offset Current*	$I_{IOS}$	$V_3 = 2.5\text{V}$	—	25	250	nA
Input Bias Current	$I_{IB}$	$V_3 = 2.5\text{V}$	—	0.2	1	$\mu\text{A}$
Input Common Mode voltage Range	$V_{ICR}$	$7\text{V} < V_{CC} < 40\text{V}$	-0.3	—	$V_{CC}$	V
Large Signal Open Loop Voltage Range	$G_{VO}$	$0.5\text{V} < V_3 < 3.5\text{V}$	60	74	—	dB
Unity Gain Band width	fc	—	—	650	—	KHz

### PWM Compacator Section(Pin3)

Inhibit Threshold Voltage	$V_{THI}$	Zero Duty cycle	—	4	4.5	V
*Output Source Current	$I_{O^+}$	$0.5\text{V} < V_3 < 3.5\text{V}$	2	—	—	mA
*Output Sink Current	$I_{O^-}$	$0.5\text{V} < V_3 < 3.5\text{V}$	-0.2	-0.6	—	mA

### Output Section

Output Saturation Voltage	Common-Emitter	$V_{CE(SAT)}$	$V_E = 15\text{V}$ , $I_C = 200\text{mA}$	—	1.1	1.3	V
	Emitter-Follower		$V_C = 15\text{V}$ , $I_E = 200\text{mA}$	—	1.5	2.5	
Collector off-state Current	$I_C(\text{off})$	$V_{CC} = V_C = 40\text{V}$ , $V_E = 0$	—	2	100	$\mu\text{A}$	
Emitter off-state Current	$I_E(\text{off})$	$V_{CC} = V_C = 40\text{V}$ , $V_E = 0$	—	—	-100	$\mu\text{A}$	

\* : These limits apply when the voltage measured at Pin 3 is within the range specified.

# DBL 494

## ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Out put Control(Pin 13)							
Output Control Voltage Required for single-Ended or Parallel Output Operation	$V_{OCL}$				0.4	V	
Output Control Voltage Required for Push-pull operation	$V_{OCH}$		2.4			V	
Total Device							
Standby power Supply Current	$I_{CC}$			6	10	mA	
Output AC Characteristic							
Rise Time	Common Emitter	$T_r$			100	200	ns
	Emitter Follower				100	200	ns
Fall Time	Common Emitter	$T_f$			25	100	ns
	Emitter Follower				40	100	ns

## INFORMATION

The basic oscillator (switching) frequency is controlled by an external resistor ( $R_t$ ) and capacitor ( $C_t$ ). The relationship between the values of  $R_t$ ,  $C_t$  and frequency is shown in

The level of the sawtooth wave form is compared with an error voltage by the pulse width modulated comparator. The output of the PWM Comparator directs the pulse steering flip flop and the output control logic.

The error voltage is generated by the error amplifier. The error amplifier boosts the voltage difference between the output and the 5V internal reference. See Figure 7 for error amp sensing techniques. The second error amp is typically used to implement current limiting.

The output control logic (Pin 13) selects either push-pull or single-ended operation of the output transistors (see Figure 6).

The dead time control prevents on-state overlap of the output transistors as can be seen in Figure 5. The dead time is approximately 3 to 5% of the total period if the dead time control (pin 4) is grounded. This dead time can be increased by connecting the dead time control to a voltage up to 5 V.

The frequency response of the error amps (Figure 11) can be modified by using external resistors and capacitors. These components are typically connected between the compensation terminal (pin 3) and the inverting input of the error amps (pin 2 or pin 15).

The switching frequency of two or more DBL494 circuits can be synchronized. The timing capacitor,  $C_t$  is connected as shown in Figure 8. Charging current is provided by the master circuit. Discharging is through all the circuits slaved to the master.  $R_t$  is required only for the master circuit.

## □ TEST CIRCUIT

Fig. 1 Error Amplifier Test Circuit

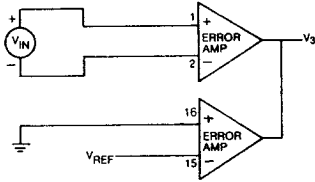


Fig. 2 Current Limit sense Amplifier Test Circuit

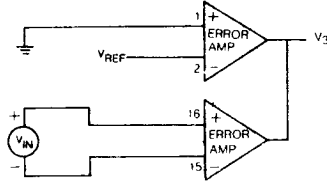


Fig. 3 Common-Emitter Configuration Test circuit and Waveform

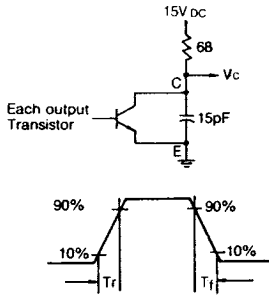


Fig. 5 Dead-Time and Feedback Control Test Circuit

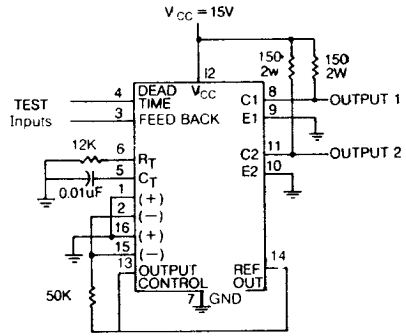
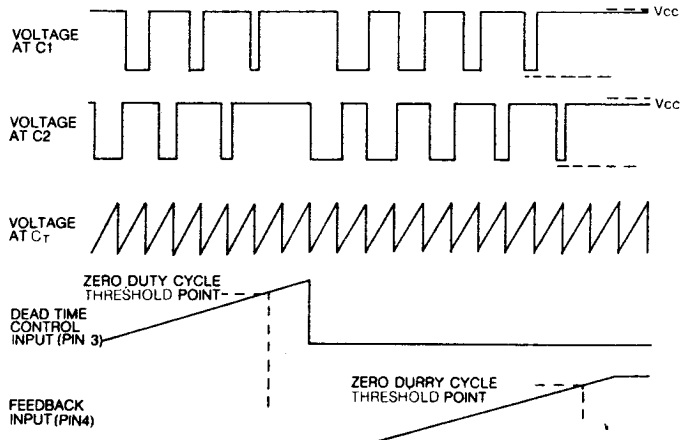


Fig. 4 Emitter-Follower Configuration Test circuit and waveform Voltage waveforms



Voltage waveforms



## □ TEST CIRCUIT

Fig. 1 Error Amplifier Test Circuit

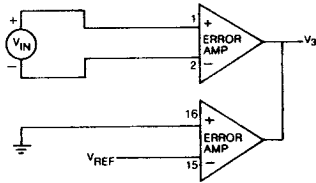


Fig. 2 Current Limit sense Amplifier Test Circuit

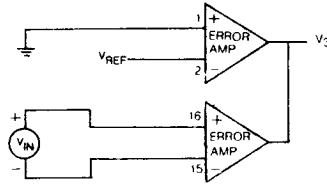


Fig. 3 Common-Emitter Configuration Test circuit and Waveform

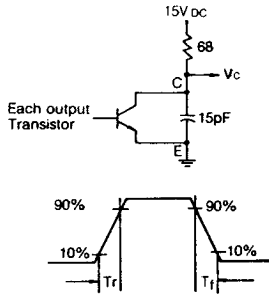


Fig. 5 Dead-Time and Feedback Control Test Circuit

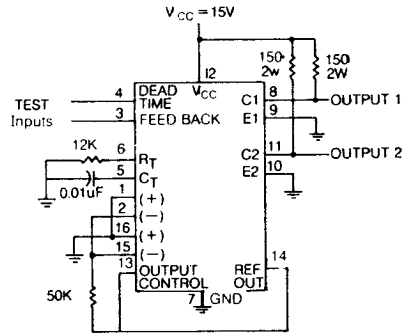


Fig. 4 Emitter-Follower Configuration Test circuit and waveform Voltage waveforms



Voltage waveforms

