

2PG006

Silicon N-channel enhancement IGBT

For plasma display panel drive
 For high speed switching circuits

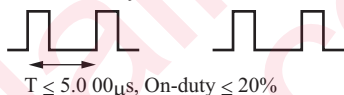
■ Features

- Low collector-emitter saturation voltage: $V_{CE(sat)} < 2.4$ V
- High-speed switching: $t_r = 175$ ns (typ.)

■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-emitter voltage (E-B short)	V_{CES}	430	V
Gate-emitter voltage (E-B short)	V_{GES}	-30 to +35	V
Collector current	I_C	40	A
Peak collector current *	I_{CP}	230	A
Power dissipation	P_C	40	W
		$T_a = 25^\circ\text{C}$	2.0
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note) *: Assurance of repetitive pulse. (Repetitive period ≤ 5 μs on-duty $\leq 20\%$)
 But, it must stay within 40% of all that the time impressed pulse repetitively.



■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

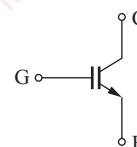
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter voltage (E-B short)	V_{CES}	$I_C = 1$ mA, $V_{GE} = 0$	430			V
Collector-emitter cutoff current (E-B short) *	I_{CES}	$V_{CE} = 344$ V, $V_{GE} = 0$			5.0	μA
Gate-emitter cutoff current (E-B short)	I_{GES}	$V_{GE} = \pm 35$ V, -30 V, $V_{CE} = 0$			± 1.0	μA
Gate-emitter threshold voltage	$V_{GE(th)}$	$V_{CE} = 10$ V, $I_C = 1.0$ mA	3.0		5.5	V
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_{GE} = 15$ V, $I_C = 40$ A		1.75	2.4	V
Collector-emitter reverse break down voltage	$-V_{CE}$	$I_C = -100$ mA, $V_{GE} = 15$ V	18	22.5		V
Short-circuit input capacitance (Common emitter)	C_{ies}	$V_{CE} = 25$ V, $V_{GE} = 0$, $f = 1$ MHz		1 200		pF
Short-circuit output capacitance (Common emitter)	C_{oes}			130		pF
Reverse transfer capacitance (Common emitter)	C_{res}			20		pF
Gate charge load	Q_g	$V_{CC} = 200$ V, $I_C = 40$ A, $V_{GE} = 15$ V		54		nC
Gate-emitter charge	Q_{ge}			7		nC
Gate-collector charge	Q_{gc}			22		nC
Turn-on delay time	$t_{d(on)}$	$V_{CC} = 200$ V, $I_C = 40$ A, $RL \approx 5 \Omega$, $V_{GE} = 15$ V		65		ns
Rise time	t_r			400		ns
Turn-off delay time	$t_{d(off)}$			185		ns
Fall time	t_f			175	260	ns

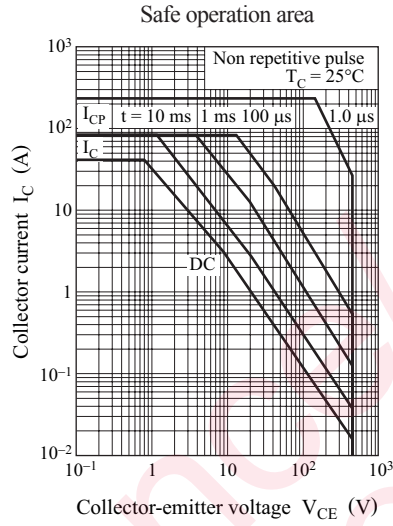
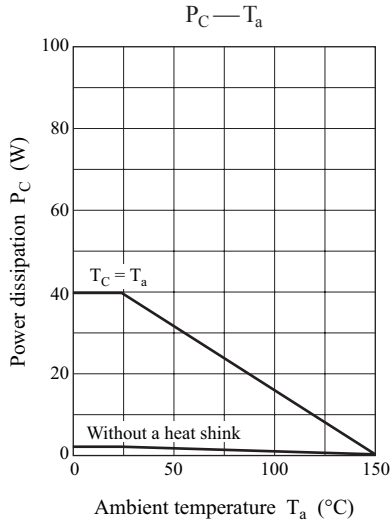
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
 2. *: I_{CES} is 100% tested according to the I_{CES} inspection standards. ($< 1.0 \mu\text{A}$ under the conditions of $V_{CE} = 344$ V, $V_{GE} = 0$)

■ Package

- Code
TO-220D-A1
- Marking Symbol: 2PG006
- Pin Name
 1. Gate
 2. Collector
 3. Emitter

■ Internal Connection





Maintenance/Discontinued

Maintenance/Discontinued includes following four Product lifecycle stage.

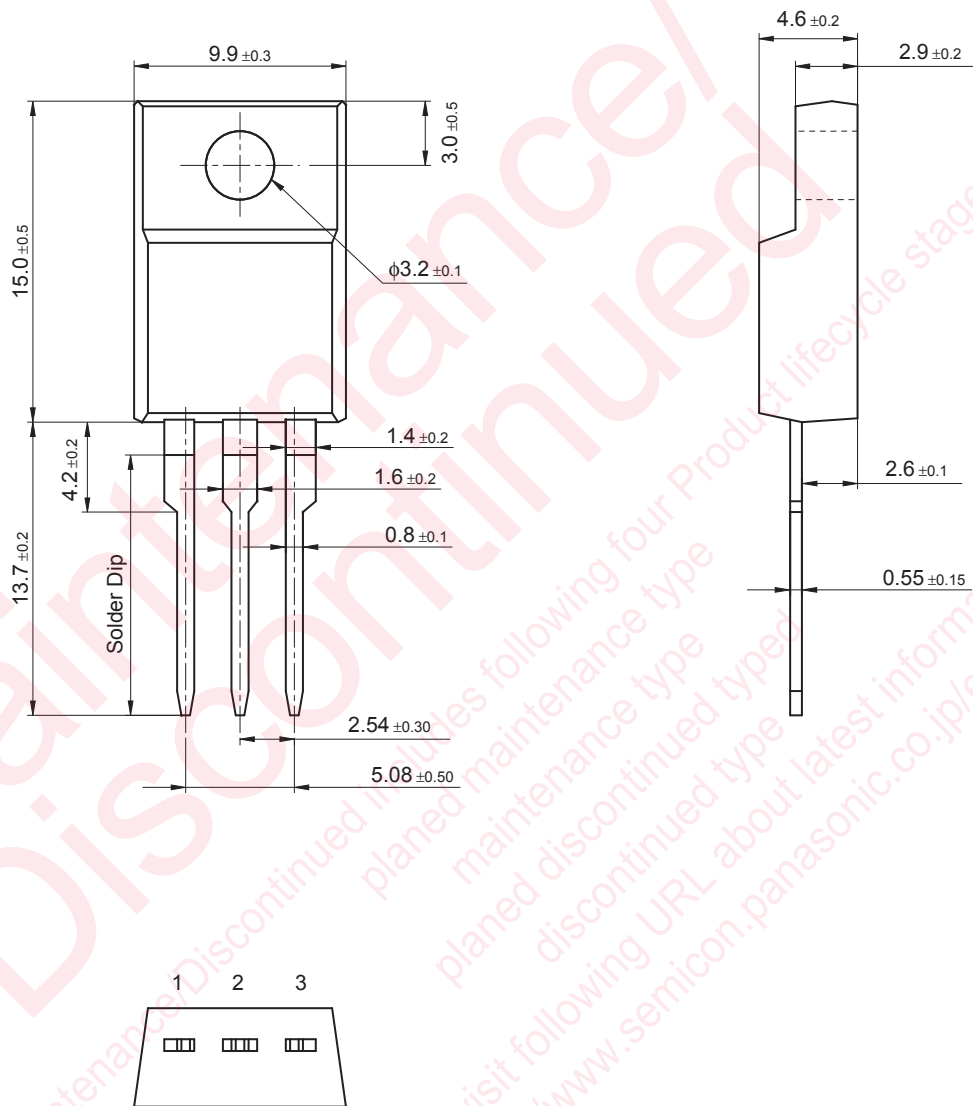
- planned maintenance type
- planned discontinued type
- discontinued type

Please visit following URL about latest information.

<http://www.semicon.panasonic.co.jp/en/>

TO-220D-A1

Unit: mm



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