FUJI Power Supply Control IC

FA3687V

Application Note

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Fuji Electric Co., Ltd.
Matsumoto Factory

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• Emergency equipment for responding to disasters and anti-burglary devices • Safety devices

6. Do not use products in this Data Book for the equipment requiring strict reliability such as (without limitation)
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• Submarine repeater equipment • Medical equipment

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CONTENTS

Note

- Parts tolerance and characteristics are not defined in all application described in this Data book. When design an actual circuit for a product, you must determine parts tolerances and characteristics for safe and stable operation.

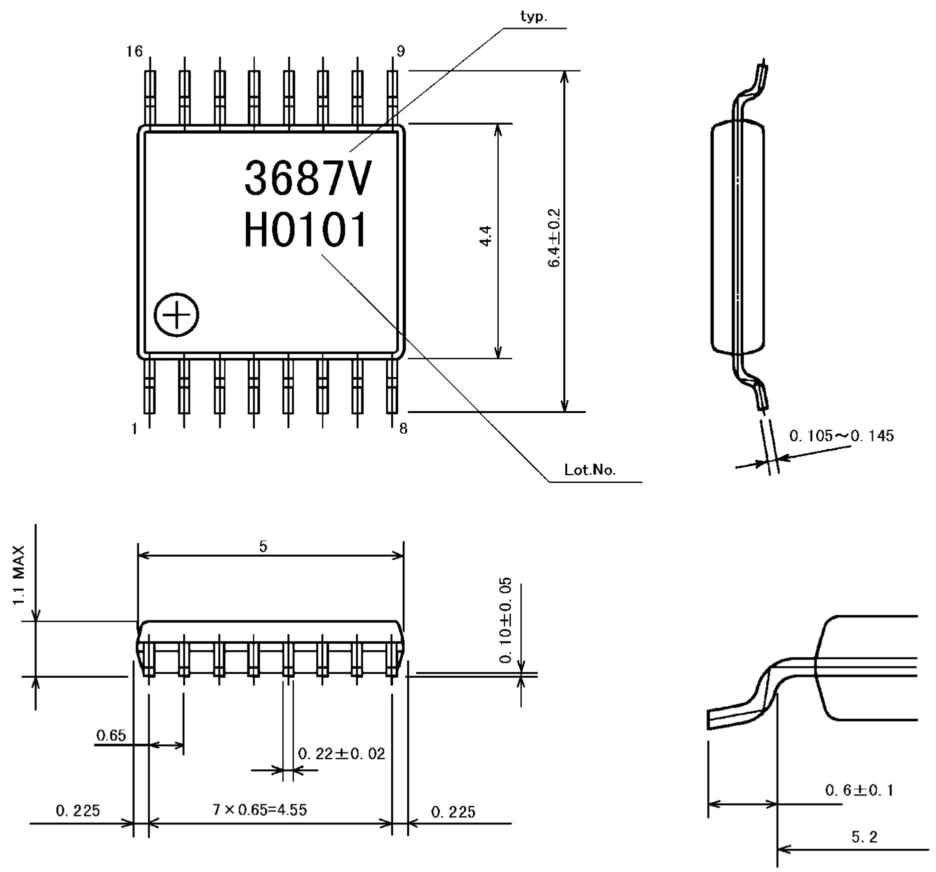
1. Description

FA3687V is a PWM type DC-to-DC converter control IC with 2ch outputs that can directly drive power MOSFETs. CMOS devices with high breakdown voltage are used in this IC and low power consumption is achieved. This IC is suitable for very small DC-to-DC converters because of their small and thin package (1.1mm max.), and high frequency operation (to 1.5MHz). You can select Pch or Nch of MOSFETs driven, and design any topology of DC-to-DC converter circuit like a buck, a boost, a inverting, a fly-back, or a forward.

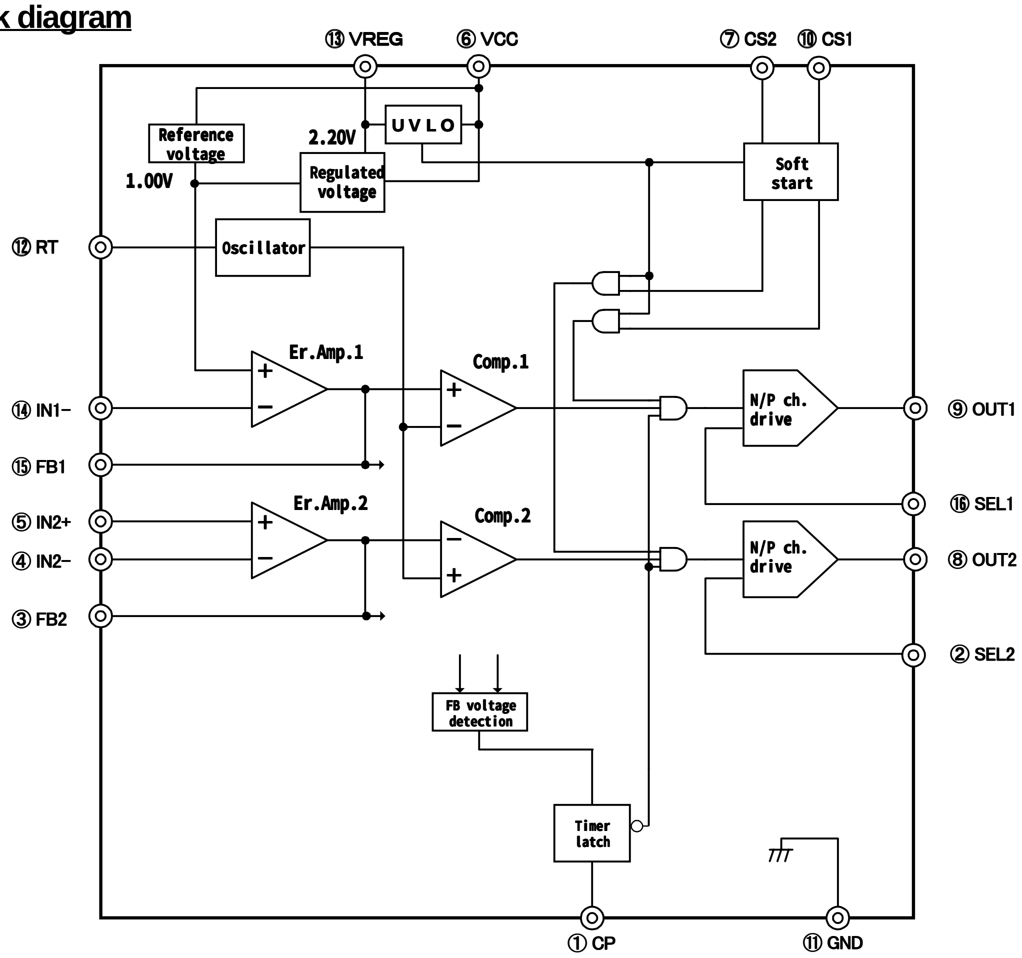
2. Features

- Wide range of supply voltage: V_{CC}=2.5 to 20V
- MOSFET direct driving
- Selectable output stage for Pch/Nch MOSFET on each channel
- Low operating current by CMOS process: 2.5mA (typ.)
- 2ch PWM control IC
- High frequency operation: 300kHz to 1.5MHz
- Simple setting of operation frequency by timing resistor
- Soft start function at each channel
- Adjustable maximum duty cycle at each channel
- Built-in undervoltage lockout
- High accuracy reference voltage: V_{REF}: 1.00V±1%, V_{REG}: 2.20V±1%
- Adjustable built-in timer latch for short-circuit protection
- Thin and small package: TSSOP-16

3. Outline



4. Block diagram



5. Pin assignment

Pin No.	Pin symbol	Description
1	CP	Timer latched short circuit protection
2	SEL2	Selection of type of driven MOSFET (OUT2)
3	FB2	Ch.2 output of error amplifier
4	IN2-	Ch.2 inverting input to error amplifier
5	IN2+	Ch.2 non-inverting input to error amplifier
6	VCC	Power supply
7	CS2	Soft start for Ch.2
8	OUT2	Ch.2 output
9	OUT1	Ch.1 output
10	CS1	Soft start for Ch.1
11	GND	Ground
12	RT	Oscillator timing resistor
13	VREG	Regulated voltage output
14	IN1-	Ch.1 inverting input to error amplifier
15	FB1	Ch.1 output of error amplifier
16	SEL1	Selection of type of driven MOSFET (OUT1)

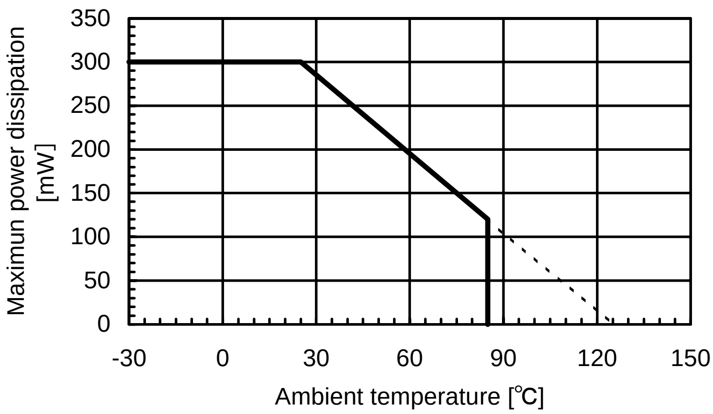
6. Ratings and characteristics

(1) Absolute maximum ratings

Item	Symbol	Test condition	rating	Unit
Power supply voltage	V_{CC}		20	V
SEL1･SEL2 pin voltage	V_{SEL}		-0.3 to 5.0	V
FB1･IN1-･FB2･IN2-･IN2+ pin voltage	V_{EA_IN}		-0.3 to 5.0	V
CS1･CS2･CP･RT･VREG pin voltage	V_{CTR_IN}		-0.3 to 5.0	V
OUT1/2 OUT pin source current	I_{OUT-}		-400(peak)	mA
OUT pin sink current	I_{OUT+}		150(peak)	mA
OUT1/2 OUT pin source current	I_{OUT-}		-50(continuous)	mA
OUT pin sink current	I_{OUT+}		50(continuous)	mA
Power dissipation ※1	P_d	Ta≦25℃	300	mW
Operating junction temperature	T_J		+125	℃
Operating ambient temperature	T_{OPR}		-30 to +85	℃
Storage temperature	T_{STG}		-40 to +125	℃

※1 Derating factor Ta≧25℃ : 3mW/℃

Maximum power dissipation curve



(2) Recommended operating conditions

Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		2.5	-	18	V
CS1･CS2･CP pin voltage	V_{CTR_IN}		0.0	-	2.5	V
SEL1･SEL2 pin voltage	V_{SEL_IN}		0.0	-	2.5	V
IN1-･IN2-･IN2+ pin voltage	V_{EA_IN}		0.0	-	2.5	V
Oscillation frequency	f_{OSC}		300	500	1500	kHz
VREG pin capacitance	C_{REG}	Vcc＜10V	0.1	1.0	4.7	μF
		10V≦Vcc＜18V	0.47	1.0	4.7	μF
VREG pin current	I_{REG}		-	-	1.0	mA
VCC pin capacitance	C_{VCC}		1.0	-	-	μF
CS1 pin capacitance	C_{CS1}	Between CS1 and GND	0.01	-	-	μF
CS2 pin capacitance	C_{CS2}	Between CS2 and VREG	0.01	-	-	μF
CP pin capacitance	C_{CP}	Between CP and VREG ※2	０．０１	—	—	μF

※2. If the timer latched mode is not needed, connect the CP pin to GND.

(3) Electrical characteristics

* The characteristics is based on the condition of V_{CC}=3.3V, C_{REG}=1.0μF, R_T=12kΩ, Ta=+25°C, unless otherwise specified.

(1) Regulated voltage for internal control blocks (VREG pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Regulated voltage	V_{REG}		2.178	2.200	2.222	V
Line regulation	V_{REG_LINE}	V_{CC}=2.5 to 18V	—	±5	±15	mV
Load regulation	V_{REG_LOAD}	I_{REG}=0 to 1mA	-5	-1		mV
Variation with temperature	V_{REG_TC}	Ta=-30 to +85°C		±0.5		%

(2) Oscillator section (RT pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{OSC}		435	500	565	kHz
Line regulation	f_{OSC_LINE}	V_{CC}=2.5 to 18V	—	±1	±5	%
Variation with temperature	f_{OSC_TC1}	Ta=-30 to +85°C		±3		%

(3) Error Amplifier section (IN1-・FB1・IN2-・IN2+・FB2 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Reference voltage (ch.1)	V_{REF1}	※3	0.99	1.00	1.01	V
V_{REF1} Line regulation (ch.1)	V_{REF_LINE}	V_{CC}=2.5 to 18V	—	±2	±5	mV
V_{REF1}Variation with temperature (ch.1)	V_{REF_TC1}	Ta=-30 to +85°C		±0.5		%
Input offset voltage (ch.2)	V_{OFFSET}	V_{IN2+}=1.0V, IN2+・IN2-	—	—	±10	mV
V_{OFFSET} Line regulation (ch.2)	V_{OFF_LINE}	V_{CC}=2.5～18V		0		mV
Input bias current	I_{IN-}	V_{INx-}=0.0 to 2.5V		0.0		mA
Common mode input voltage	V_{COM}	IN2+・IN2-	0.7		1.5	V
Open loop gain	A_{VO}			70		dB
Unity gain bandwidth	f_T			1.5		MHz
Output current (sink)	I_{SIFB}	V_{FB1}=0.5V,V_{IN1-}=V_{REG} V_{FB2}=0.5V,V_{IN2-}=V_{REG},V_{IN2+}=1V	2.3	3.5	4.7	mA
Output current (source)	I_{SOFB}	V_{FB1}=V_{REG}-0.5V,V_{IN1-}=0V V_{FB2}=V_{REG}-0.5V,V_{IN2-}=0V,V_{IN2+}=1V	-360	-270	-180	μA

* 3: The FB1 voltage is measured under the condition that IN1- pin and FB1 pin are shorted. The input offset voltage of the error amplifier is included.

(4) Soft start section (CS1･CS2 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Threshold voltage (CS1) (Driving Nch-MOSFET)	V_{CS1D0N}	Duty cycle=0%, V_{FB1}=1.4V		0.82		V
	$V_{CS1D20N}$	Duty cycle =20%, V_{FB1}=1.4V	0.89	0.925	0.96	V
	$V_{CS1D80N}$	Duty cycle =80%, V_{FB1}=1.4V	1.25	1.285	1.32	V
	$V_{CS1D100N}$	Duty cycle =100%, V_{FB1}=1.4V		1.38		V
Threshold voltage (CS1) (Driving Pch-MOSFET)	V_{CS1D0P}	Duty cycle =0%, V_{FB1}=1.4V		0.82		V
	$V_{CS1D20P}$	Duty cycle =20%, V_{FB1}=1.4V	0.90	0.935	0.97	V
	$V_{CS1D80P}$	Duty cycle =80%, V_{FB1}=1.4V	1.26	1.295	1.33	V
	$V_{CS1D100P}$	Duty cycle =100%, V_{FB1}=1.4V		1.38		V
Threshold voltage (CS2) (Driving Nch-MOSFET)	V_{CS2D0N}	Duty cycle =0%, V_{FB2}=0.7V		1.33		V
	$V_{CS2D20N}$	Duty cycle =20%, V_{FB2}=0.7V	1.21	1.245	1.28	V
	$V_{CS2D80N}$	Duty cycle =80%, V_{FB2}=0.7V	0.85	0.885	0.92	V
	$V_{CS2D100N}$	Duty cycle =100%, V_{FB2}=0.7V		0.80		V
Threshold voltage (CS2) (Driving Pch-MOSFET)	V_{CS2D0P}	Duty cycle =0%, V_{FB2}=0.7V		1.33		V
	$V_{CS2D20P}$	Duty cycle =20%, V_{FB2}=0.7V	1.20	1.235	1.27	V
	$V_{CS2D80P}$	Duty cycle =80%, V_{FB2}=0.7V	0.84	0.875	0.91	V
	$V_{CS2D100P}$	Duty cycle =100%, V_{FB2}=0.7V		0.80		V

(5) Pulse width modulation (PWM) section (FB1･FB2 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Threshold voltage (FB1) (Driving Nch-MOSFET)	V_{FB1D0N}	Duty cycle =0%, V_{CS1}=V_{REG}		0.82		V
	$V_{FB1D20N}$	Duty cycle =20%, V_{CS1}=V_{REG}		0.925		V
	$V_{FB1D80N}$	Duty cycle =80%, V_{CS1}=V_{REG}		1.285		V
	$V_{FB1D100N}$	Duty cycle =100%, V_{CS1}=V_{REG}		1.38		V
Threshold voltage (FB1) (Driving Pch-MOSFET)	V_{FB1D0P}	Duty cycle =0%, V_{CS1}=V_{REG}		0.82		V
	$V_{FB1D20P}$	Duty cycle =20%, V_{CS1}=V_{REG}		0.935		V
	$V_{FB1D80P}$	Duty cycle =80%, V_{CS1}=V_{REG}		1.295		V
	$V_{FB1D100P}$	Duty cycle =100%, V_{CS1}=V_{REG}		1.38		V
Threshold voltage (FB2) (Driving Nch-MOSFET)	V_{FB2D0N}	Duty cycle =0%, V_{CS2}=0V		1.33		V
	$V_{FB2D20N}$	Duty cycle =20%, V_{CS2}=0V		1.245		V
	$V_{FB2D80N}$	Duty cycle =80%, V_{CS2}=0V		0.885		V
	$V_{FB2D100N}$	Duty cycle =100%, V_{CS2}=0V		0.80		V
Threshold voltage (FB2) (Driving Pch-MOSFET)	V_{FB2D0P}	Duty cycle =0%, V_{CS2}=0V		1.33		V
	$V_{FB2D20P}$	Duty cycle =20%, V_{CS2}=0V		1.235		V
	$V_{FB2D80P}$	Duty cycle =80%, V_{CS2}=0V		0.875		V
	$V_{FB2D100P}$	Duty cycle =100%, V_{CS2}=0V		0.80		V

(6) Timer latch protection section (CP pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Threshold voltage of FB1	$V_{THFB1TL}$	※6-1	1.5	—	2.0	V
Threshold voltage of FB2	$V_{THFB2TL}$	※6-2	0.2	—	0.6	V
Threshold voltage of CS1	$V_{THFB3TL}$	※6-3	0.2	—	0.6	V
Threshold voltage of CS2	$V_{VTHCS1TL}$	※6-4	1.5	—	2.0	V
Charge current of CP	I_{CP}	V_{CP}=0.5V,V_{FB1}=2.1V	-2.4	-2.0	-1.5	μA
Threshold voltage of CP	V_{THCPTL}		1.6	—	2.1	V

(7) Under voltage lockout circuit section (VCC pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
ON threshold voltage of VCC	V_{UVLO}		2.0	2.2	2.35	V
Hysteresis voltage	ΔV_{UVLO}			0.1		V

(8) Output section (OUT1･OUT2･SEL1･SEL2 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
High side on resistance of OUT1/2	R_{ONHI}	I_{OUT2}=-50mA		10	20	Ω
		I_{OUT1}=-50mA,V_{CC}=5V		9		Ω
		I_{OUT1}=-50mA,V_{CC}=15V		8		Ω
Low side on resistance of OUT1/2	R_{ONLO}	I_{OUT1}=50mA		5	10	Ω
		I_{OUT2}=50mA,V_{CC}=5V		5		Ω
		I_{OUT2}=50mA,V_{CC}=15V		5		Ω
Rise time of OUT1/2	t_{RISE}	C_L=1000pF		25		ns
Fall time of OUT1/2	t_{FALL}	C_L=1000pF		40		ns
SEL pin voltage for driving Nch-MOSFET	V_{SELN}		0.0	—	0.2	V
SEL pin voltage for driving Pch-MOSFET	V_{SELP}		V_{REG}-0.2	—	V_{REG}	V

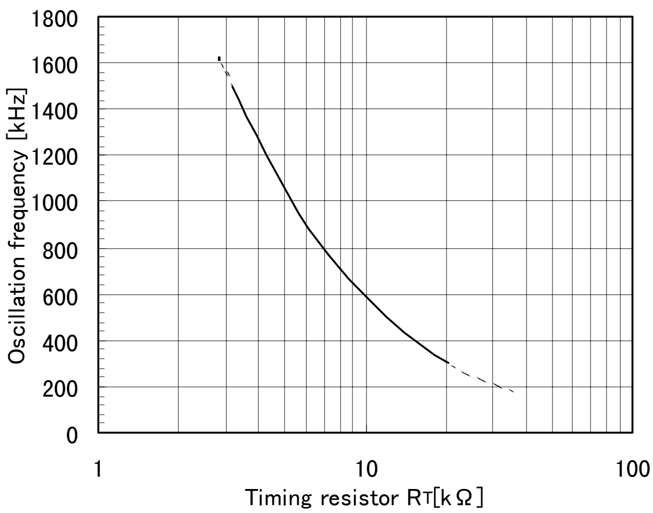
(9) Overall section						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Operating mode supply current	I_{CCA}	Ch.1, Ch.2 operating mode		2.5	3.5	mA
	I_{CCA1}	Ch.1, Ch.2 off mode		2.0		mA
	I_{CCA2}	Ch.1, Ch.2 operating mode, Vcc=18V		3.0		mA
	I_{CCA3}	Latch mode		2.0		mA

*6-1: The current source of the CP pin operates when the voltage of FB1 exceeds the threshold voltage as shown in the table.
*6-2: The current source of the CP pin operates when the voltage of FB2 falls below the threshold voltage as shown in the table.
* 6-3: The timer latch of FB1 is disabled when the CS1 voltage is below the threshold voltage as shown in the table.
* 6-4: The timer latch of FB2 is disabled when the CS2 voltage is above the threshold voltage as shown in the table.

7. Characteristic curves

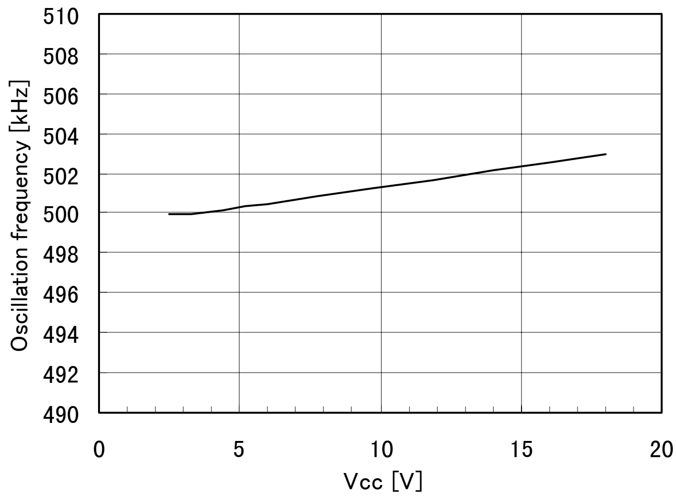
Oscillation frequency vs.Timing resistor

Vcc=3.3V,Ta=25℃



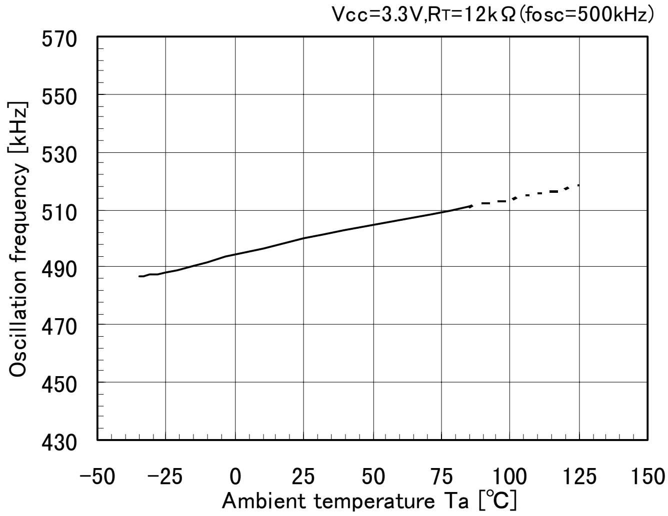
Oscillation frequency vs. Supply voltage Vcc

Ta=25℃,RT=12kΩ(fosc=500kHz)



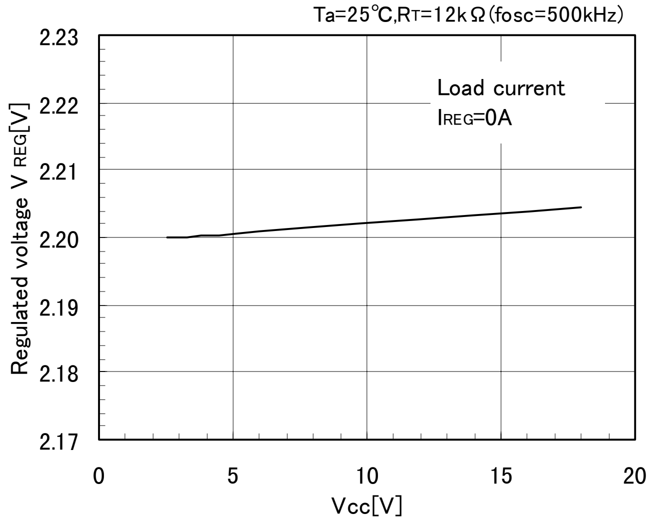
Oscillation frequency vs. ambient temperature

Vcc=3.3V,RT=12kΩ(fosc=500kHz)



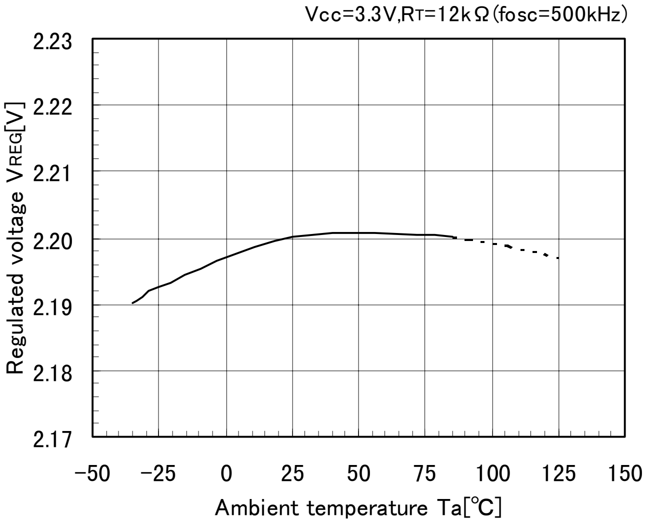
Regulated voltage vs. Supply voltage Vcc

Ta=25℃,RT=12kΩ(fosc=500kHz)



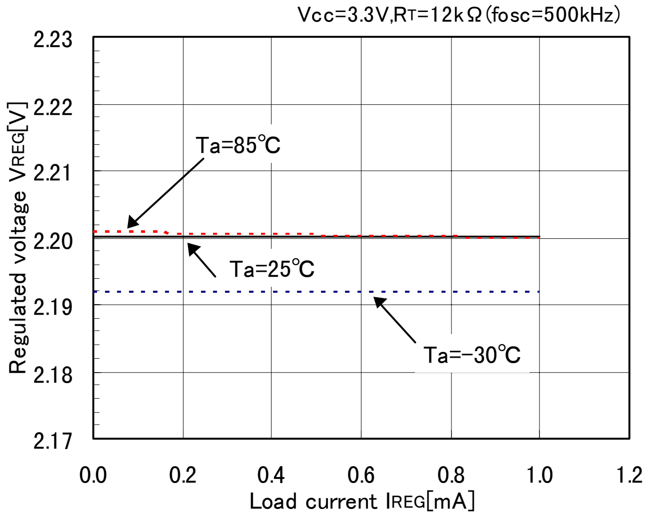
Regulated voltage vs. ambient temperature

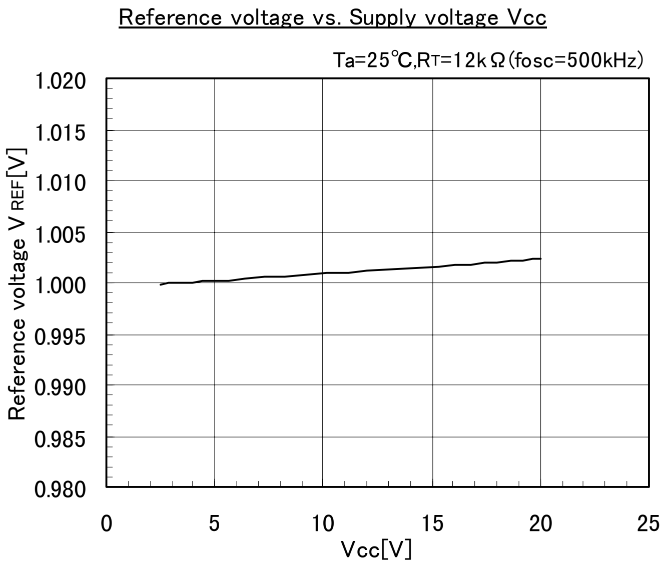
Vcc=3.3V,RT=12kΩ(fosc=500kHz)

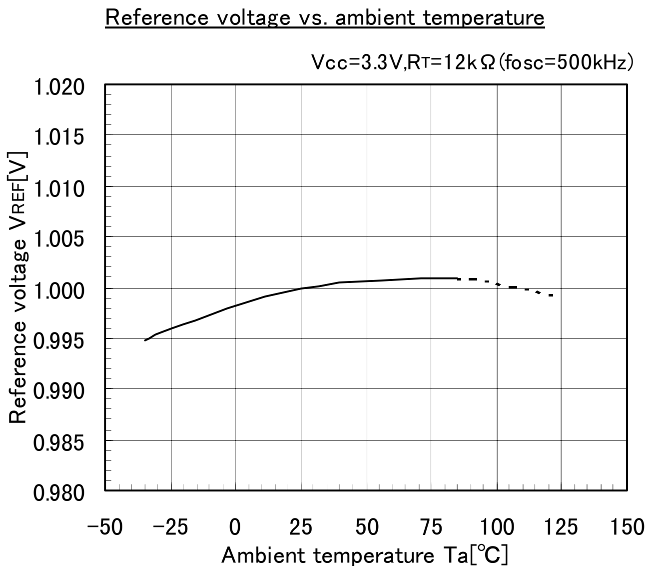


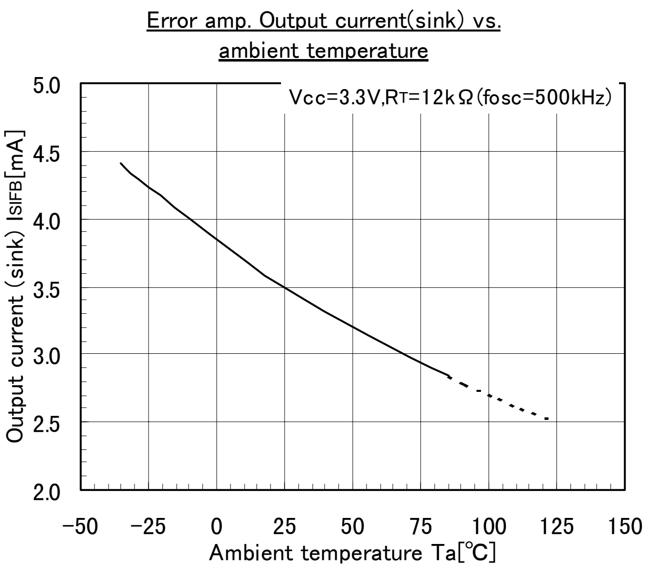
Regulated voltage vs. load current

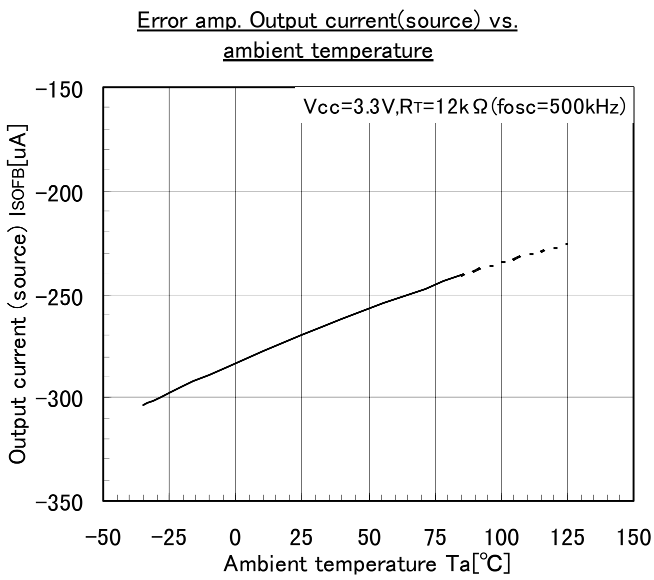
Vcc=3.3V,RT=12kΩ(fosc=500kHz)

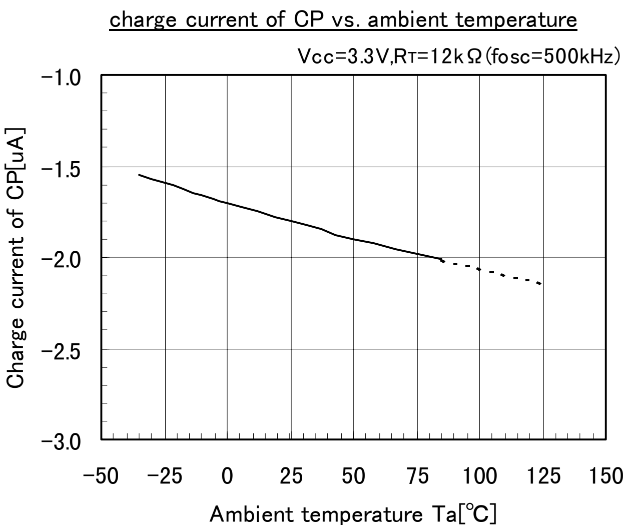


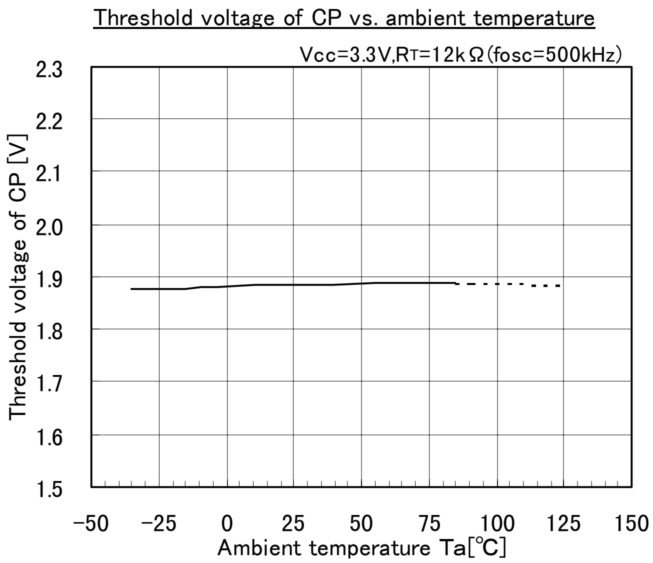

Reference voltage vs. Supply voltage Vcc
Ta=25℃,RT=12kΩ(fosc=500kHz)
Reference voltage VREF[V]
1.020
1.015
1.010
1.005
1.000
0.995
0.990
0.985
0.980
0
5
10
15
20
25
Vcc[V]


Reference voltage vs. ambient temperature
Vcc=3.3V,RT=12kΩ(fosc=500kHz)
Reference voltage VREF[V]
1.020
1.015
1.010
1.005
1.000
0.995
0.990
0.985
0.980
−50
−25
0
25
50
75
100
125
150
Ambient temperature Ta[℃]

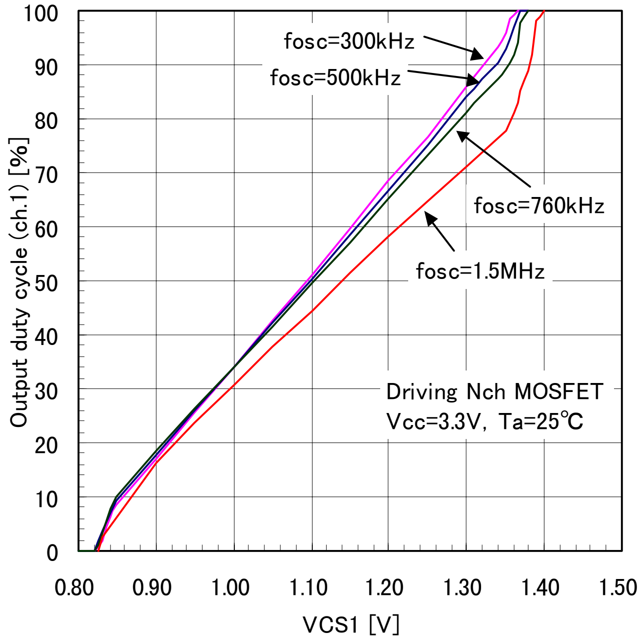

Error amp. Output current(sink) vs.
ambient temperature
Vcc=3.3V,RT=12kΩ(fosc=500kHz)
Output current (sink) ISIFB[mA]
5.0
4.5
4.0
3.5
3.0
2.5
2.0
−50
−25
0
25
50
75
100
125
150
Ambient temperature Ta[℃]


Error amp. Output current(source) vs.
ambient temperature
Vcc=3.3V,RT=12kΩ(fosc=500kHz)
Output current (source) ISOFB[uA]
−150
−200
−250
−300
−350
−50
−25
0
25
50
75
100
125
150
Ambient temperature Ta[℃]

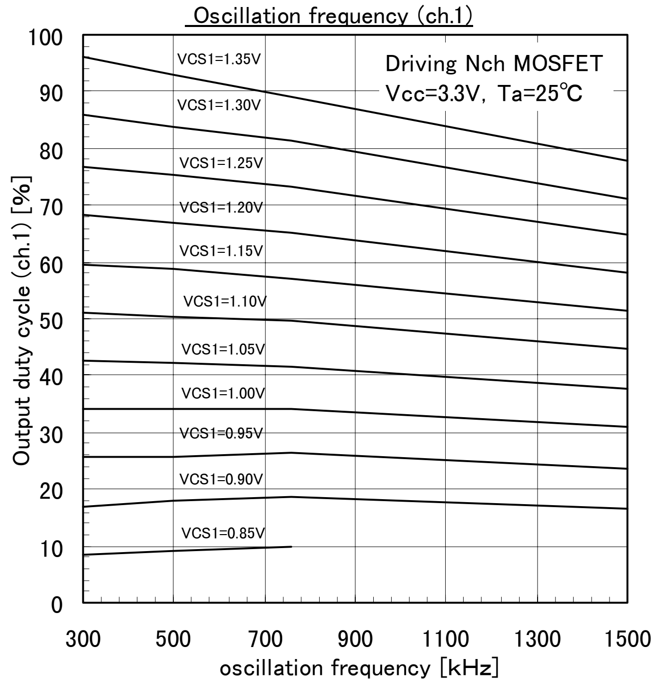

charge current of CP vs. ambient temperature
Vcc=3.3V,RT=12kΩ(fosc=500kHz)
Charge current of CP[uA]
−1.0
−1.5
−2.0
−2.5
−3.0
−50
−25
0
25
50
75
100
125
150
Ambient temperature Ta[℃]


Threshold voltage of CP vs. ambient temperature
Vcc=3.3V,RT=12kΩ(fosc=500kHz)
Threshold voltage of CP [V]
2.3
2.2
2.1
2.0
1.9
1.8
1.7
1.6
1.5
−50
−25
0
25
50
75
100
125
150
Ambient temperature Ta[℃]

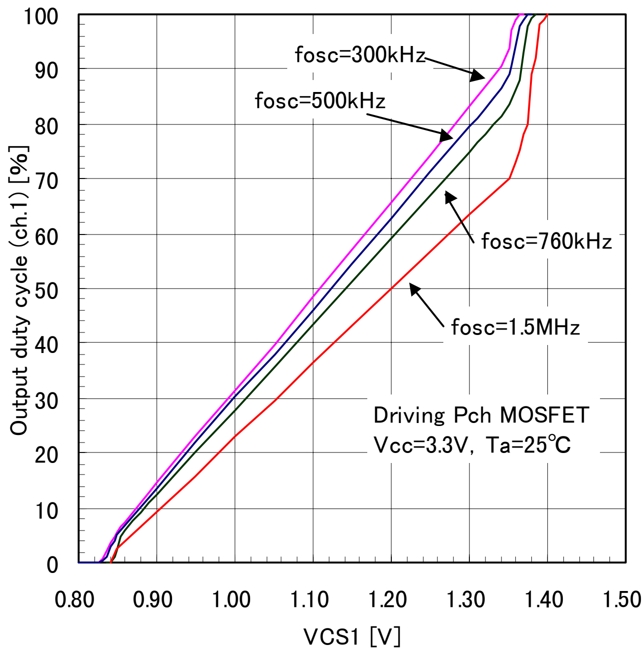
Output duty cycle vs.CS voltage (ch.1)



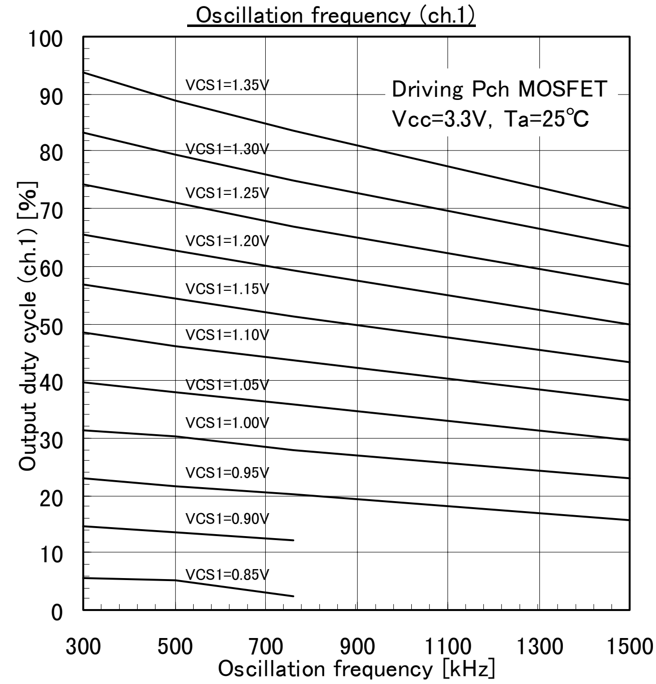
Output duty cycle vs.
Oscillation frequency (ch.1)



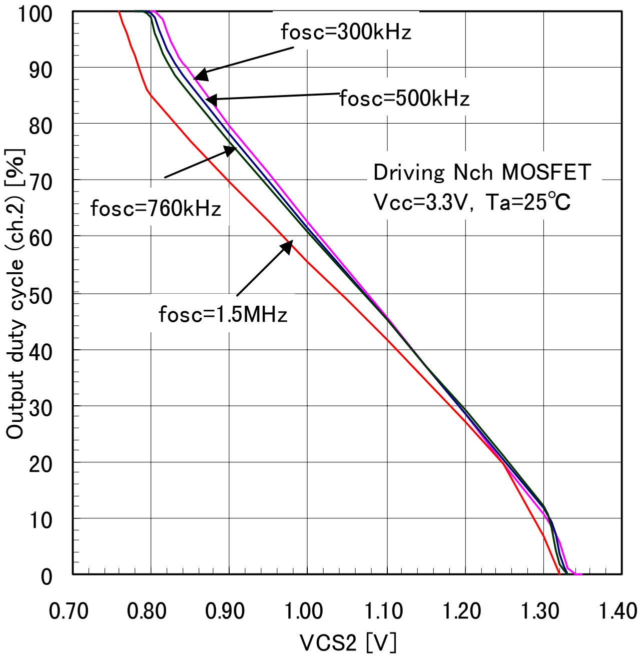
Output duty cycle vs.CS voltage (ch.1)



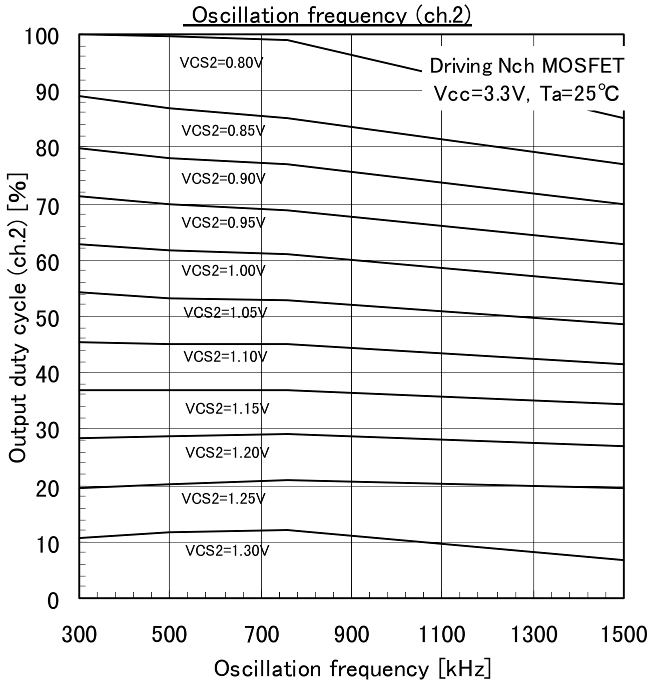
Output duty cycle vs.
Oscillation frequency (ch.1)



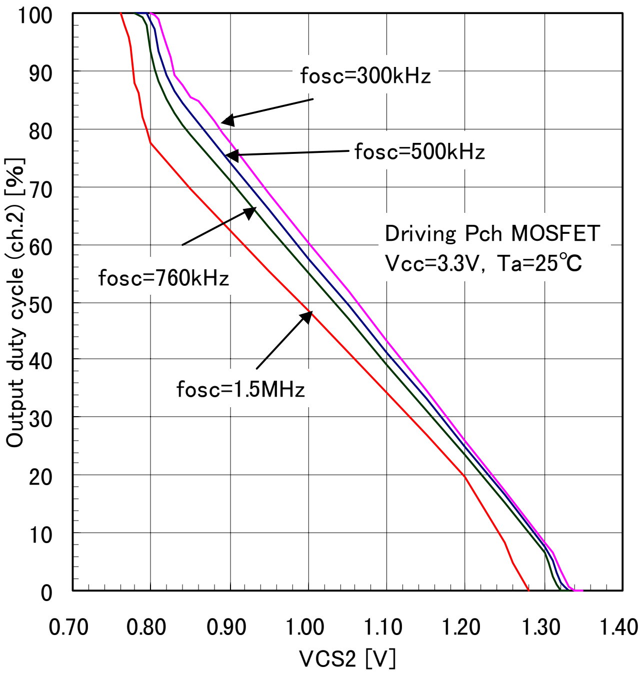
Output duty cycle vs.CS voltage (ch.2)



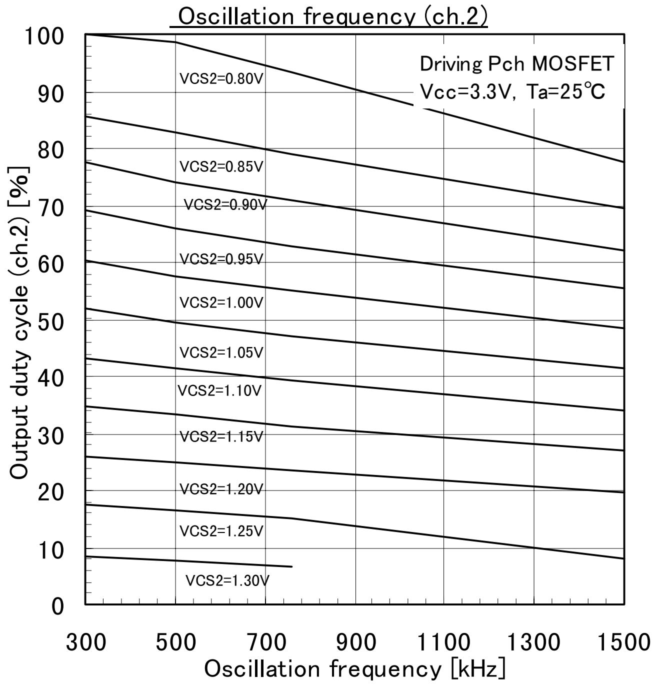
Output duty cycle vs.
Oscillation frequency (ch.2)

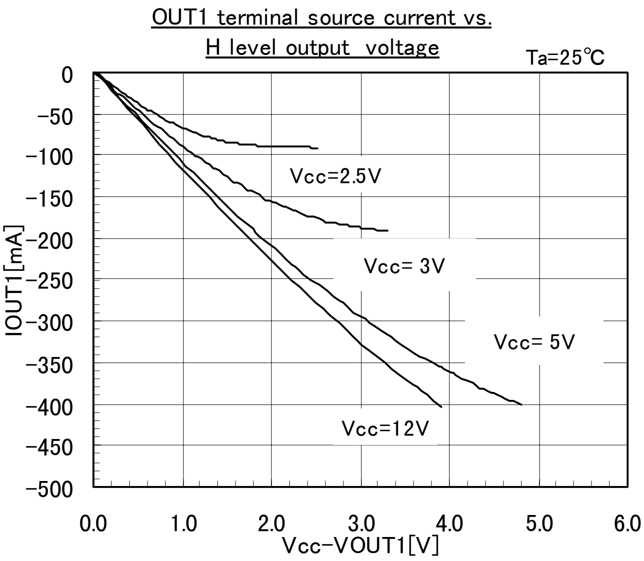


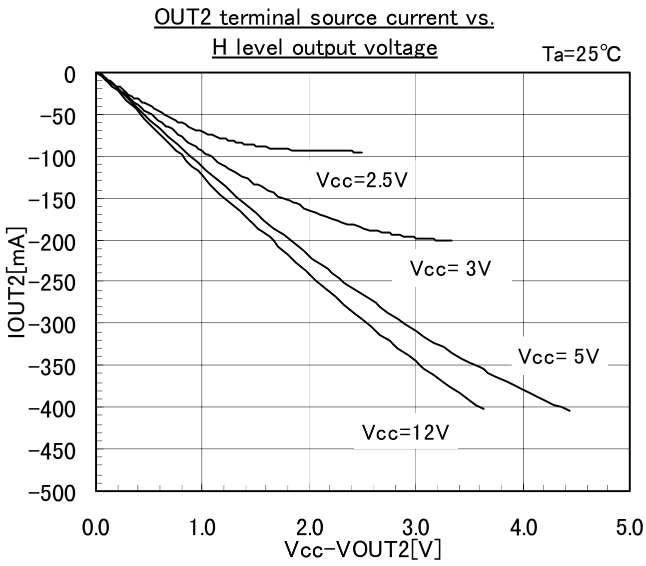
Output duty cycle vs. CS voltage (ch.2)

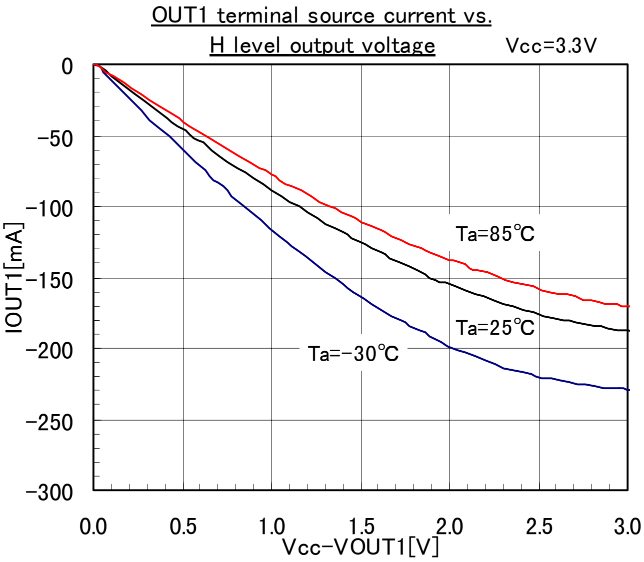


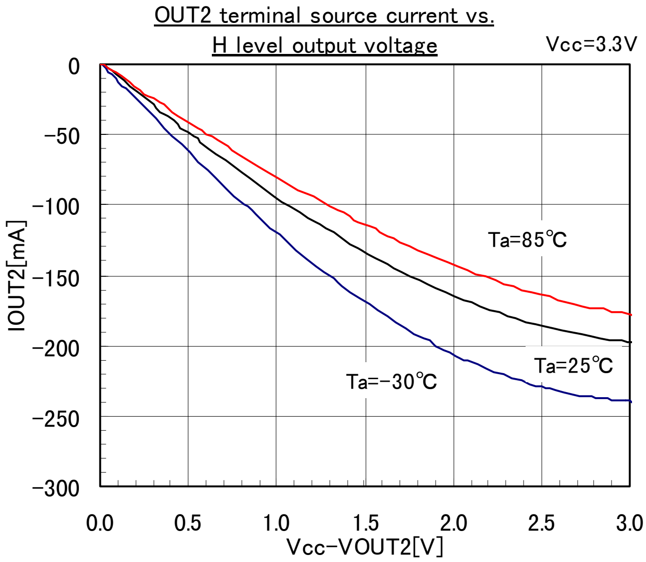
Output duty cycle vs.
Oscillation frequency (ch.2)

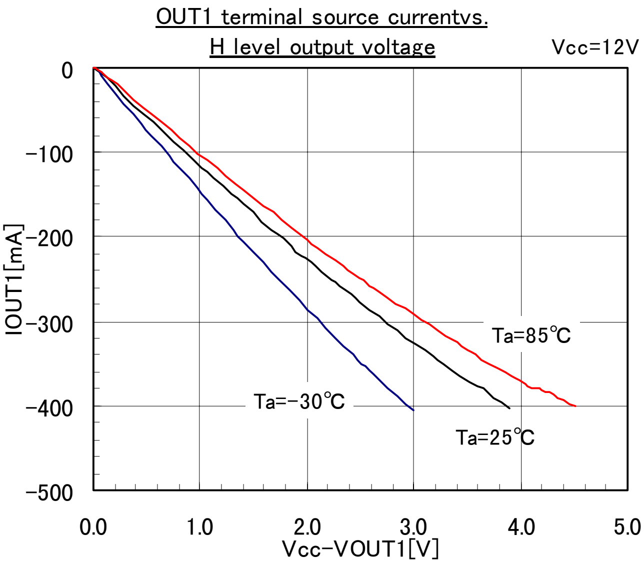


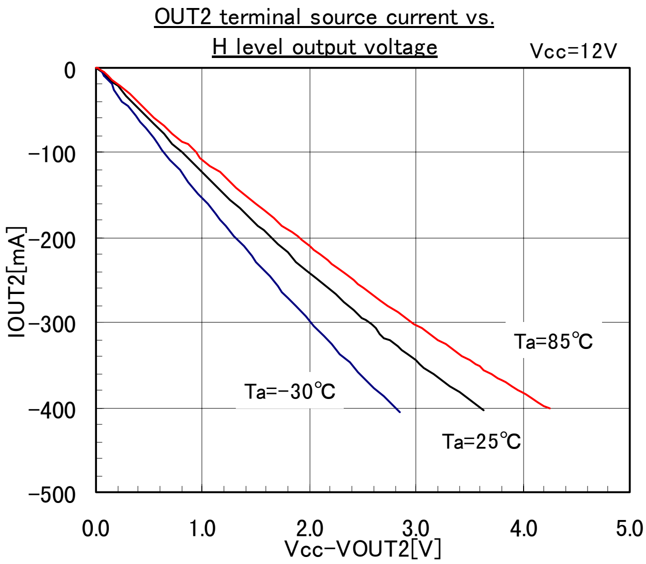

OUT1 terminal source current vs.
H level output voltage
Ta=25℃
IOUT1[mA]
Vcc-VOUT1[V]
Vcc=2.5V
Vcc= 3V
Vcc= 5V
Vcc=12V


OUT2 terminal source current vs.
H level output voltage
Ta=25℃
IOUT2[mA]
Vcc-VOUT2[V]
Vcc=2.5V
Vcc= 3V
Vcc= 5V
Vcc=12V

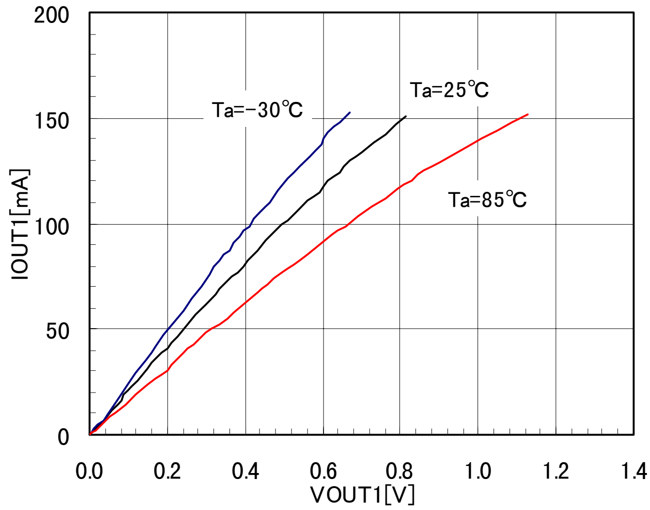

OUT1 terminal source current vs.
H level output voltage
Vcc=3.3V
IOUT1[mA]
Vcc-VOUT1[V]
Ta=85℃
Ta=25℃
Ta=-30℃


OUT2 terminal source current vs.
H level output voltage
Vcc=3.3V
IOUT2[mA]
Vcc-VOUT2[V]
Ta=85℃
Ta=25℃
Ta=-30℃

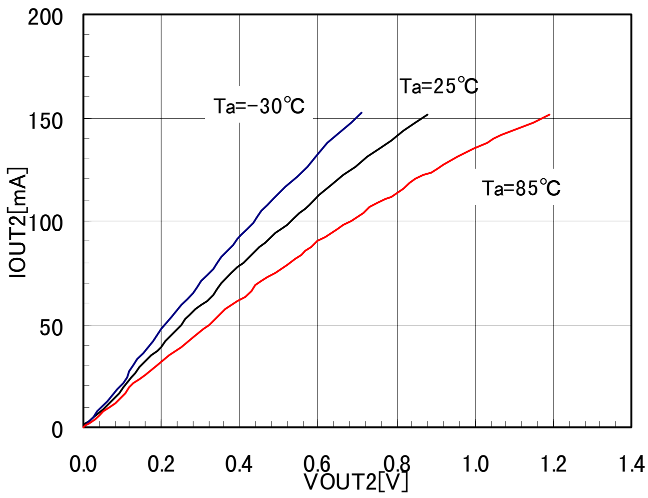

OUT1 terminal source currentvs.
H level output voltage
Vcc=12V
IOUT1[mA]
Vcc-VOUT1[V]
Ta=85℃
Ta=-30℃
Ta=25℃


OUT2 terminal source current vs.
H level output voltage
Vcc=12V
IOUT2[mA]
Vcc-VOUT2[V]
Ta=85℃
Ta=-30℃
Ta=25℃

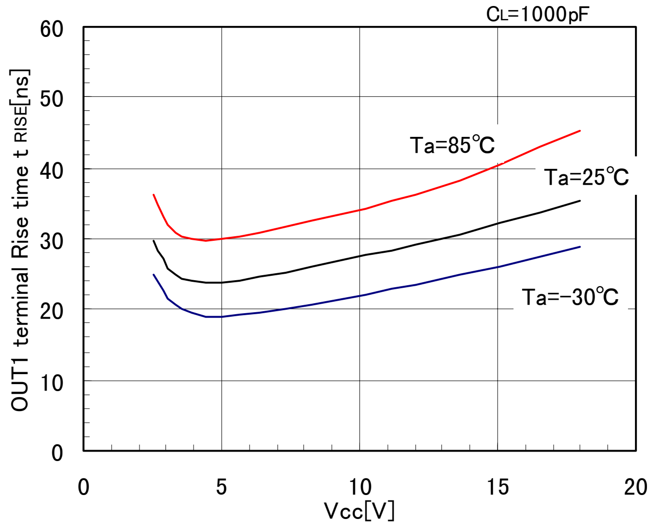
OUT1 terminal sink current vs. L level voltage



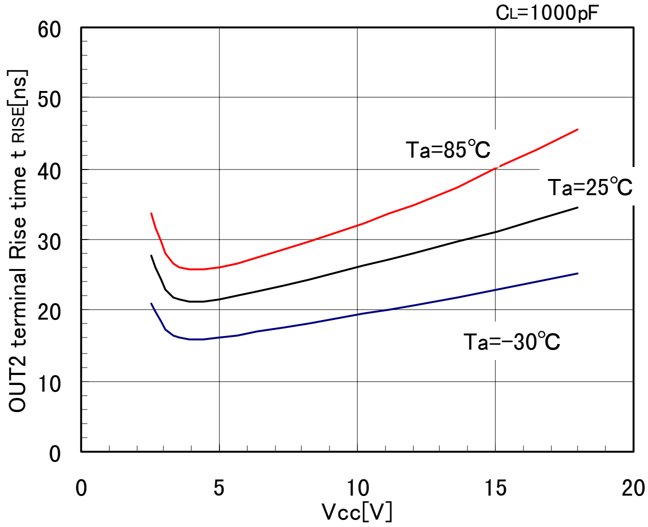
OUT2 terminal sink current vs. L level voltage



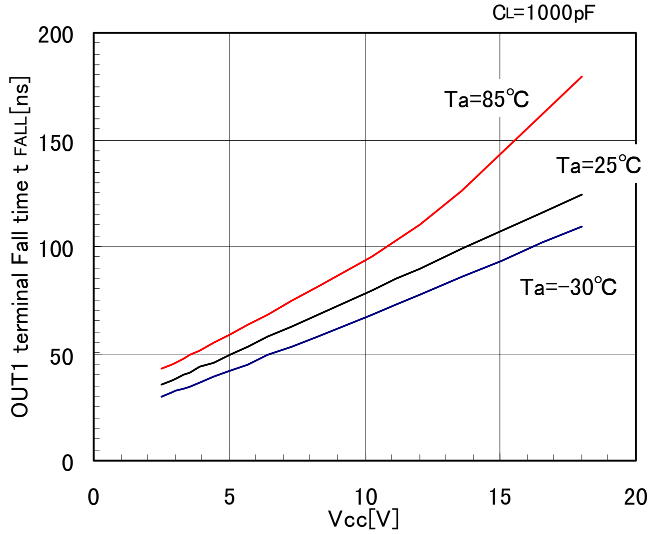
OUT1 terminal Rise time vs. Supply voltage Vcc



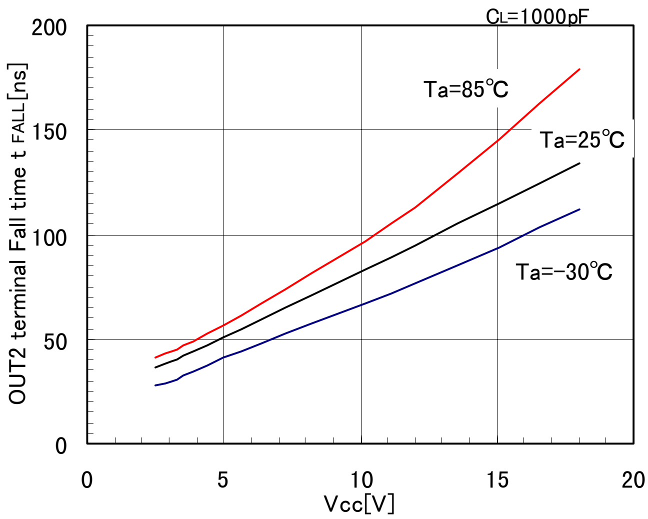
OUT2 terminal Rise time vs. Supply voltage Vcc



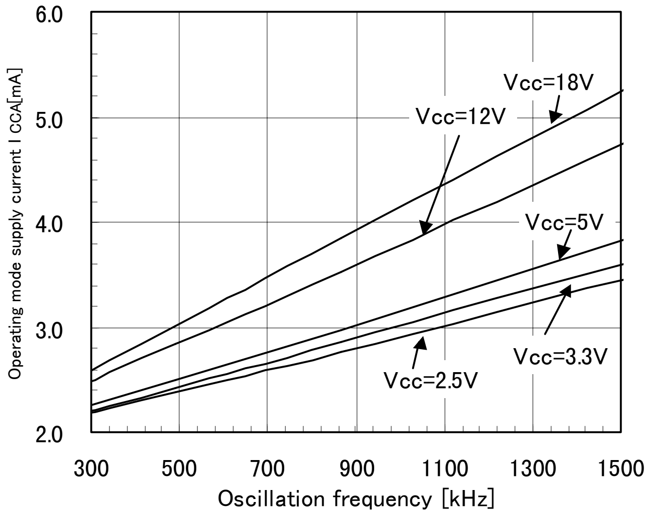
OUT1 terminal Fall time vs. Supply voltage Vcc



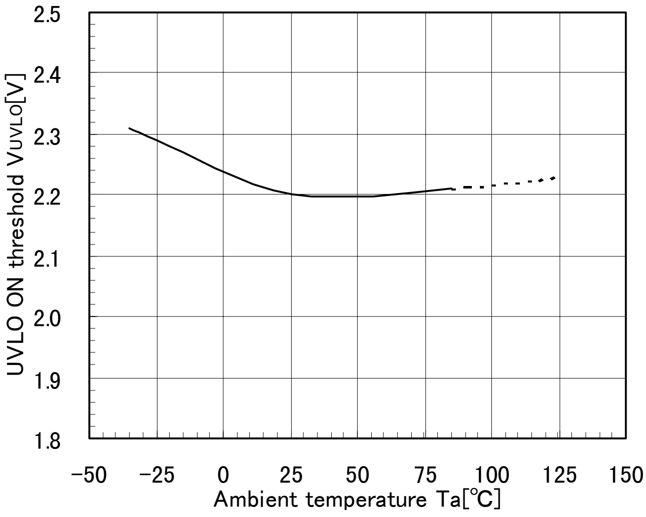
OUT2 terminal Fall time vs. Supply voltage Vcc



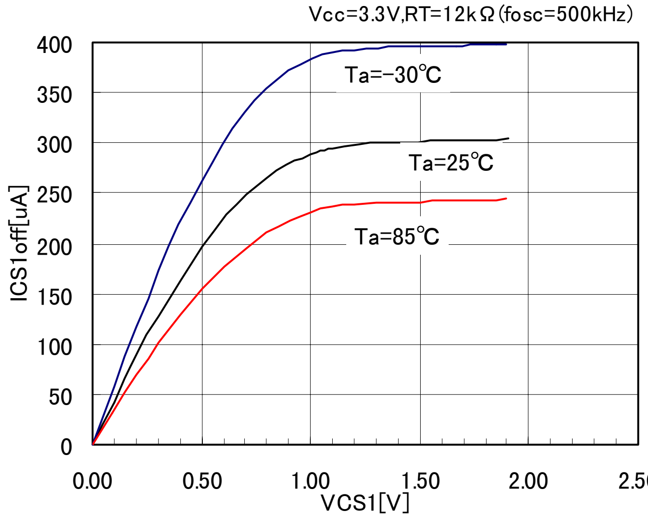
Operating mode supply current vs. Oscillation frequency



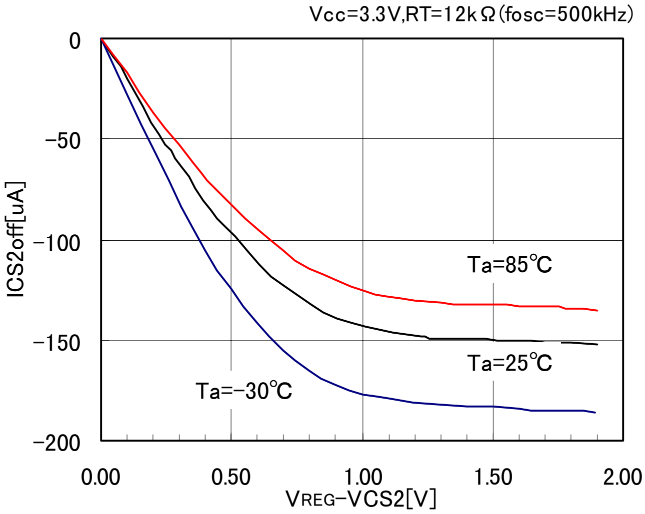
UVLO ON threshold vs. ambient temperature



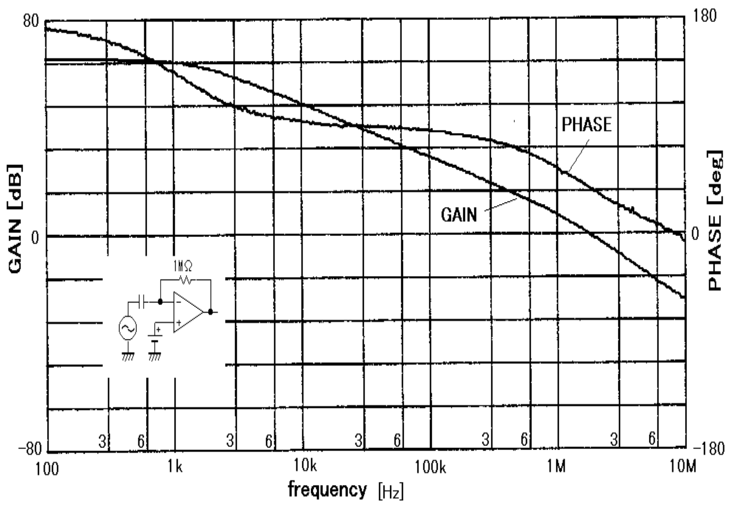
CS1 internal discharge switch current vs. voltage



CS2 internal discharge switch current vs. voltage



Error Amplifier Gain and Phase vs. frequency



8. Description of each circuit

(1) Reference voltage circuit (VREF)

This circuit generates the reference voltage of 1.00V±1% compensated in temperature from VCC voltage, and is connected to the non-inverting input of the error amplifier. The voltage cannot be observed directly because there is no external pin for this purpose.

(2) Regulated Voltage circuit (VREG)

This circuit generates 2.20V±1% based on the reference voltage VREF, and is used as the power supply of the internal IC circuits. The voltage is generated when the supply voltage, VCC, is input. The VREG voltage is also used as a regulated power supply for Soft Start, Maximum Duty cycle limitation, and others. The output current for external circuit should be within 1mA. A capacitor connected between VREG pin and GND pin is necessary to stabilize the VREG voltage (To determine capacitance, refer to Recommended operating conditions). The VREG voltage is regulated in VCC voltage of 2.4V or above.

(3) Oscillator

The oscillator generates a triangular waveform by charging and discharging the built-in capacitor. A desired oscillation frequency can be set by the value of the resistor connected to the RT pin (Fig. 1). The built-in capacitor voltage oscillates between approximately 0.82V and 1.38V at fosc=500kHz(that of ch1 and ch2 are slightly different) with almost the same charging and discharging gradients (Fig. 2). You can set the desired oscillation frequency by changing the gradients using the resistor connected to the RT pin. (Large RT: low frequency, Small RT: high frequency) The oscillator waveform cannot be observed from the outside because a pin for this purpose is not provided. The RT pin voltage is approximately 1V DC in normal operation. The oscillator output is connected to the PWM comparator.

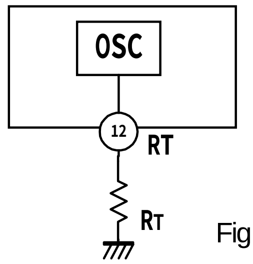


Fig.1

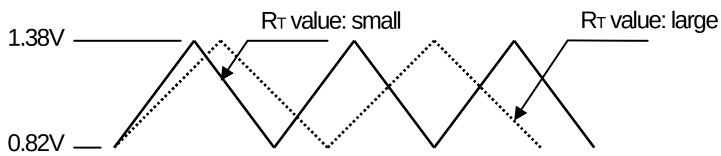


Fig.2

(4) Error Amplifier Circuit

The error amplifier 1 has the inverting input of IN1(-) pin (Pin14). The non-Inverting input is internally connected to the reference voltage VREF (1.00V±1%; 25℃). The error amplifier 2 has the inverting input IN2(-) pin (Pin4) and non-inverting input IN2(+) pin (Pin5) externally. Since each input of error amplifier 2 is connected to the pins, CH2 is suitable for any circuit topology. The FB pins (Pin3, Pin15) are the output of the error amplifier. An external RC network is connected between FB pin and IN- pin for gain and phase compensation setting. (Fig. 3) For connecting of each topology, see Design Advice.

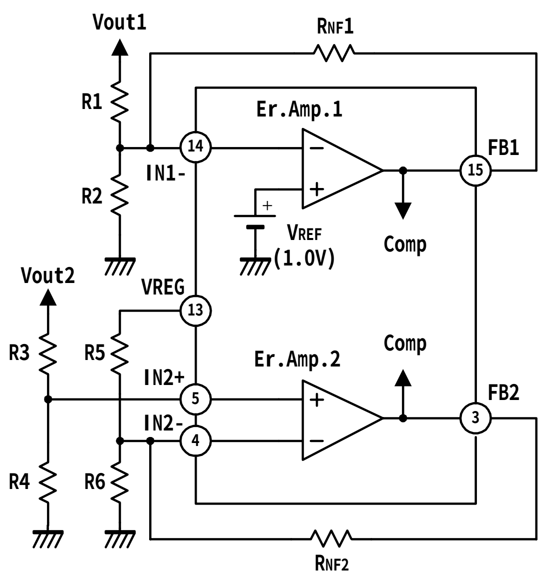


Fig.3

(5) PWM comparator

The PWM output generates from the oscillator output, the error amplifier output (FB1, FB2) and CS voltage (CS1, CS2) (Fig. 4). The oscillator output is compared with the preferred lower voltage between FB1 and CS1 for ch1. While the preferred voltage is lower than oscillator output, the PWM output is low. While the preferred voltage is higher than oscillator output, the PWM output is high. Since the phase of Ch2 is the opposite phase of Ch1, higher voltage between FB2 and CS2 is preferred and while the preferred voltage is lower than the oscillator output, the PWM output 2 is high. (Cannot be observed externally) The output polarity of OUT1, OUT2 changes according to the condition of SEL pin. (See Fig. 6)

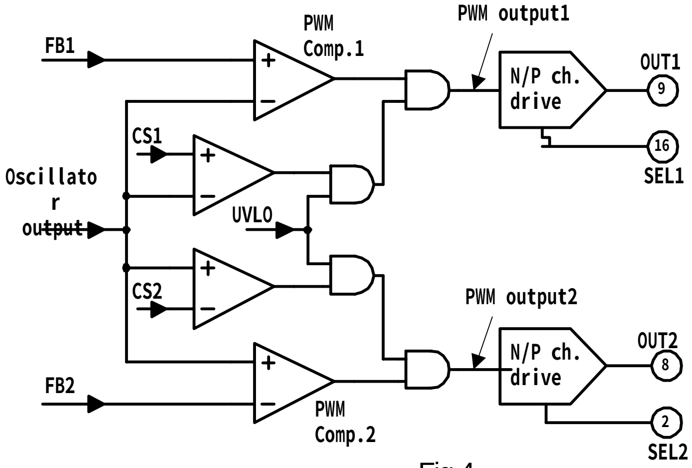


Fig.4

(6) Soft start function

This IC has a soft start function to protect DC-to-DC converter circuits from damage when starting operation. CS1 pin (Pin10), and CS2 pin (Pin7) are used for soft start function of ch1 and ch2 respectively. (Fig. 5) When the supply voltage is applied to the VCC pin and UVLO is cancelled, capacitor C_{CS1} and C_{CS2} is charged by VREG through the resistor R7 or R9. Therefore, CS1 voltage gradually increases and CS2 voltage gradually decreases. Since CS1 and CS2 pin are connected to the PWM comparator internally, the pulses gradually widen and then the soft start function operates. (Fig. 6)

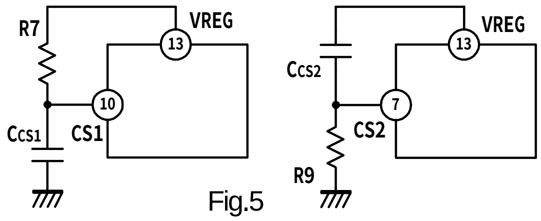


Fig.5

The maximum duty cycle can be set by using the CS pins. (See Design Advice about the detail)

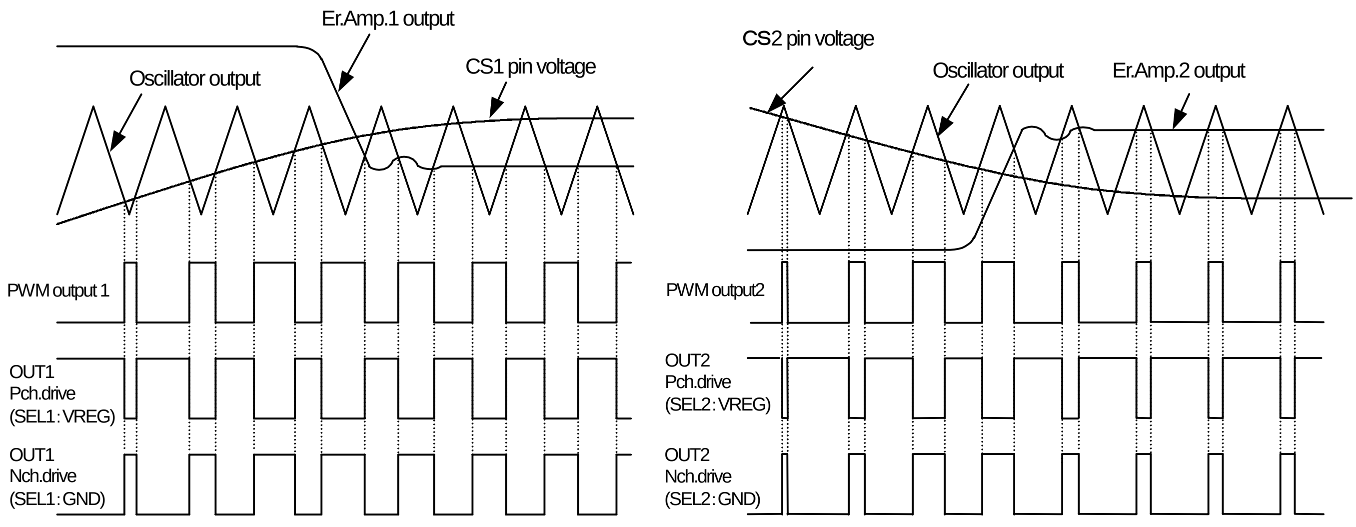


Fig.6

(7) Timer latch short-circuit protection circuit

This IC has the timer latch short-circuit protection circuit. This circuit cuts off the output of all channels when the output voltage of DC-to-DC converter drops due to short circuit or overload. To set delay time for timer latch operation, a capacitor CCP should be connected to the CP pin (Fig. 7). When one of the output voltage of the DC-to-DC converter drops due to short circuit or overload, the FB1 pin voltage increases up to around the VREG voltage for ch 1, or the FB2 pin voltage drops down to around 0 V for ch 2.When FB1 pin voltage exceeds 2.0V(max.) or FB2 pin voltage falls below 0.2V(min.), constant-current source (2 μ A typ.) starts charging the capacitor CCP connected to the CP pin. If the voltage of the CP pin exceeds 2.1 V (max.), the circuit regards the case as abnormal. Then the IC is set to off latch mode and the output of all channels is shut off, (Fig. 8) and the current consumption become 2mA(typ.) The period (tp) between the occurrence of short-circuit in the converter output and setting to off latch mode can be calculated by the following equation:

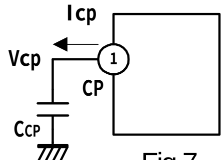


Fig.7

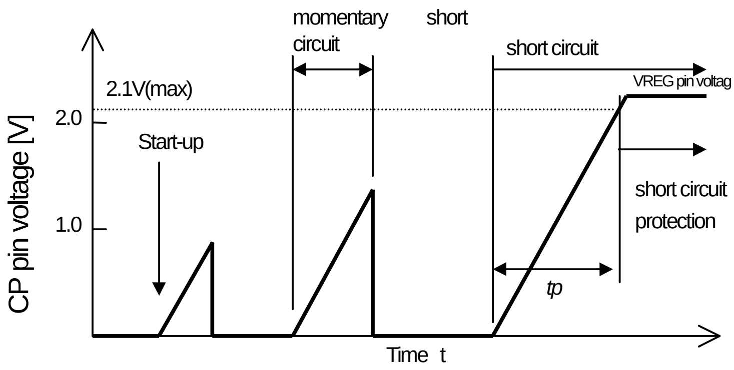


Fig.8

$$tp[s] = C_{CP} * \frac{V_{THCPTL}}{I_{CP}}$$

V_{THCPTL}: CP pin latched mode threshold voltage [V]
I_{CP}: CP charge source current [μ A]
C_{CP}: capacitance of CP pin capacitor

You can reset off latched mode of the short-circuit protection by either of the following ways about 1) CP pin, or 2) VCC pin, or 3) CS1or CS2 pin:
1) CP voltage = 0V
2) VCC voltage UVLO voltage (2.2V, typ.) or below
3) Set the CS pin of the cause of OFF latched mode as follows
CS1 pin voltage = 0V, CS2 pin voltage = VREG

If the timer-latched mode is not necessary, connect the CP pin to GND.

(8) Output circuit

The IC contains a push-pull output stage and can directly drive MOSFETs. The maximum peak current of the output stage is sink current of +150mA, and source current of - 400mA. The IC can also drive NPN and PNP transistors. The maximum current in such cases is ± 50mA. You must design the output current considering the rating of power dissipation. (See Design Advice)

You can switch the types of external discrete MOSFETs by wiring of the SEL pins (Pin 2, Pin 16). For driving Nch MOS, connect the SEL pins to GND. For driving Pch MOS, connect the SEL pins to VREG. You can design buck converter or inverting converter by driving Pch MOS, and boost converter by driving Nch MOS.

Connect them either to GND or to VREG surely.

(9) Under voltage lockout circuit

The IC contains a under voltage lockout circuit to protect the circuit from the damage caused by malfunctions when the supply voltage drops. When the supply voltage rises from 0V, the IC starts to operate at V_{CC} of 2.2V(typ.) and outputs generate pulses. If a drop of the supply voltage occurs, it stops output at V_{CC} of 2.1V(typ.). When it occurs, the CS1 pin is turned to low level and the CS2 pin to high level, and then these pins are reset.

9. Design Advice

(1) Setting the oscillation frequency

As described at Section 8-(1), “Description of Each Circuit,” a desired oscillation frequency can be determined by the value of the resistor connected to the RT pin. When designing an oscillation frequency, you can set any frequency between 300kHz and 1.5MHz. You can obtain the oscillation frequency from the characteristic curve “Oscillation frequency (fosc) vs. timing resistor resistance (R_T)” or the value can be approximately calculated by the following expression.

$$fosc = 4050 * R_T^{-0.86}$$

$$R_T = \left(\frac{4050}{fosc} \right)^{1.16}$$

fosc: oscillation frequency [kHz]
R_T: timing resistor [kΩ]

This expression, however, can be used for rough calculation, the obitained value is not guaranteed. The operation frequency varies due to the conditions such as tolerance of the characteristics of the ICs, influence of noises, or external discrete components. When determining the values, examine the effectiveness of the values in an actual circuit. The timing resistor R_T should be wired to the GND pin as shortly as possible because the RT pin is a high impedance pin and is easy affected by noises.

(2) Operation near the maximum or the minimum output duty cycle

As described in “Output duty cycle vs. voltage”, the output duty cycle of this IC changes sharply near the minimum and the maximum output duty cycle. Note that these phenomena are conspicuous for high frequency operation (when the pulse width is narrow).

(3) Determining soft start period

The period from the start of charging the capacitor C_{CS} to widening n% of output duty cycle can be roughly calculated by the following expression: (see Fig. 5 for symbols)

$$t[ms] = -R7 * C_{CS1} * \ln\left(1 - \frac{V_{CS1n}}{V_{REG}} \right)$$ for CS1 pin

$$t[ms] = -R9 * C_{CS2} * \ln\left(\frac{V_{CS2n}}{V_{REG}} \right)$$ for CS2 pin

C_{CS1}, C_{CS2}: Capacitance connected to CS1or CS2 pin [μF]
R7, R9: Resistance connected to CS1 or CS2 pin [kΩ]

V_{CS1n} and V_{CS2n} are the voltage of the CS1 and CS2 pins in n% of output duty cycle, and vary in accordance with operating frequency. The value can be obtained from the characteristic curve “Output duty cycle vs. CS voltage”

To reset the soft start function, the supply voltage VCC is lowered below the UVLO voltage (2.1V typ.) and then the internal switch discharges the CS capacitor. The characteristics of the internal switch for discharge are shown in following the characteristics curves of “Characteristics of CS1 internal discharge switch current vs. voltage” and “Characteristics of CS2 internal discharge switch current vs. voltage”. Therefore, when determining the period of soft start at restarting the power supply, consider the characteristics carefully.

(4) Setting Maximum Duty Cycle

As described in the Fig. 9, you can limit maximum duty cycle by connecting a resistor divider "R7, R8 or R9, R10" between CS1, CS2 and VREG pin. Set the maximum duty cycle considering that relation between the maximum output duty cycle and the CS pin voltage changes with operation frequency as described in the characteristics curves of "Output duty cycle vs. Oscillation frequency" and "Output duty cycle vs. CS voltage". When the maximum duty cycle is limited, CS pin voltage at start-up is described in Fig. 10, and the approximate value of soft start period can be obtained by the following expressions:

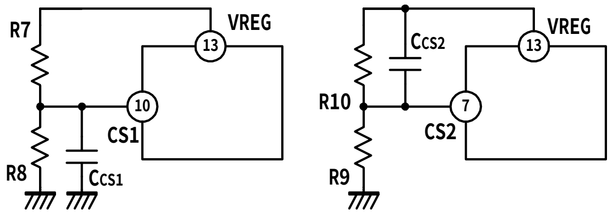
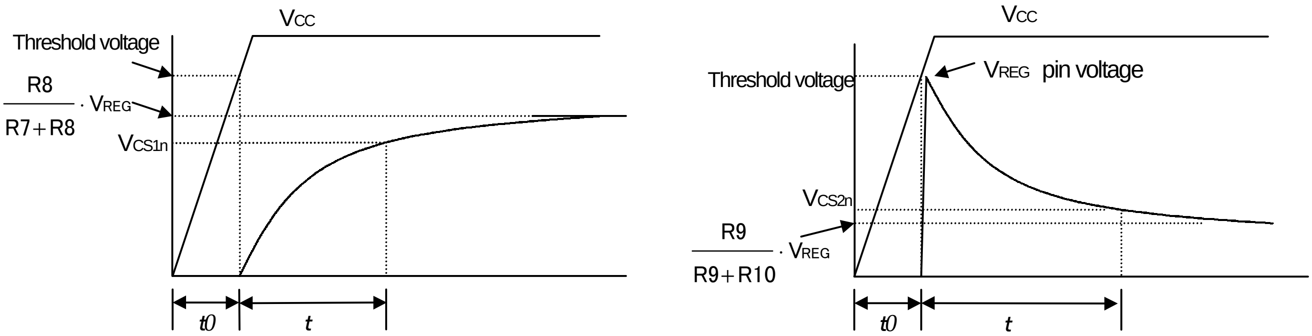


Fig.9



t0: Time from power-on of VCC to reaching unlock voltage of UVLO

Fig.10

$$t[ms] = -R_0 * C_{CS1} * \ln\left(1 - \frac{V_{CS1n}}{V_{CS1}}\right) \qquad R_0 = \frac{R7 * R8}{R7 + R8} \qquad \text{for CS1}$$

The divided CS1 voltage is obtained by:

$$V_{CS1} = \frac{R8}{R7 + R8} * V_{REG}$$

$$t[ms] = -R_0 * C_{CS2} * \ln\left(\frac{V_{CS2n} - V_{CS2}}{V_{REG} - V_{CS2}}\right) \qquad R_0 = \frac{R9 * R10}{R9 + R10} \qquad \text{for CS2}$$

The divided CS2 voltage is obtained by:

$$V_{CS2} = \frac{R9}{R9 + R10} * V_{REG}$$

C_{CS1}, C_{CS2}: Capacitance connected to the CS1 or CS2 pin [μF]
R7, R8, R9, R10: Resistance connected to CS1 or CS2 pin [kΩ]

V_{CS1n} and V_{CS2n} are the voltages of CS1 and CS2 under a certain output duty cycle and varies with operation frequencies. The values of V_{CS1n} and V_{CS2n} can be obtained from the characteristics curve of "Output duty cycle vs. CS voltage".
The charging of C_{CS1} and C_{CS2} after UVLO is unlocked.
Therefore, the period from power-on of Vcc to widening n% of output duty cycle is the sum of t0 and t

(5) Determining the output voltage of DC-DC converters

The ways to determine the output voltage of the DC-DC converter of each channel is shown in Fig. 10 and the following equations.

For ch1:
The positive output voltage of DC-to-DC converter (a buck, a boost) is determined by:

$$Vout1=\frac{R1+R2}{R2}*V_{REF}$$

For ch2:
The positive output voltage of DC-to-DC converter is determined by:

$$Vout2=V1*\frac{R3+R4}{R3}$$

Here, $V1=V_{REG}*\frac{R6}{R5+R6}$

When R5=R6,

$$Vout2=V_{REG}*\left(\frac{R3+R4}{2R3}\right)$$

The negative output voltage of DC-to-DC converter (inverting) is determined by:

$$Vout2=\frac{R3+R4}{R3}*V1-\frac{R4}{R3}*V_{REG}$$

The ratio of resistances is determined by:

$$\frac{R3}{R4}=\frac{V_{REG}-V1}{Vout2+V1}$$

(Use the absolute value of the Vout2 voltage.)

When R5=R6,

$$Vout2=V_{REG}*\left(\frac{R3-R4}{2R3}\right)$$

Connect the SEL1 and SEL2 pin to GND or VREG surely.

ch1

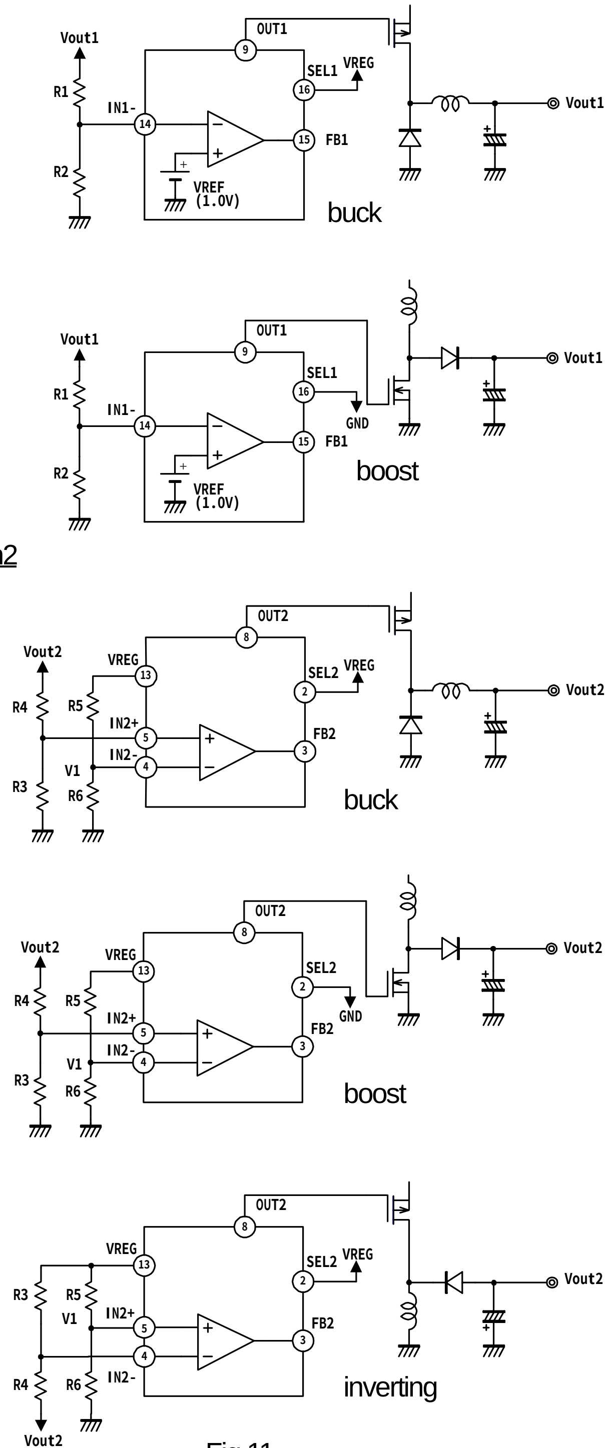


Fig.11

(6) Restriction of external discrete components and Recommended operating conditions

To achieve a stable operation of the IC, the value of external discrete components connected to VCC, VREG, CS, CP pins should be within the recommended operating conditions. And the voltage and the current applied to each pin should be also within the recommended operating conditions. If the pin voltage of OUT1, OUT2, or VREG becomes higher than the VCC pin voltage, the current flows from the pins to the VCC pin because parasitic three diode exist between the VCC pin and these pins. Be careful not to allow this current to flow.

(5) Loss Calculation

Since it is difficult to measure IC loss directly, the calculation to obtain the approximate loss of the IC connected directly to a MOSFET is described below.

When the supply voltage is V_{CC}, the current consumption of the IC is I_{CCA}, the total input gate charge of the driven MOSFET is Qg and the switching frequency is fsw, the total loss Pd of the IC can be calculated by:

$Pd \fallingdotseq V_{CC}*(I_{CCA}+Qg*fsw)$.

The value in this expression is influenced by the effects of the dependency of supply voltage, the characteristics of temperature, or the tolerance of parameter. Therefore, evaluate the appropriateness of IC loss sufficiently considering the range of values of above parameters under all conditions.

Example)

I_{CCA}=2.5mA for V_{CC}=3.3V in the case of a typical IC from the characteristics curve. Qg=6nC, fsw=500kHz, the IC loss "Pd" is as follows.

Pd≒3.3*(2.5mA+6nC*500kHz)≒18.2mW

if two MOSFETs are driven under the same condition for 2 channels, Pd is as follows:

Pd≒3.3*{2.5mA+2*(6nC*500kHz)}=28.1mW

10.Application circuit