FDD6685

30 V P-Channel POWERTRENCH® MOSFET

ON Semiconductor®

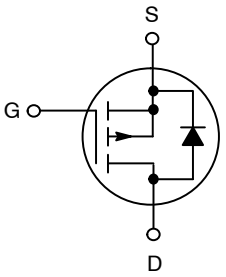
www.onsemi.com

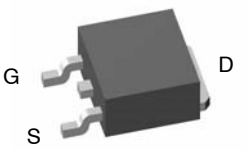
General Description

This P−Channel MOSFET is a rugged gate version of ON Semiconductor's advanced POWERTRENCH process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5 V – 2 5V).

Features

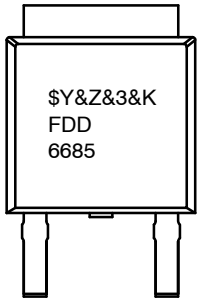
- −40 A, −30 V
  - $R_{DS(ON)}$ = 20 mΩ @ V_{GS} = −10 V
  - $R_{DS(ON)}$ = 30 mΩ @ V_{GS} = −4.5 V
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability
- Qualified to AEC Q101
- This Device is Pb−Free and are RoHS Compliant





DPAK3 (TO−252 3 LD)
CASE 369AS

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDD6685	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain−Source Voltage		−30	V
V_{GSS}	Gate−Source Voltage		±25	V
I_D	Continuous Drain Current	@T_C = 25°C (Note 5)	−40	A
		@T_A = 25°C (Note 3a)	−11	
		Pulsed, PW ≤ 100 μs (Note 3b)	−100	
P_D	Power Dissipation for Single Operation	(Note 3)	52	W
		(Note 3a)	3.8	
		(Note 3b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 3)	2.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 3a)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 3b)	96	°C/W

1. This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at http://www.aecouncil.com/
2. All ON Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Device	Reel Size	Tape Width	Quantity
FDD6685	FDD6685	13”	16 mm	2500 Units

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRAIN−SOURCE AVALANCHE RATINGS (NOTE 4)						
E_{AS}	Single Pulse Drain−Source Avalanche Energy	I_D = −11 A		42		mJ
I_{AS}	Maximum Drain−Source Avalanche Current			−11		A
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−30			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C		−24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −24 V, V_{GS} = 0 V			−1	μA
I_{GSS}	Gate−Body Leakage	V_{GS} = ±25V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−1	−1.8	−3	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate Threshold Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C		5		mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −10 V, I_D = −11 A		14	20	mΩ
		V_{GS} = −4.5 V, I_D = −9 A		21	30	
		V_{GS} = −10 V, I_D = −11 A, T_J = 125°C		20		

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ON CHARACTERISTICS						
$I_{D(on)}$	On–State Drain Current	V_{GS} = –10 V, V_{DS} = –5 V	–20			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –11 A		26		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –15 V, V_{GS} = 0 V, f = 1.0 MHz		1715		pF
C_{oss}	Output Capacitance			440		pF
C_{rss}	Reverse Transfer Capacitance			225		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		3.6		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –15 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		17	31	ns
t_r	Turn–On Rise Time			11	21	ns
$t_{d(off)}$	Turn–Off Delay Time			43	68	ns
t_f	Turn–Off Fall Time			21	34	ns
Q_g	Total Gate Charge	V_{DS} = –15V, I_D = –11 A, V_{GS} = –5 V		17	24	nC
Q_{gs}	Gate–Source Charge			9		nC
Q_{gd}	Gate–Drain Charge			4		nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –3.2 A (Note 4)		–0.8	–1.2	V
Trr	Diode Reverse Recovery Time	IF = –11 A, diF/dt = 100 A/μs		26		ns
Qrr	Diode Reverse Recovery Charge			13		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

3. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ = 40°C/W when mounted on 1in^2 pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%
5. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$
   where P_D is maximum power dissipation at T_C = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and V_{GS} = 10 V.
6. Starting T_J = 25°C, L = 0.69 mH, I_{AS} = –11 A

TYPICAL CHARACTERISTICS

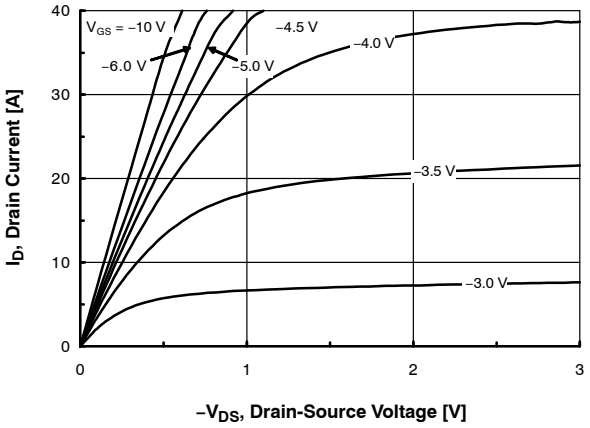


Figure 1. On-Region Characteristics

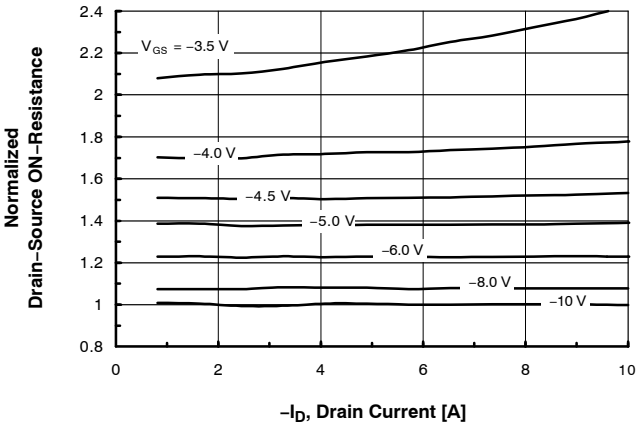


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

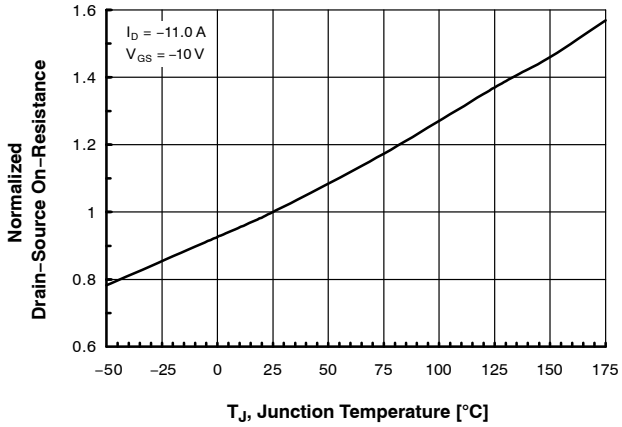


Figure 3. On-Resistance Variation with Temperature

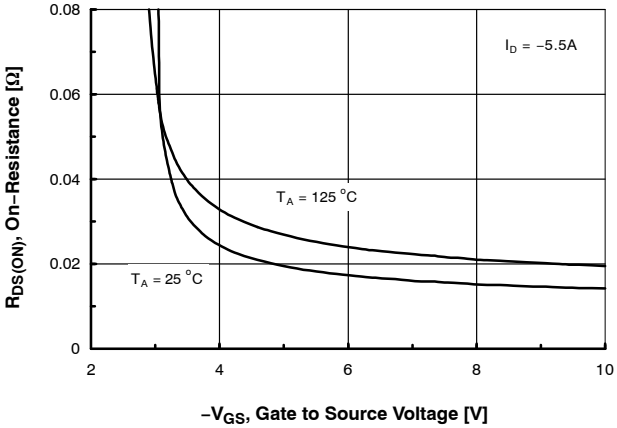


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

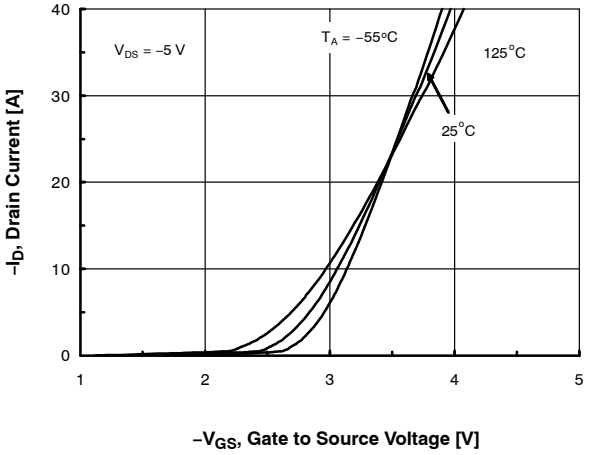


Figure 5. Transfer Characersistics

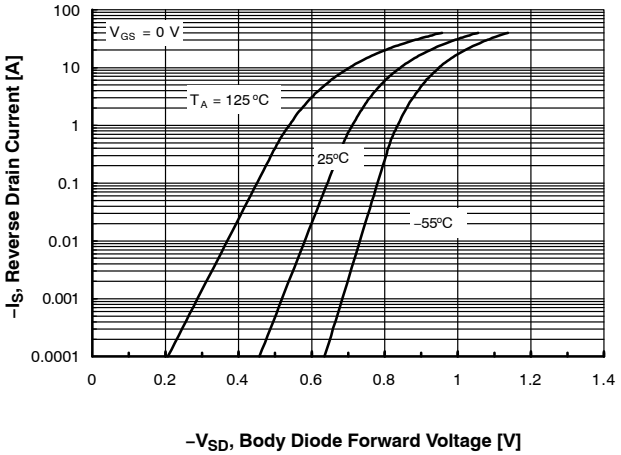


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

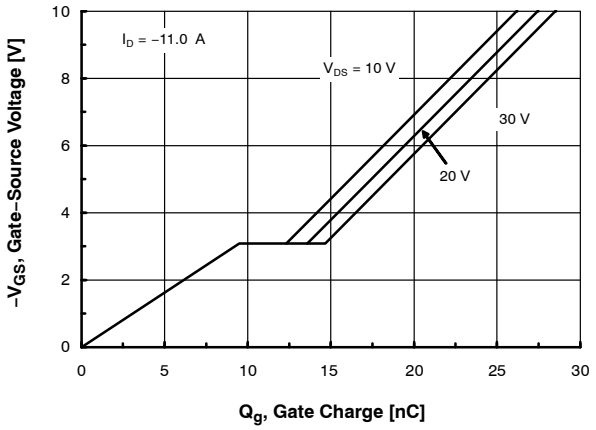


Figure 7. Gate Charge Characteristics

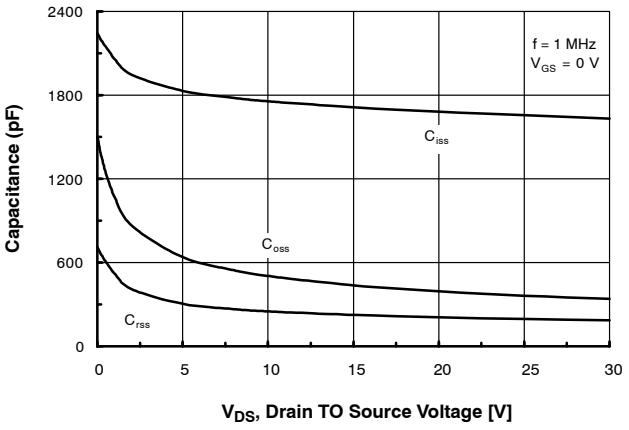


Figure 8. Capacitance Characteristics

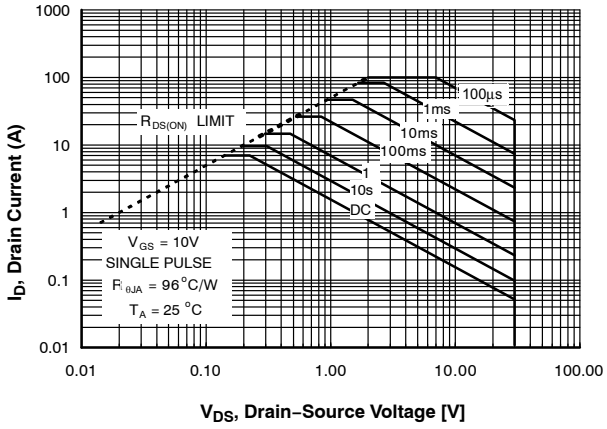


Figure 9. Maximum Safe Operating Area

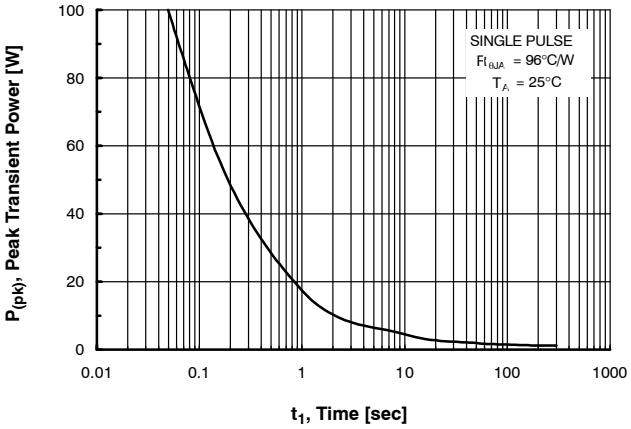


Figure 10. Single Pulse Minimum Power Dissipation

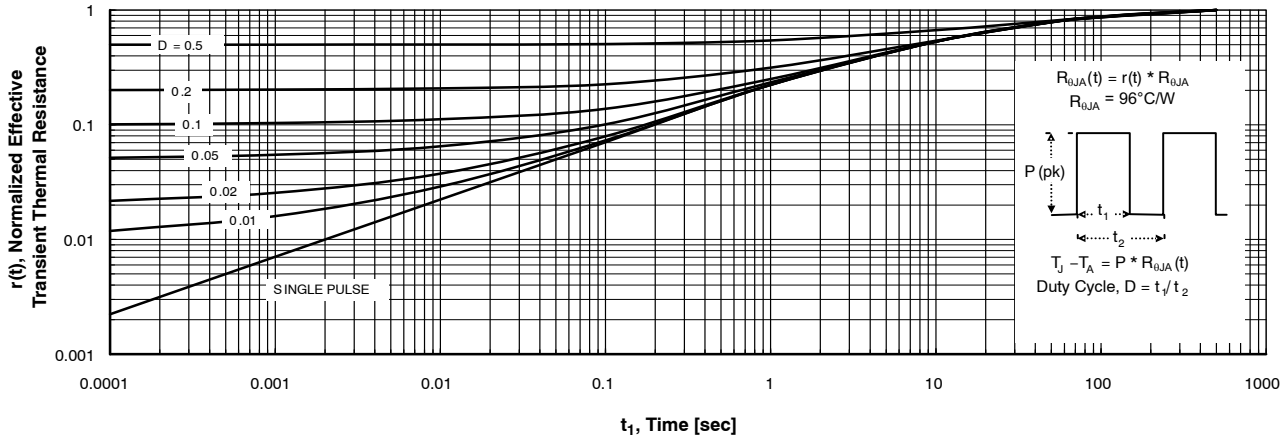
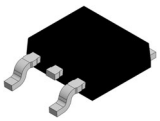


Figure 11. Transient Thermal Response Curve

NOTES:

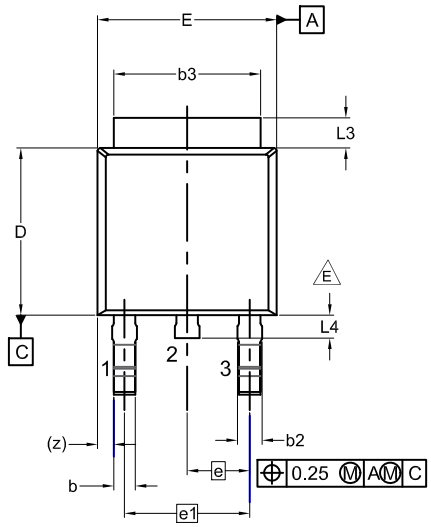
7. Thermal characterization performed using the conditions described in Note 3b.
8. Transient thermal response will change depending on the circuit board design.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

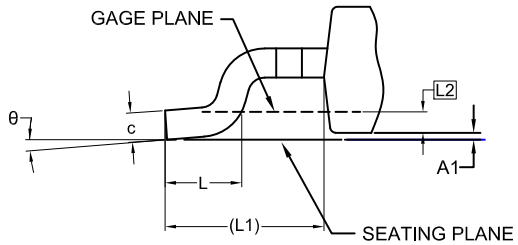


DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE A

DATE 28 SEP 2022



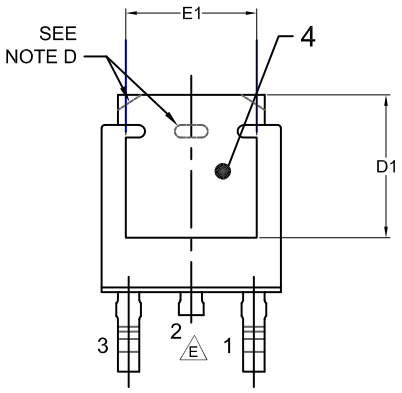
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



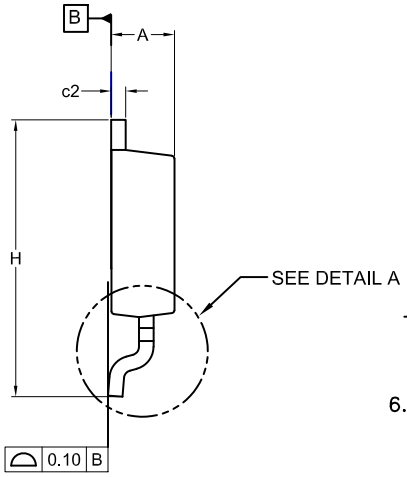
DETAIL A
(ROTATED -90°)
SCALE: 12X

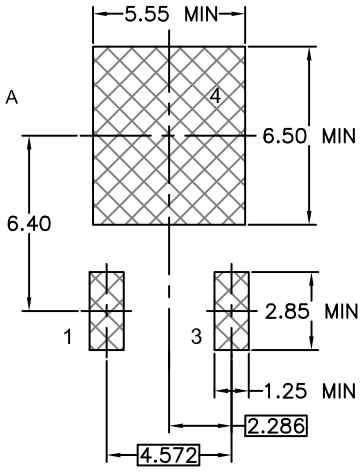
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	—	—
E	6.35	6.54	6.73
E1	4.32	—	—
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	—	—	1.02
θ	0°	---	10°

NON-DIODE PRODUCTS VERSION



NON-DIODE PRODUCTS VERSION





LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK3 (TO−252 3 LD)	PAGE 1 OF 1

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