

# MOSFET – N-Channel, POWERTRENCH®

**30 V, 7 A, 23 mΩ**

## FDS8984, FDS8984-F40

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of dc-dc converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### Features

- Max  $R_{DS(ON)} = 23\text{ m}\Omega$  @  $V_{GS} = 10\text{ V}$ ,  $I_D = 7\text{ A}$
- Max  $R_{DS(ON)} = 30\text{ m}\Omega$  @  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 6\text{ A}$
- Low Gate Charge
- 100%  $R_G$  Tested
- This Device is Pb-Free and Halogen Free

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

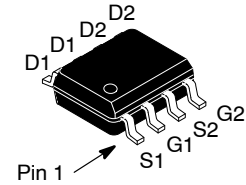
Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	- Continuous (Note 1a)	7
		- Pulsed	30
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	32	mJ
$P_D$	Power Dissipation for Single Operation	1.6	W
	Derate Above $25^\circ\text{C}$	13	mW/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

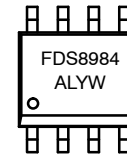
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C}/\text{W}$

$V_{DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
30 V	23 mΩ @ $V_{GS} = 10\text{ V}$	7.0 A
	30 mΩ @ $V_{GS} = 4.5\text{ V}$	6.0 A



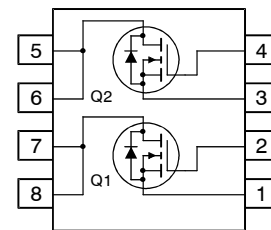
SOIC8  
CASE 751EB

### MARKING DIAGRAM



FDS8984 = Specific Device Code  
A = Assembly Site  
L = Wafer Lot Number  
YW = Assembly Start Week

### PIN ASSIGNMENT



N-Channel MOSFET

### ORDERING INFORMATION

Device	Package	Shipping†
FDS8984	SOIC8 (Pb-Free)	2500 / Tape & Reel
FDS8984-F40	SOIC8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDS8984, FDS8984-F40

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	30	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	23	-	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}$ , $V_{GS} = 0\ \text{V}$ $V_{DS} = 24\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $T_J = 125^\circ\text{C}$	-	-	1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$ , $V_{DS} = 0\ \text{V}$	-	-	$\pm 100$	nA

## ON CHARACTERISTICS (Note 3)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1.2	1.7	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	-4.3	-	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Drain to Source On-Resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 7\ \text{A}$ $V_{GS} = 4.5\ \text{V}$ , $I_D = 6\ \text{A}$ $V_{GS} = 10\ \text{V}$ , $I_D = 7\ \text{A}$ , $T_J = 125^\circ\text{C}$	-	19 24 26	23 30 32	$\text{m}\Omega$

## DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 15\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1.0\ \text{MHz}$	-	475	635	pF
$C_{oss}$	Output Capacitance		-	100	135	pF
$C_{rss}$	Reverse Transfer Capacitance		-	65	100	pF
$R_G$	Gate Resistance	$f = 1.0\ \text{MHz}$	-	0.9	1.6	$\Omega$

## SWITCHING CHARACTERISTICS (Note 3)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\ \text{V}$ , $I_D = 7\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $R_{GS} = 33\ \Omega$	-	5	10	ns
$t_r$	Rise Time		-	9	18	ns
$t_{d(off)}$	Turn-Off Delay Time		-	42	68	ns
$t_f$	Fall Time		-	21	34	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\ \text{V}$ , $V_{GS} = 10\ \text{V}$ , $I_D = 7\ \text{A}$	-	9.2	13	nC
$Q_g$	Total Gate Charge	$V_{DS} = 15\ \text{V}$ , $V_{GS} = 5\ \text{V}$ , $I_D = 7\ \text{A}$	-	5.0	7	nC
$Q_{gs}$	Gate to Source Gate Charge		-	1.5	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	2.0	-	nC

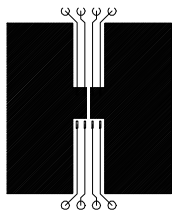
## DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 7\ \text{A}$	-	0.9	1.25	V
		$I_{SD} = 2.1\ \text{A}$	-	0.8	1.0	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 7\ \text{A}$ , $d_i/d_t = 100\ \text{A}/\mu\text{s}$	-	-	33	ns
$Q_{rr}$	Diode Reverse Recovery Charge		-	-	20	nC

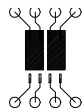
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## NOTES:

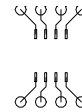
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $78^\circ\text{C}/\text{W}$  when mounted on a  $0.5\ \text{in}^2$  pad of 2 oz copper



b.  $125^\circ\text{C}/\text{W}$  when mounted on a  $0.02\ \text{in}^2$  pad of 2 oz copper



c.  $135^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\ \text{mH}$ ,  $I_{AS} = 8\ \text{A}$ ,  $V_{DD} = 27\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ .
- Pulse Test: Pulse Width  $< 300\ \mu\text{s}$ , Duty Cycle  $< 2.0\%$ .

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

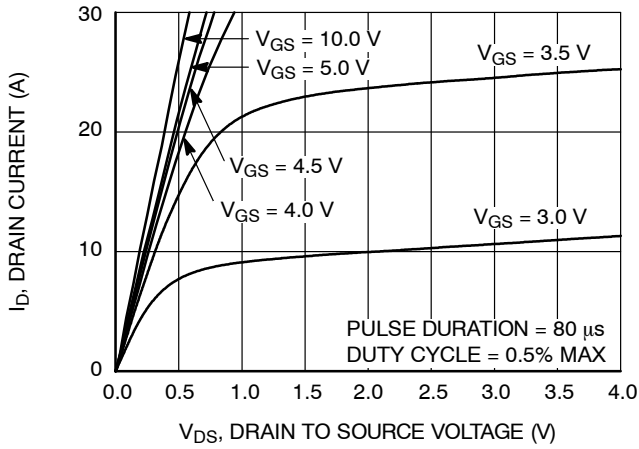


Figure 1. On Region Characteristics

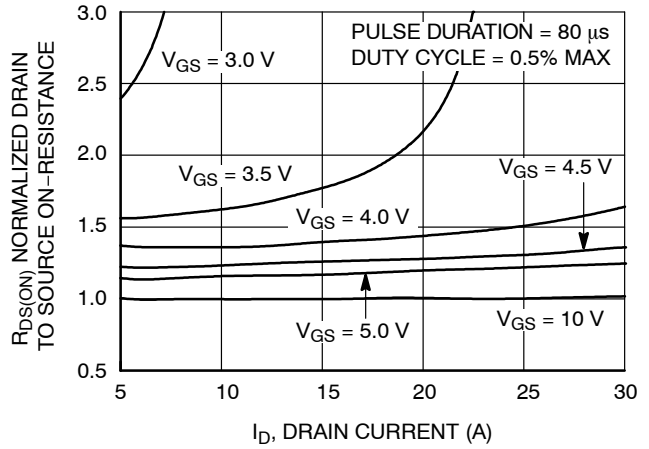


Figure 2. On-Resistance vs. Drain Current and Gate Voltage

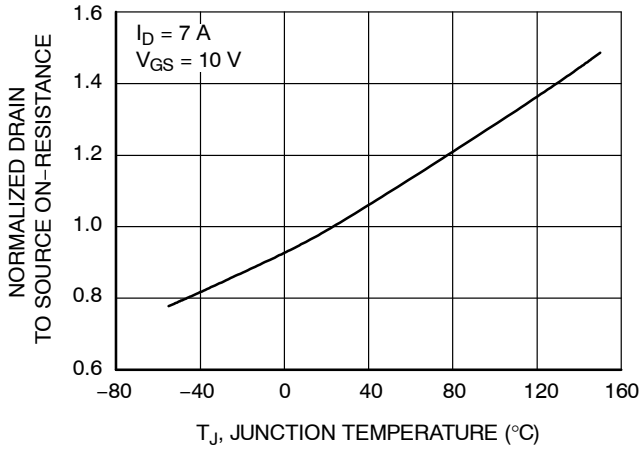


Figure 3. On-Resistance vs. Temperature

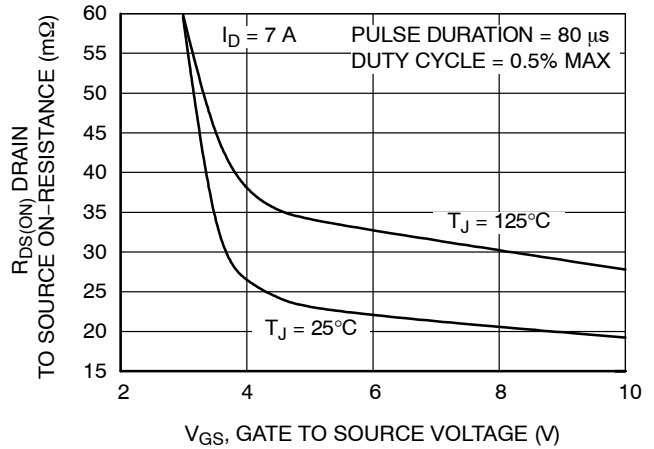


Figure 4. On-Resistance vs. Gate to Source Voltage

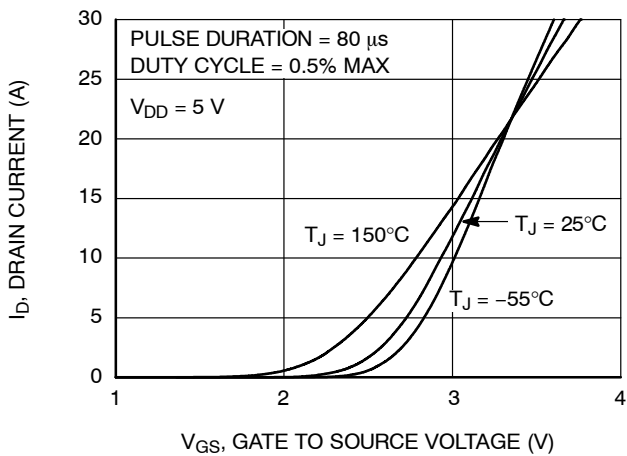


Figure 5. Transfer Characteristics

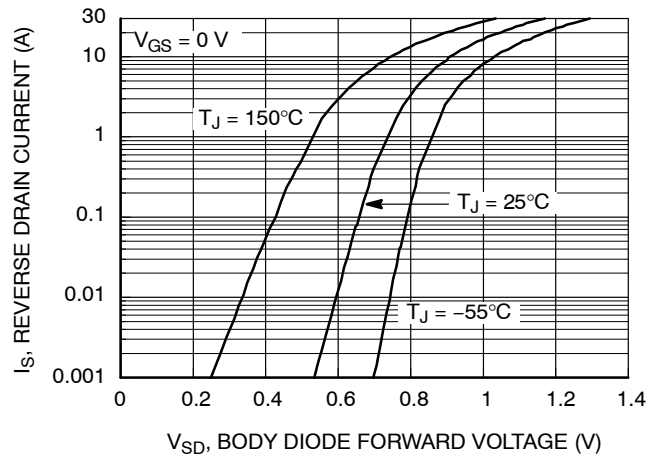


Figure 6. Source to Drain Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

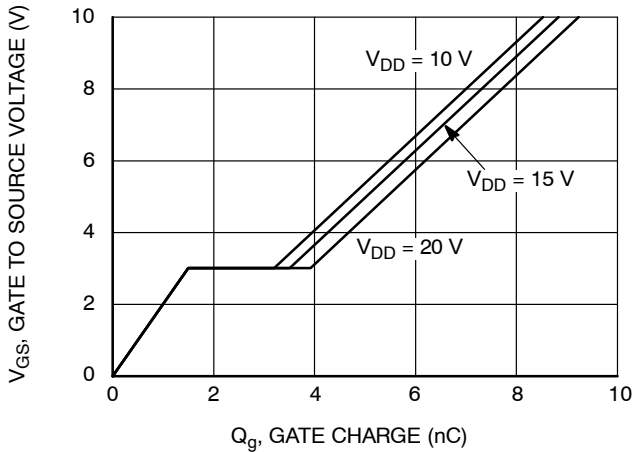


Figure 7. Gate Charge Characteristics

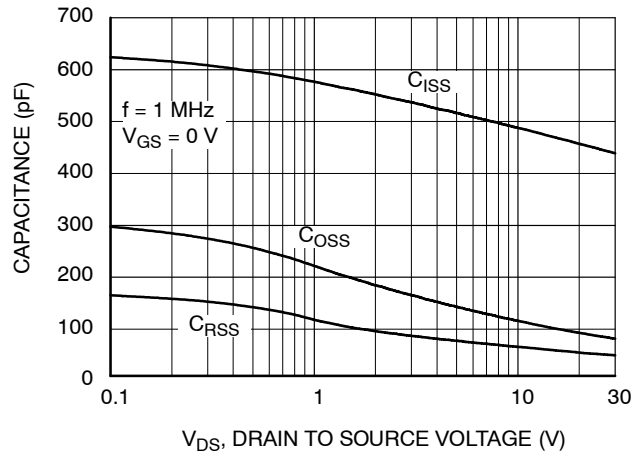


Figure 8. Capacitance vs. Drain to Source Voltage

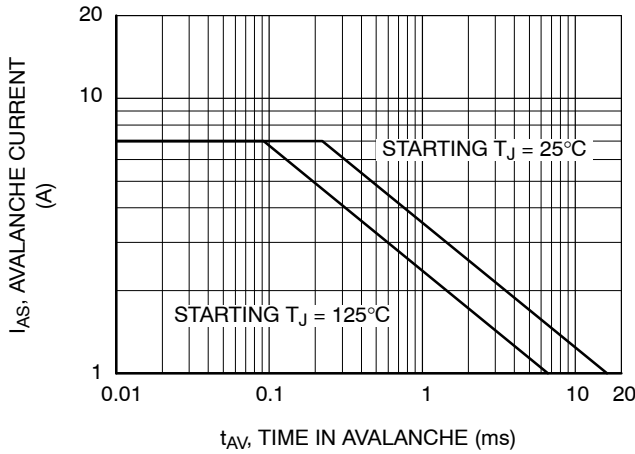


Figure 9. Unclamped Inductive Switching Capability

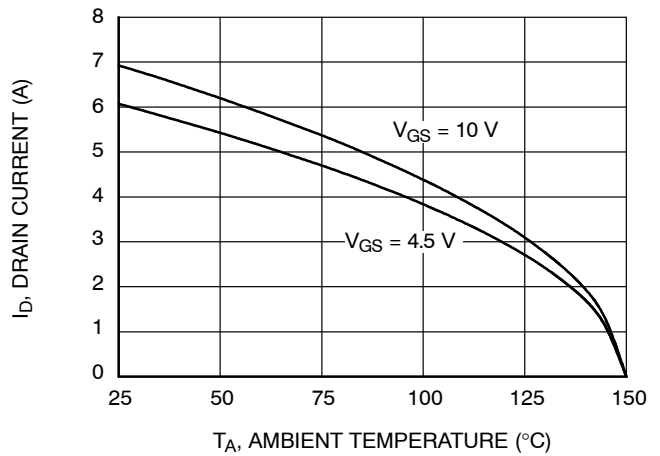


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

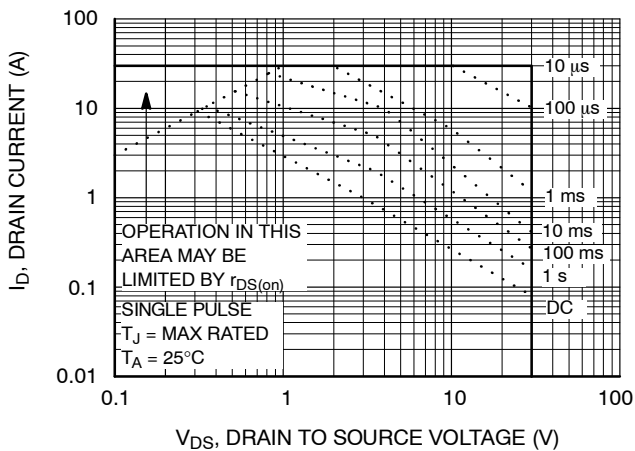


Figure 11. Forward Bias Safe Operating Area

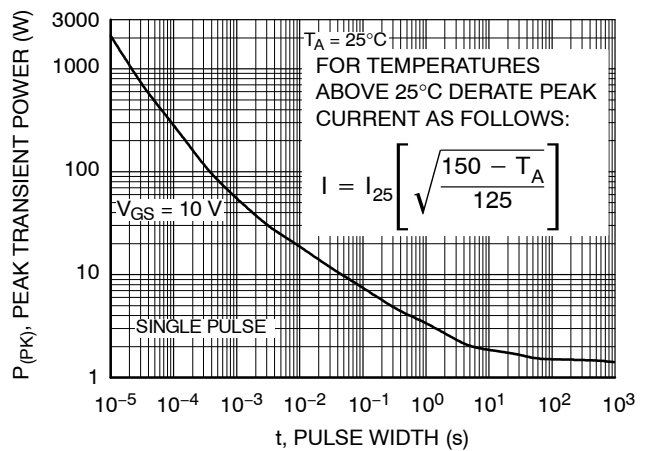


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

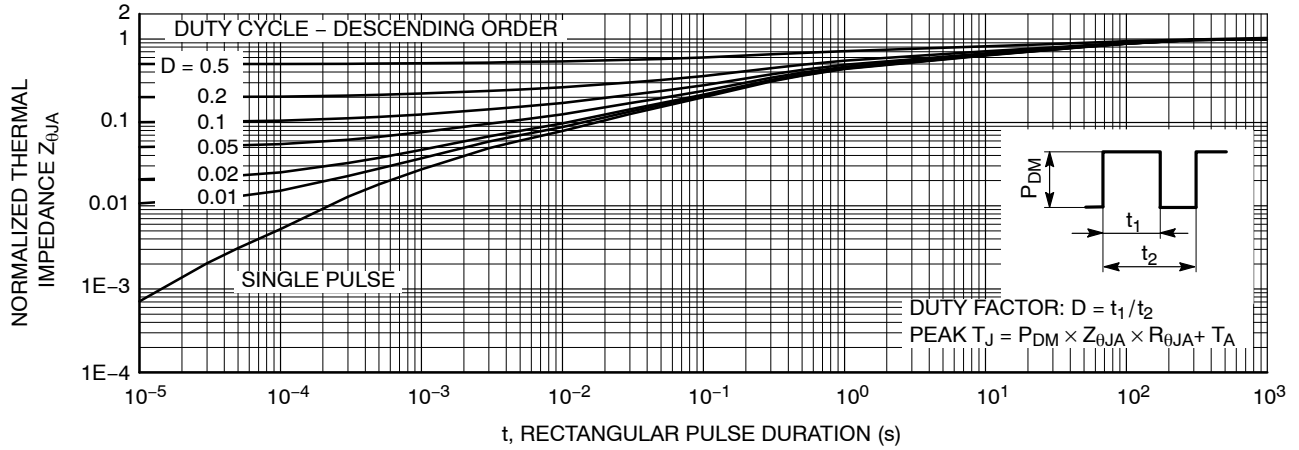


Figure 13. Transient Thermal Response Curve

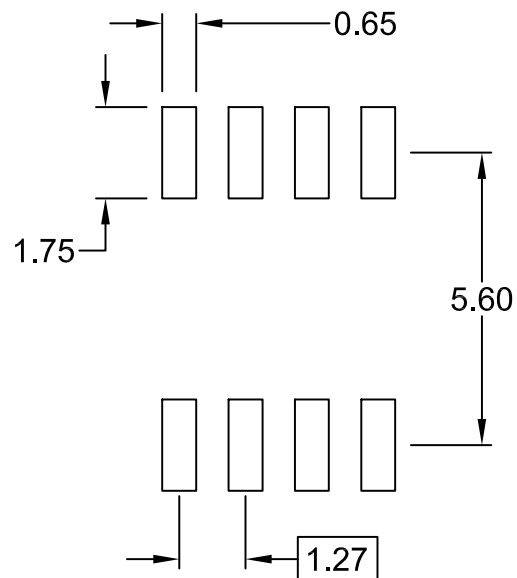
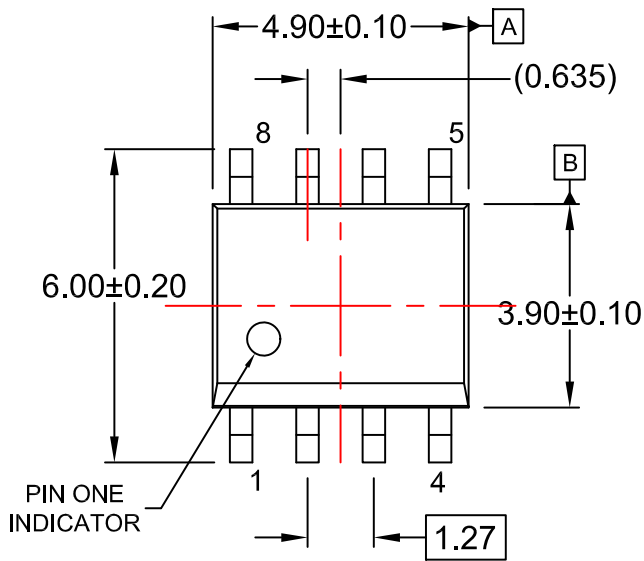
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

ON Semiconductor®

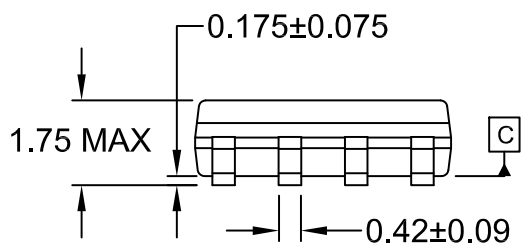


**SOIC8**  
**CASE 751EB**  
**ISSUE A**

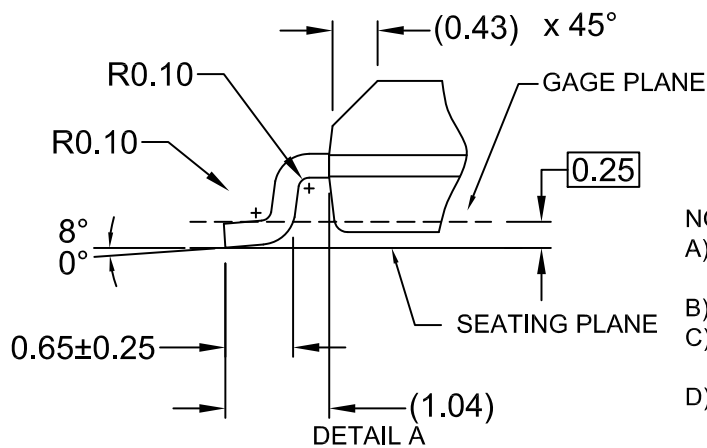
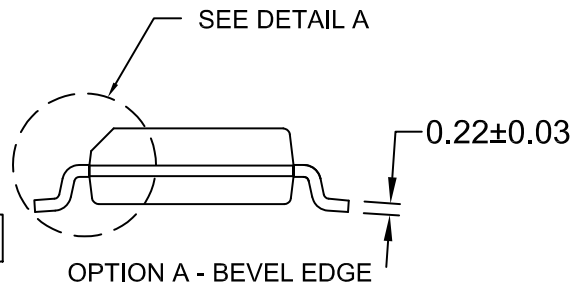
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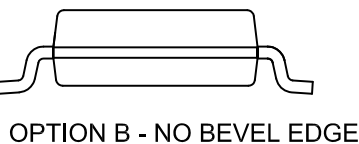
⊕ 0.25 (M) C B A



⌒ 0.10



SCALE: 2:1



**NOTES:**

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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