

FSQ0170RNA, FSQ0270RNA Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged 700V SenseFET
- Consumes only 0.8W at 230 V_{AC} & 0.5W Load with Burst-Mode Operation
- Precision Fixed Operating Frequency, 100kHz
- Internal Start-up Circuit and Built-in Soft-Start
- Pulse-by-Pulse Current Limiting and Auto-Restart Mode
- Over-Voltage Protection (OVP), Overload Protection (OLP), Internal Thermal Shutdown Function (TSD)
- Under-Voltage Lockout (UVLO)
- Low Operating Current (3mA)
- Adjustable Peak Current Limit

Applications

- Auxiliary Power Supply for PC and Server
- SMPS for VCR, SVR, STB, DVD & DVCD Player, Printer, Facsimile & Scanner
- Adapter for Camcorder

Related Application Notes

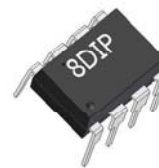
- AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)
- AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)
- AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications
- AN-4147: Design Guidelines for RCD Snubber of Flyback
- AN-4148: Audible Noise Reduction Techniques for FPS™ Applications

Description

The FSQ0170RNA, and FSQ0270RNA, consists of an integrated current mode Pulse Width Modulator (PWM) and an avalanche-rugged 700V Sense FET. It is specifically designed for high-performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. The integrated PWM controller features include: a fixed-frequency generating oscillator, Under-Voltage Lockout (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, and temperature compensated precision current sources for loop compensation and fault protection circuitry.

Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSQ0170RNA, and FSQ0270RNA reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform that is well suited for the design of cost-effective flyback converters, as in PC auxiliary power supplies.

8-DIP



Ordering Information

Product Number	Package	Marking Code	BV _{DSS}	f _{osc}	R _{DS(ON)} (MAX.)
FSQ0170RNA	8DIP	Q0170RA	700V	100kHz	11Ω
FSQ0270RNA	8DIP	Q0270RA	700V	100kHz	7.2Ω

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Application Diagram

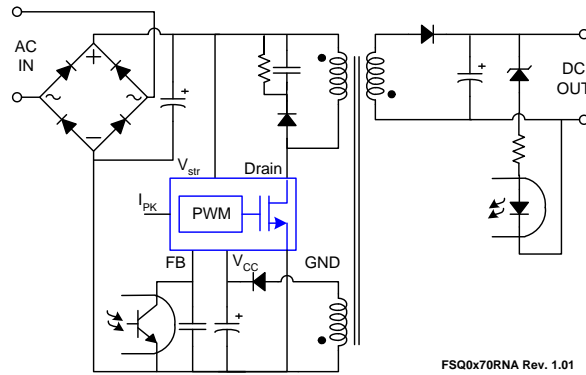


Figure 1. Typical Flyback Application

Output Power Table⁽¹⁾

Product	230V _{AC} ±15% ⁽²⁾		85–265V _{AC}	
	Adapter ⁽³⁾	Open Frame ⁽⁴⁾	Adapter ⁽³⁾	Open Frame ⁽⁴⁾
FSQ0170RNA	14W	20W	9W	13W
FSQ0270RNA	17W	24W	11W	16W

Notes:

1. The maximum output power can be limited by junction temperature.
2. 230 V_{AC} or 100/115 V_{AC} with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink, at 50°C ambient.
4. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sink, at 50°C ambient.

Internal Block Diagram

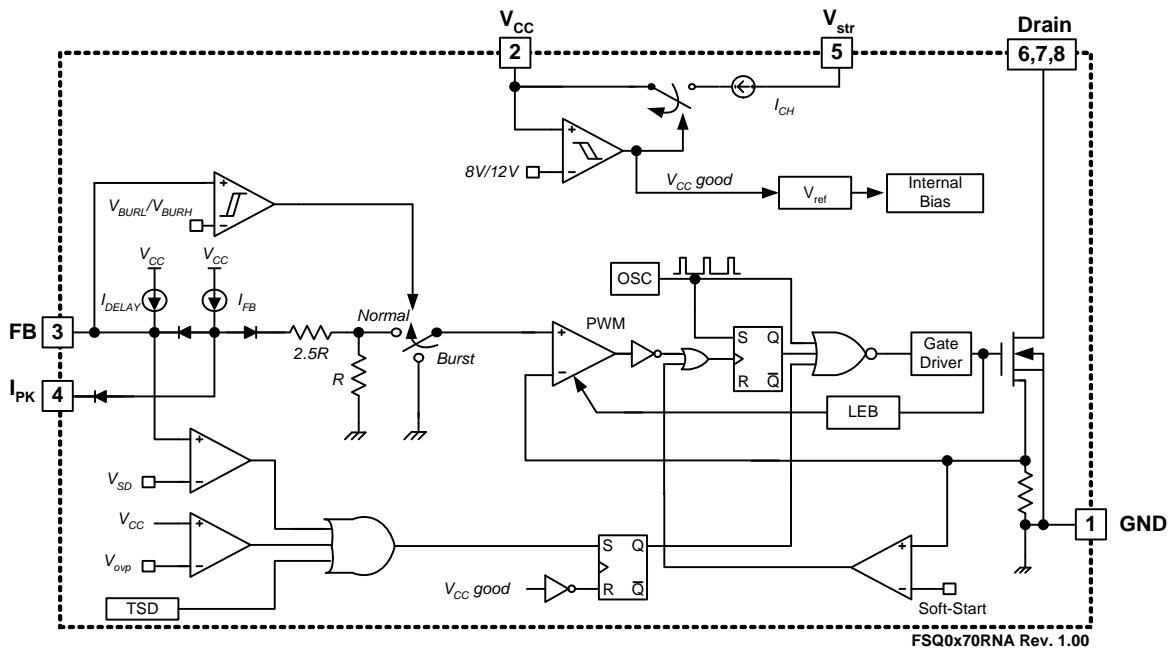


Figure 2. Internal Block Diagram

Pin Configuration

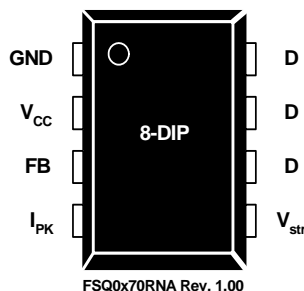


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	Ground. SenseFET source terminal on primary side and internal control ground.
2	V_{CC}	Power Supply. Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V_{str}) via an internal switch during start-up, see Figure 2. It is not until V_{CC} reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	FB	Feedback. The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and opto-coupler are typically connected externally. A feedback voltage of 6V triggers overload protection (OLP). There is a time delay while charging external capacitor C_{FB} from 3V to 6V using an internal 5 μ A current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
4	I_{PK}	Peak Current Limit. This pin adjusts the peak current limit of the SenseFET. The 0.9mA feedback current source is diverted to the parallel combination of an internal 2.8k Ω resistor and any external resistor to GND on this pin. This determines the peak current limit. If this pin is tied to V_{CC} or left floating, the typical peak current limit is 0.8A (FSQ0170RNA), 0.9A (FSQ0270RNA).
5	V_{str}	Start-up. This pin connects to the rectified AC line voltage source. At start-up, the internal switch supplies internal bias and charges an external storage capacitor placed between the V_{CC} pin and ground. Once the V_{CC} reaches 12V, the internal switch is opened.
6	Drain	SenseFET drain. High-voltage power SenseFET drain connection.
7	Drain	SenseFET drain. High-voltage power SenseFET drain connection.
8	Drain	SenseFET drain. High-voltage power SenseFET drain connection.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only

Symbol	Characteristic	Value	Unit
V _{DRAIN}	Drain Pin Voltage	700	V
V _{STR}	Vstr Pin Voltage	700	V
I _{DM}	Drain Current Pulsed ⁽⁵⁾	FSQ0170RNA	4
		FSQ0270RNA	8
E _{AS}	Single Pulsed Avalanche Energy ⁽⁶⁾	FSQ0170RNA	50
		FSQ0270RNA	140
V _{CC}	Supply Voltage	20	V
V _{FB}	Feedback Voltage Range	-0.3 to V _{CC}	V
P _D	Total Power Dissipation	1.5	W
T _J	Operating Junction Temperature	Internally limited	°C
T _A	Operating Ambient Temperature	-25 to +85	°C
T _{STG}	Storage Temperature	-55 to +150	°C

Notes:

5. Non-repetitive rating: Pulse width is limited by maximum junction temperature.
6. L = 51mH, starting T_J = 25°C.

Thermal Impedance

T_A = 25°C, unless otherwise specified. All items are tested with the standards JESD 51-2 and 51-10 (DIP).

Symbol	Parameter	Value	Unit
θ _{JA}	Junction-to-Ambient Thermal Resistance ⁽⁷⁾	80	°C/W
θ _{JC}	Junction-to-Case Thermal Resistance ⁽⁸⁾	20	°C/W
θ _{JT}	Junction-to-Top Thermal Resistance ⁽⁹⁾	35	°C/W

Notes:

7. Free standing with no heatsink; without copper clad.
(Measurement Condition - Just before junction temperature T_J enters into OTP.)
8. Measured on the DRAIN pin close to plastic interface.
9. Measured on the PKG top surface.

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
SenseFET Section⁽¹⁰⁾							
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{DS} = 700\text{V}, V_{GS} = 0\text{V}$			50	μA	
		$V_{DS} = 560\text{V}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$			200		
$R_{DS(ON)}$	Drain-Source On-State Resistance ⁽¹¹⁾	FSQ0170RNA FSQ0270RNA	$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$		8.8	11	Ω
					6.0	7.2	
C_{ISS}	Input Capacitance	FSQ0170RNA FSQ0270RNA			250		
					550		
C_{OSS}	Output Capacitance	FSQ0170RNA FSQ0270RNA	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		25		pF
					38		
C_{RSS}	Reverse Transfer Capacitance	FSQ0170RNA FSQ0270RNA			10		
					17		
$t_{d(on)}$	Turn-On Delay Time	FSQ0170RNA FSQ0270RNA			12		
					20		
t_r	Rise Time	FSQ0170RNA FSQ0270RNA	$V_{DS} = 350\text{V}, I_D = 1.0\text{A}$		4		ns
					15		
$t_{d(off)}$	Turn-Off Delay Time	FSQ0170RNA FSQ0270RNA			30		
					55		
t_f	Fall Time	FSQ0170RNA FSQ0270RNA			10		
					25		
Control Section							
f_{OSC}	Switching Frequency		92	100	108	KHz	
Δf_{OSC}	Switching Frequency Variation ⁽¹⁰⁾	$-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		± 5	± 10	%	
D_{MAX}	Maximum Duty Cycle	Measured at $0.1 \times V_{DS}$	55	60	65	%	
D_{MIN}	Minimum Duty Cycle		0	0	0	%	
V_{START}	UVLO Threshold Voltage	$V_{FB} = \text{GND}$	11	12	13	V	
V_{STOP}		$V_{FB} = \text{GND}$	7	8	9		
I_{FB}	Feedback Source Current	$V_{FB} = \text{GND}$	0.7	0.9	1.1	mA	
$t_{S/S}$	Internal Soft-Start Time ⁽¹⁰⁾	$V_{FB} = 4\text{V}$		10		ms	

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
Burst-Mode Section							
V _{BURH}	Burst-Mode Voltage	T _J = 25°C	0.5	0.6	0.7	V	
V _{BURL}			0.3	0.4	0.5	V	
V _{BUR(HYS)}			100	200	300	mV	
Protection Section							
I _{LIM}	Peak Current Limit	FSQ0170RNA	di/dt = 170mA/μs	0.70	0.80	0.90	A
		FSQ0270RNA	di/dt = 200mA/μs	0.79	0.90	1.01	
t _{CLD}	Current Limit Delay Time ⁽¹⁰⁾			500		ns	
T _{SD}	Thermal Shutdown Temperature ⁽¹⁰⁾		125	140		°C	
V _{SD}	Shutdown Feedback Voltage		5.5	6.0	6.5	V	
V _{OVP}	Over-Voltage Protection		18	19		V	
I _{DELAY}	Shutdown Delay Current	V _{FB} = 4V	3.5	5.0	6.5	μA	
t _{LEB}	Leading Edge Blanking Time ⁽¹⁰⁾		200			ns	
Total Device Section							
I _{OP}	Operating Supply Current (Control Part Only)	V _{CC} = 14V	1	3	5	mA	
I _{CH}	Startup Charging Current	V _{CC} = 0V, R _{STR} < 100kΩ ⁽¹²⁾	0.70	0.85	1.00	mA	
V _{STR}	V _{str} Supply Voltage	V _{CC} = 0V		24		V	

Notes:

10. These parameters, although guaranteed, are not 100% tested in production.
11. Pulse test: Pulse width ≤ 300μs, duty ≤ 2%.
12. R_{STR} is connected between the rectified AC line voltage source and VSTR pin.

Typical Performance Characteristics (Control Part)

These characteristic graphs are normalized at $T_A = 25^\circ\text{C}$.

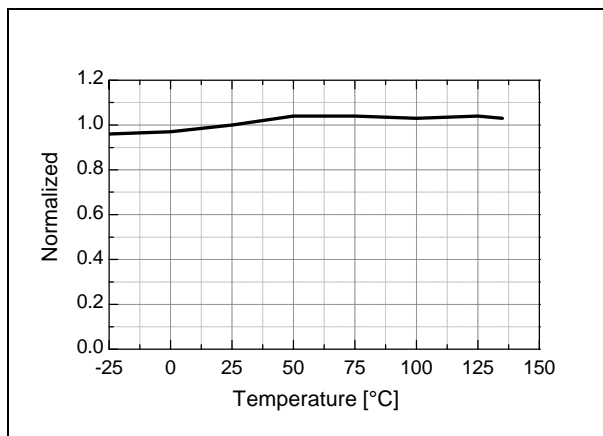


Figure 4. Operating Frequency (f_{OSC}) vs. T_A

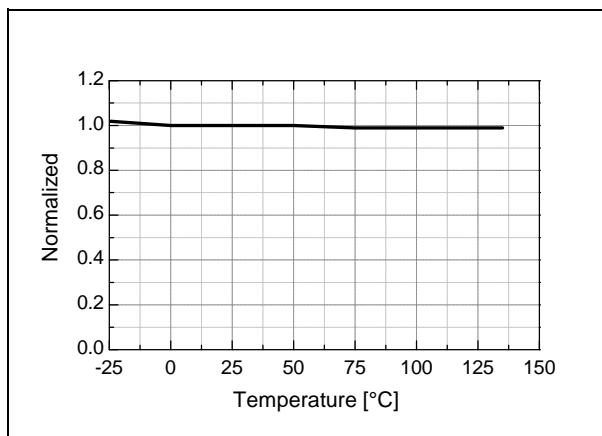


Figure 5. Over-Voltage Protection (V_{OVP}) vs. T_A

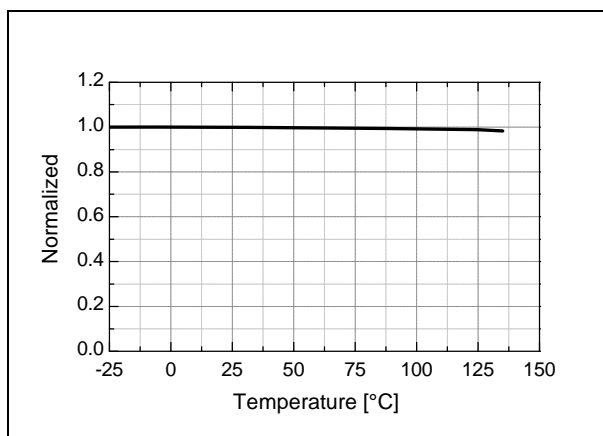


Figure 6. Maximum Duty Cycle (D_{MAX}) vs. T_A

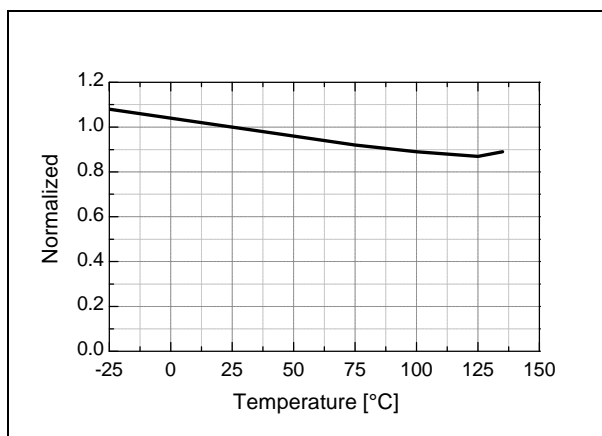


Figure 7. Operating Supply Current (I_{OP}) vs. T_A

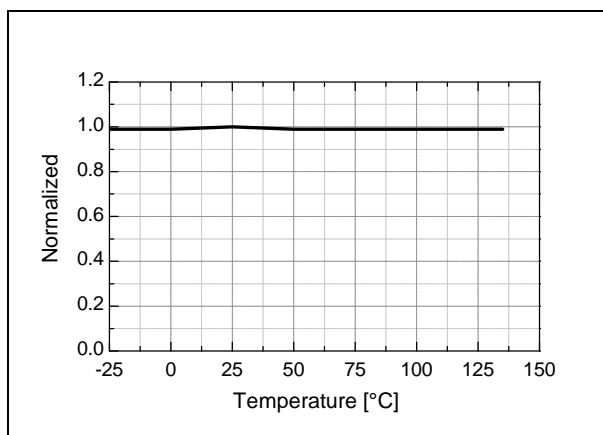


Figure 8. Start Threshold Voltage (V_{START}) vs. T_A

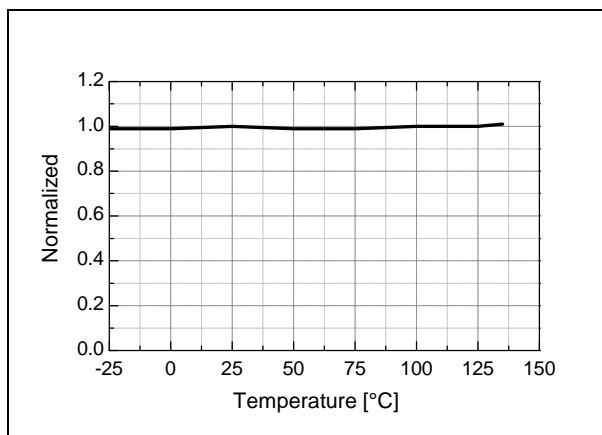


Figure 9. Stop Threshold Voltage (V_{STOP}) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A = 25^\circ\text{C}$.

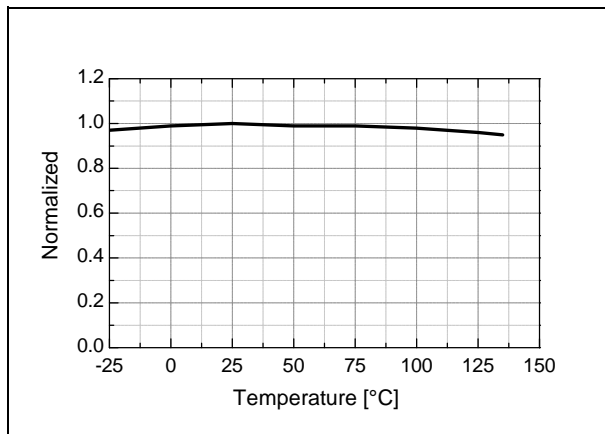


Figure 10. Feedback Source Current (I_{FB}) vs. T_A

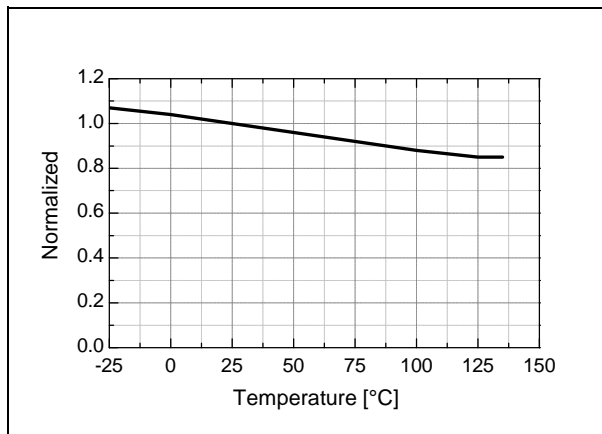


Figure 11. Startup Charging Current (I_{CH}) vs. T_A

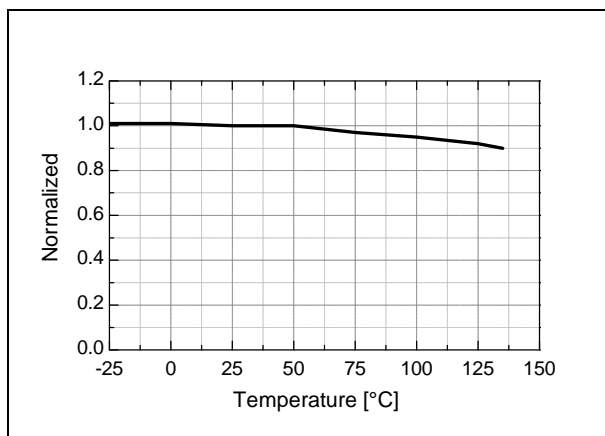


Figure 12. Peak Current Limit (I_{LIM}) vs. T_A

IC to detect the temperature of the SenseFET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

4.3 Over-Voltage Protection (OVP): In the event of a malfunction in the secondary-side feedback circuit, or an open feedback loop caused by a soldering defect, the current through the opto-coupler transistor becomes almost zero (see Figure 14). V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an Over-Voltage Protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the FPS uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, the OVP circuit is activated, resulting in termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 19V.

5. Soft-Start: The FPS has an internal soft-start circuit that slowly increases the SenseFET current after start-up, as shown in Figure 16. The typical soft-start time is 10ms, where progressive increments of the SenseFET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This also helps prevent transformer saturation and reduces the stress on the secondary diode during startup.

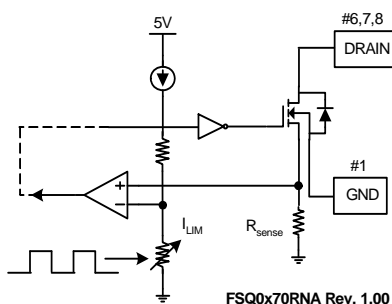


Figure 16. Soft-Start Function

6. Burst Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. Feedback voltage decreases as the load decreases, as shown in Figure 17, and the device automatically enters burst-mode when the feedback voltage drops below V_{BURH} (typically 600mV). Switching continues until the feedback voltage drops below V_{BURL} (typically 400mV).

At this point, switching stops and the output voltage starts to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} , switching resumes. The feedback voltage then falls and the process is repeated. Burst-mode operation alternately enables and disables switching of the SenseFET and reduces switching loss in standby mode.

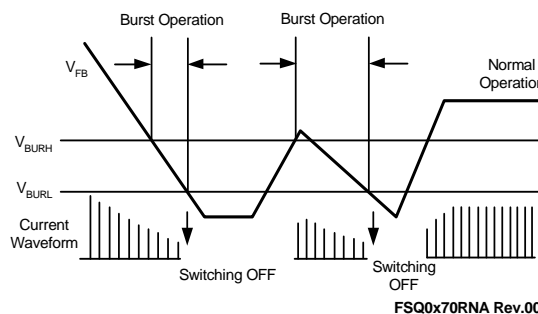


Figure 17. Burst Operation Function

7. Adjusting Peak Current Limit: As shown in Figure 18, a combined 2.8kΩ internal resistance is connected to the non-inverting lead on the PWM comparator. An external resistance of R_x on the current limit pin forms a parallel resistance with the 2.8kΩ when the internal diodes are biased by the main current source of 900μA.

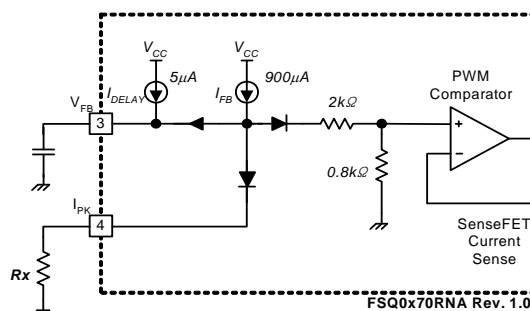


Figure 18. Peak Current Limit Adjustment

For example, FSQ0270RNA has a typical SenseFET peak current limit (I_{LIM}) of 0.9A. I_{LIM} can be adjusted to 0.6A by inserting R_x between the I_{PK} pin and the ground. The value of the R_x can be estimated by the following equations:

$$0.9A: 0.6A = 2.8k\Omega : Xk\Omega,$$

$$X = R_x \parallel 2.8k\Omega$$

where X represents the resistance of the parallel network.

Application Information

Methods of Reducing Audible Noise

Switching-mode power converters have electronic and magnetic components, which generate audible noise when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20KHz, they can make noise, depending on the load condition. The following sections discuss methods to reduce noise.

Glue or Varnish

The most common method of reducing noise involves using glue or varnish to tighten magnetic components. The motion of core, bobbin, and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise. Glue or varnish can also crack the core because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect, depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. Another possibility is to use a Zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of the 2~4kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4kHz. When the fundamental frequency of noise is located in this range, the noise sounds louder although the noise intensity level is identical (see Figure 19).

When the FPS acts in burst mode and the burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of burst mode operation lies in the range of 2~4kHz, adjusting the feedback loop can shift the burst operation frequency. To reduce the burst operation frequency, increase a feedback gain capacitor (C_F), opto-coupler supply resistor (R_D); and feedback capacitor (C_B), and decrease a feedback gain resistor (R_F), as shown in Figure 20.

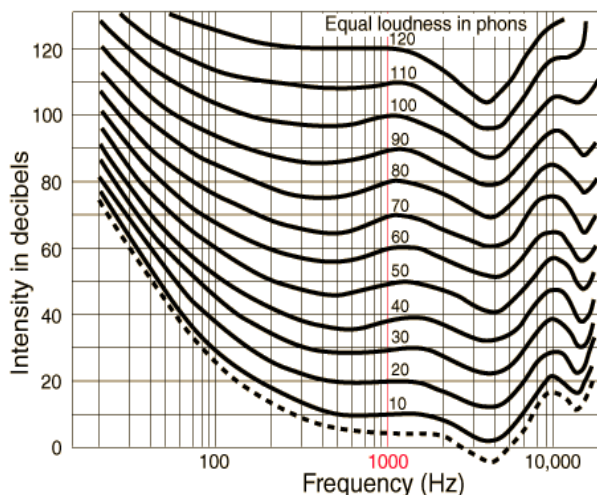


Figure 19. Equal Loudness Curves

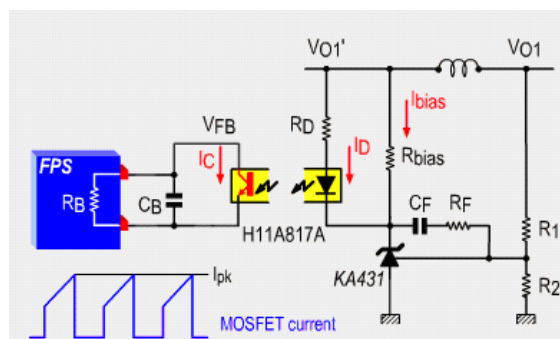


Figure 20. Typical Feedback Network of FPS

Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters using Fairchild Power Switch (FPS™)

AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for FPS™ Applications

2. Transformer

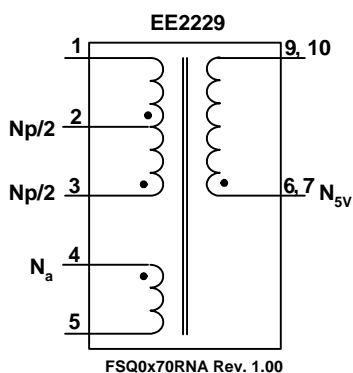


Figure 22. Transformer Schematic Diagram

3. Winding Specification

	Pin (S → F)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	$0.3\phi \times 1$	72	Solenoid winding
Insulation: Polyester Tape $t = 0.025\text{mm}$, 1 Layers				
N_a	4 → 5	$0.25\phi \times 2$	22	Solenoid winding
Insulation: Polyester Tape $t = 0.025\text{mm}$, 2 Layers				
N_{5V}	6, 7 → 9, 10	$0.65\phi \times 2$	8	Solenoid winding
Insulation: Polyester Tape $t = 0.025\text{mm}$, 2 Layers				
$N_p/2$	2 → 1	$0.3\phi \times 1$	72	Solenoid winding
Insulation: Polyester Tape $t = 0.025\text{mm}$, 2 Layers				

4. Electrical Characteristics

	Pin	Specification	Remark
Inductance	1–3	$1.20\text{mH} \pm 5\%$	100kHz, 1V
Leakage	1–3	$< 30\mu\text{H}$ Max	Short all other pins

5. Core & Bobbin

- Core: EE2229 (Material: PL-7, $A_e = 35.7 \text{ mm}^2$)
- Bobbin: BE2229

6. Demo Circuit Part List

Part Number	Value	Quantity	Description (Manufacturer)
C6, C8	47nF	2	Ceramic Capacitor
C1	2.2nF (1KV)	1	AC Ceramic Capacitor(X1 & Y1)
C10	1nF (200V)	1	Mylar Capacitor
CS1	1.5nF (50V)	1	Ceramic Capacitor
C2, C3	22 μ F (400V)	2	Low Impedance Electrolytic Capacitor KMX series
C4, C9	1000 μ F (16V)	2	Low ESR Electrolytic Capacitor NXC series
C5	470 μ F (10V)	1	Low ESR Electrolytic Capacitor NXC series
C7	47 μ F (25V)	1	General Electrolytic Capacitor
CL9	10 μ F (50V)	1	General Electrolytic Capacitor
L1	330 μ H	1	Inductor
L2	1 μ H	1	Inductor
R6	2.4 (1W)	1	Fusible Resistor
J1, J2, J4, L3	0	4	Jumper
R2	4.7k Ω	1	Resistor
R3	560 Ω	1	Resistor
R4	100 Ω	1	Resistor
R5	1.25k Ω	1	Resistor
R11	1.2k Ω	1	Resistor
R9	10k Ω	1	Resistor
R10	2 Ω	1	Resistor
R14	30 Ω	1	Resistor
RL3	1k Ω	1	Resistor
RL1, RL2	1M Ω	2	Resistor
RL4	120k Ω	1	Resistor
RL5	30k Ω	1	Resistor
RL7	40k Ω	1	Resistor
RS1	9 Ω	1	Resistor
ZR1	80 Ω	1	Resistor
U1	FOD817A	1	IC (Fairchild Semiconductor)
U2	TL431	1	IC (Fairchild Semiconductor)
U3	FSQ0270RNA	1	IC (Fairchild Semiconductor)
QL1	2N2907	1	IC (Fairchild Semiconductor)
QL2	2N2222	1	IC (Fairchild Semiconductor)
D2, D3, D4, D5, D6, DS1	1N4007	6	Diode (Fairchild Semiconductor)
D1	SB540	1	Schottky Diode (Fairchild Semiconductor)
ZD1	1N4745	1	Zener Diode (Fairchild Semiconductor)
DL1	1N5233	1	Zener Diode (Fairchild Semiconductor)
ZP1	82V (1W)	1	Zener Diode (Fairchild Semiconductor)
ZDS1	P6KE180A	1	TVS (Fairchild Semiconductor)

7. Layout

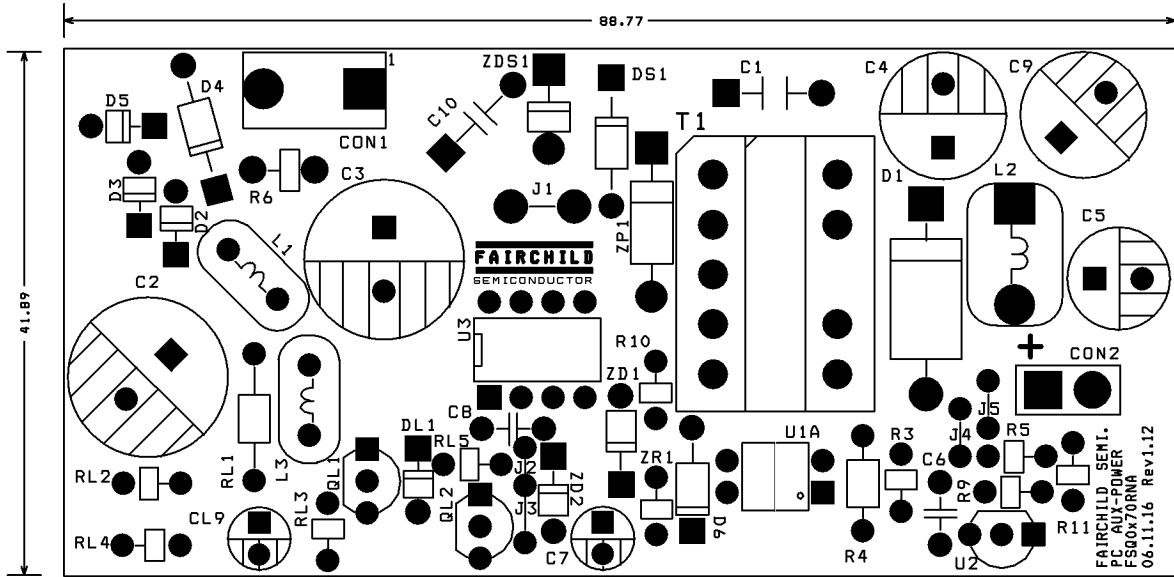


Figure 23. Top Image of PCB

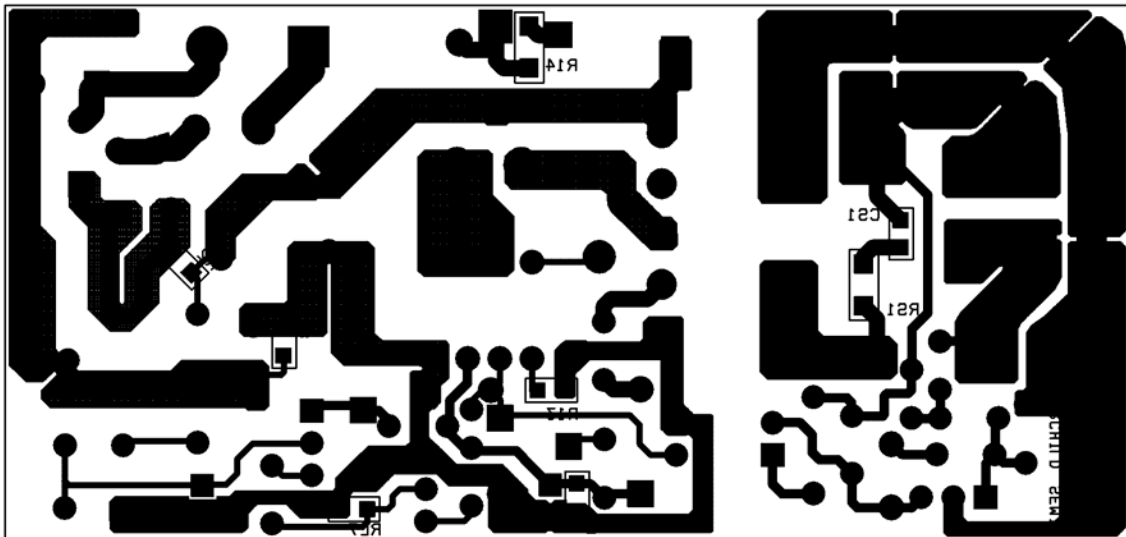
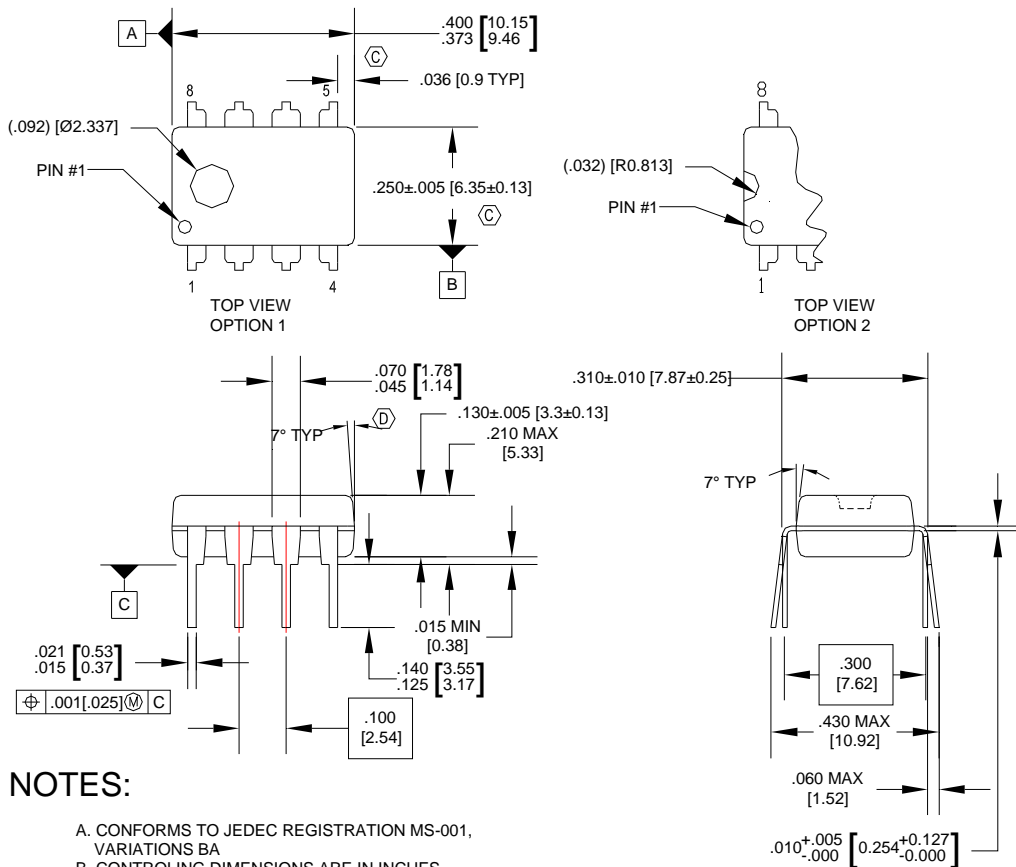


Figure 24. Bottom Image of PCB

Package Dimensions



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS BA
- B. CONTROLLING DIMENSIONS ARE IN INCHES
REFERENCE DIMENSIONS ARE IN MILLIMETERS
- (C) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED
.010 INCHES OR 0.25MM.
- (D) DOES NOT INCLUDE DAMBAR PROTRUSIONS.
DAMBAR PROTRUSIONS SHALL NOT EXCEED
.010 INCHES OR 0.25MM.
- E. DIMENSIONING AND TOLERANCING
PER ASME Y14.5M-1994.

N08EREVG

Figure 25. 8-Lead Dual In-Line Package (DIP)

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