FAIRCHILD SEMICONDUCTOR™

August 1997
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# FST3125
# Quad Bus Switch

## General Description

The Fairchild Switch FST3125 provides four high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as four 1-bit switches with separate $\overline{OE}$ inputs. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

## Features

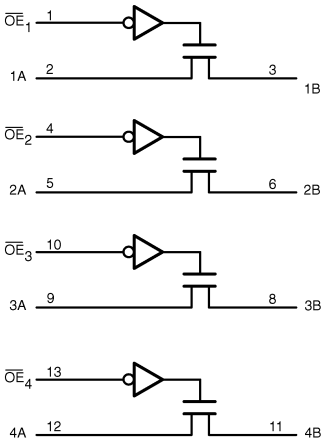
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low $I_{CC}$.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| FST3125M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| FST3125QSC | MQA16 | 16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide |
| FST3125MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

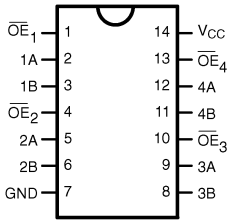
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Diagram

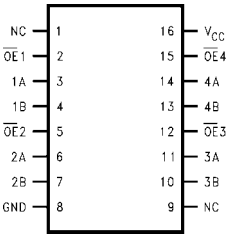



## Connection Diagrams

**Pin Assignment for SOIC and TSSOP**




**Pin Assignment for QSOP**




## Pin Descriptions

| Pin Name | Description |
|---|---|
| $\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$, $\overline{OE}_4$ | Bus Switch Enables |
| 1A, 2A, 3A, 4A | Bus A |
| 1B, 2B, 3B, 4B | Bus B |
| NC | Not Connected |

## Truth Table

| Inputs | Inputs/Outputs |
|---|---|
| $\overline{OE}$ | A,B |
| L | A = B |
| H | Z |

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | –0.5V to +7.0V |
| DC Switch Voltage ($V_S$) | –0.5V to +7.0V |
| DC Input Voltage ($V_{IN}$)(Note 2) | –0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) $V_{IN}$<0V | –50mA |
| DC Output ($I_{OUT}$) Sink Current | 128mA |
| DC $V_{CC}$/GND Current ($I_{CC}$/$I_{GND}$) | +/– 100mA |
| Storage Temperature Range ($T_{STG}$) | –65°C to +150 °C |

## Recommended Operating Conditions (Note 3)

| | |
|---|---|
| Power Supply Operating ($V_{CC}$) | 4.0V to 5.5V |
| Input Voltage ($V_{IN}$) | 0V to 5.5V |
| Output Voltage ($V_{OUT}$) | 0V to 5.5V |
| Input Rise and Fall Time ($t_r$, $t_f$) | |
| Switch Control Input | 0ns/V to 5ns/V |
| Switch I/O | 0ns/V to DC |
| Free Air Operating Temperature ($T_A$) | –40 °C to +85 °C |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 3:** Unused control inputs must be held high or low. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = –40 °C to +85 °C | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ (Note 4) | Max | | |
| $V_{IK}$ | Clamp Diode Voltage | 4.5 | | | –1.2 | V | $I_{IN}$ = –18mA |
| $V_{IH}$ | High Level Input Voltage | 4.0–5.5 | 2.0 | | | V | |
| $V_{IL}$ | Low Level Input Voltage | 4.0–5.5 | | | 0.8 | V | |
| $I_I$ | Input Leakage Current | 5.5 | | | ±1.0 | µA | 0≤ $V_{IN}$ ≤5.5V |
| $I_{OZ}$ | OFF-STATE Leakage Current | 5.5 | | | ±1.0 | µA | 0 ≤A, B ≤$V_{CC}$ |
| $R_{ON}$ | Switch On Resistance (Note 5) | 4.5 | | 4 | 7 | Ω | $V_{IN}$ = 0V, $I_{IN}$ = 64mA |
| | | 4.5 | | 4 | 7 | Ω | $V_{IN}$ = 0V, $I_{IN}$ = 30mA |
| | | 4.5 | | 8 | 15 | Ω | $V_{IN}$ = 2.4V, $I_{IN}$ = 15mA |
| | | 4.0 | | 11 | 20 | Ω | $V_{IN}$ = 2.4V, $I_{IN}$ = 15mA |
| $I_{CC}$ | Quiescent Supply Current | 5.5 | | | 3 | µA | $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | 5.5 | | | 2.5 | mA | One input at 3.4V. Other inputs at $V_{CC}$ or GND |

**Note 4:** Typical values are at $V_{CC}$ = 5.0V and $T_A$ = +25°C

**Note 5:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40\ °C$ to $+85\ °C$, $C_L = 50pF$, $RU = RD = 500\Omega$ | | | | Units | Conditions | Figure No. |
|---|---|---|---|---|---|---|---|---|
| | | $V_{CC} = 4.5 - 5.5V$ | | $V_{CC} = 4.0V$ | | | | |
| | | Min | Max | Min | Max | | | |
| $t_{PHL}$,$t_{PLH}$ | Prop Delay Bus to Bus (Note 6) | | 0.25 | | 0.25 | ns | $V_I$ = OPEN | Figure 1<br>Figure 2 |
| $t_{PZH}$, $t_{PZL}$ | Output Enable Time | 1.0 | 5.0 | | 5.5 | ns | $V_I$ = 7V for $t_{PZL}$<br>$V_I$ = OPEN for $t_{PZH}$ | Figure 1<br>Figure 2 |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time | 1.5 | 5.3 | | 5.6 | ns | $V_I$ = 7V for $t_{PLZ}$<br>$V_I$ = OPEN for $t_{PHZ}$ | Figure 1<br>Figure 2 |

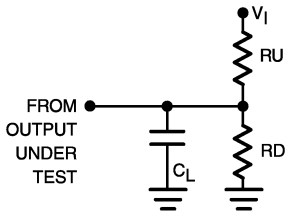
**Note 6:** This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

## Capacitance (Note 7)

| Symbol | Parameter | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Control Pin Input Capacitance | 3 | | pF | $V_{CC}$ = 5.0V |
| $C_{I/O}$ | Input/Output Capacitance | 5 | | pF | $V_{CC}$, $\overline{OE}$ = 5.0V |

**Note 7:** $T_A$ = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

## AC Loading and Waveforms




**Note:** Input driven by 50 Ω source terminated in 50 Ω

**Note:** $C_L$ includes load and stray capacitance

**Note:** Input PRR = 1.0 MHz, $t_W$ = 500ns

**FIGURE 1. AC Test Circuit**

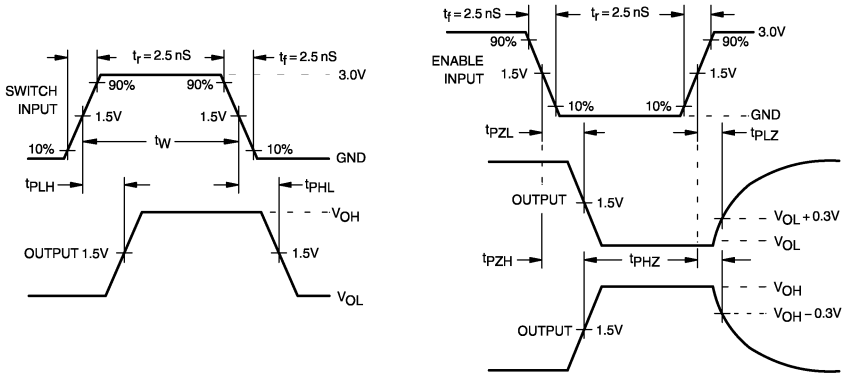
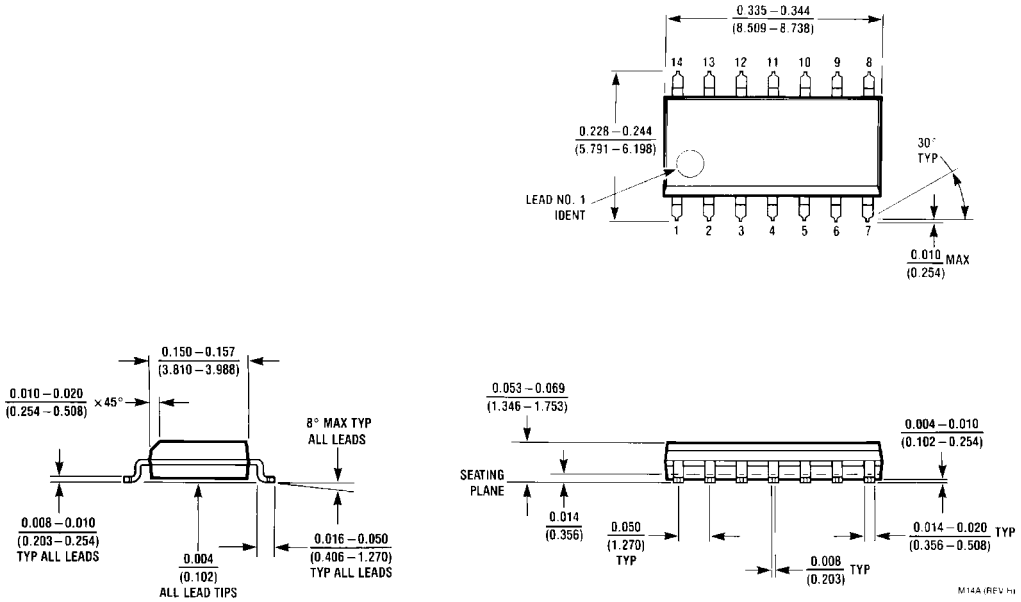
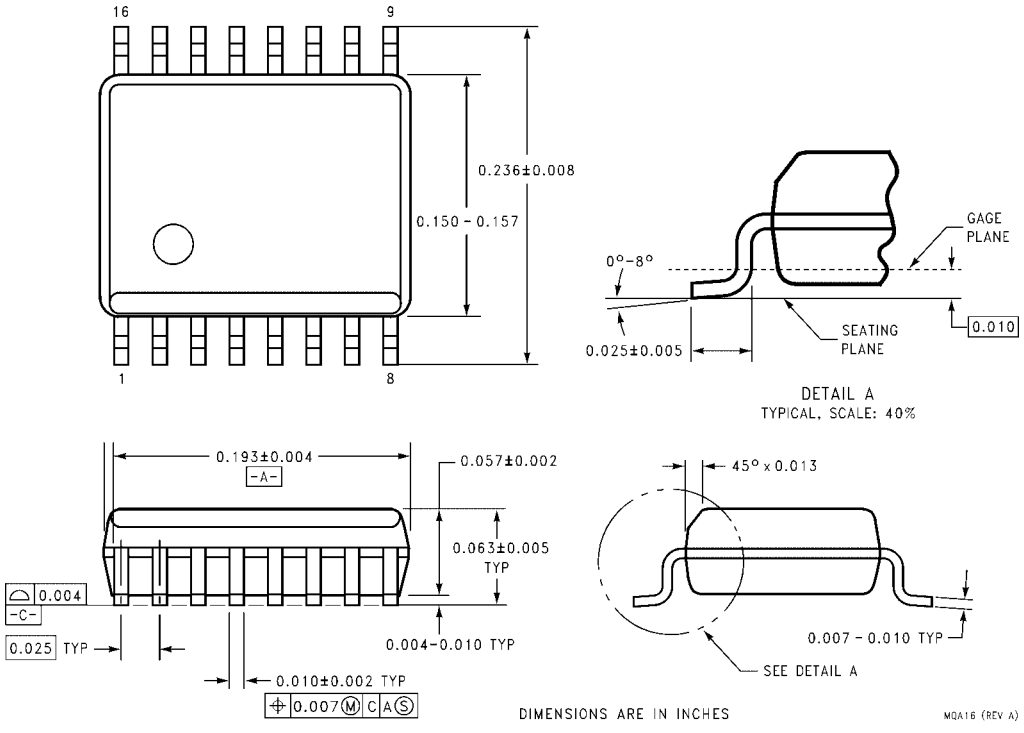



**FIGURE 2. AC Waveforms**

## Physical Dimensions inches (millimeters) unless otherwise noted

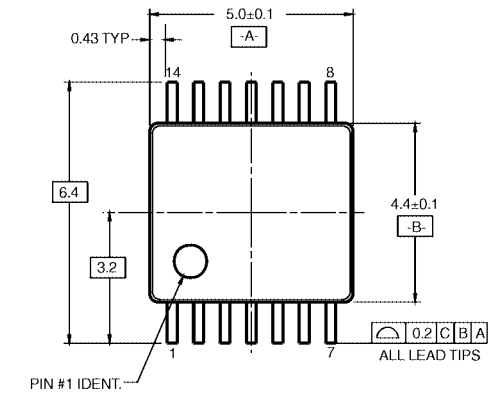


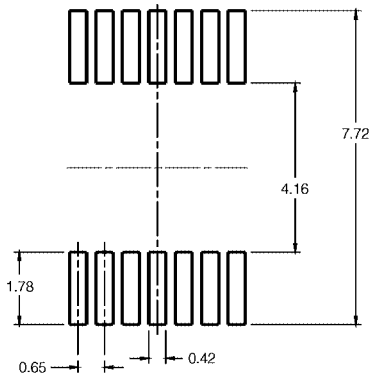

**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow**
**Package Number M14A**



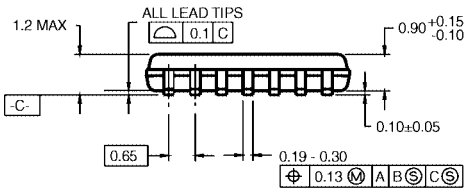

**16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide**
**Package Number MQA16**

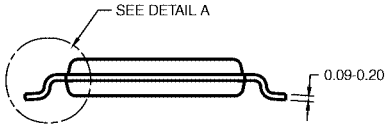
## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

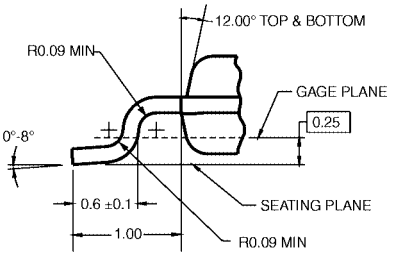



LAND PATTERN RECOMMENDATION




DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC14**

## Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.