GSC93BC46/56/66

3-wire Serial EEPROMs 1K/2K/4K

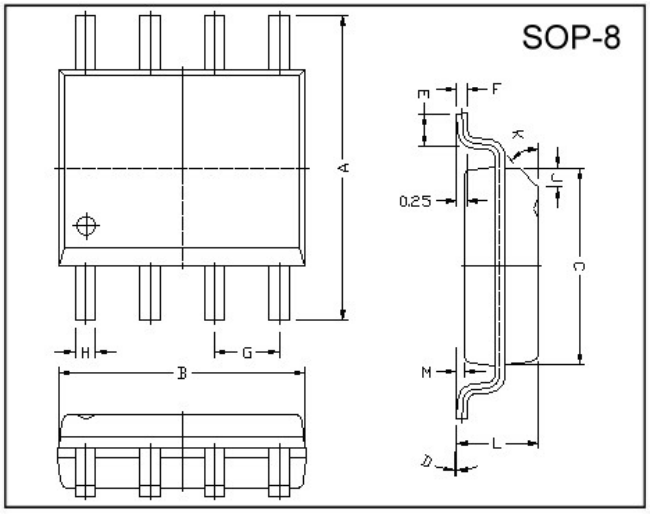
Description

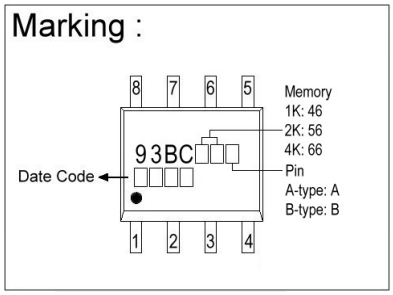
The GSC93BC family provides 1K, 2K and 4K of serial electrically erasable and programmable read-only memory (EEPROM). The wide Vdd range allows for low-voltage operation down to 1.8V and up to 5.5V. The device, fabricated using traditional CMOS EEPROM technology, is optimized for many industrial and commercial applications where low-voltage and low-power operation is essential. The device is accessed via a 3-wire serial interface.

Features

- Internally organized as 128x8 or 64x16 (1K), 256x8 or 128x16 (2K), 512x8 or 256x16 (4K)
- Wide-voltage range operation: 1.8V~5.5V
- 3-wire serial interface bus
- Date retention: 100years
- High endurance: 1,000,000 Write Cycles
- 2MHz (5V) clock rate
- Sequential read operation
- Self-timed write cycle (10ms max)

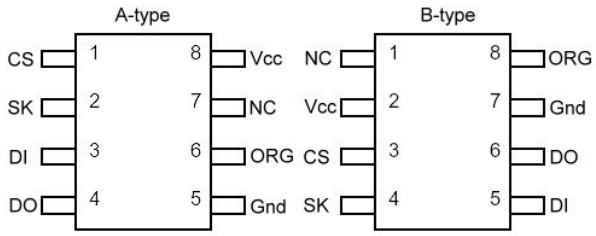
Package Dimensions





REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

Figure 1. Pin Configurations



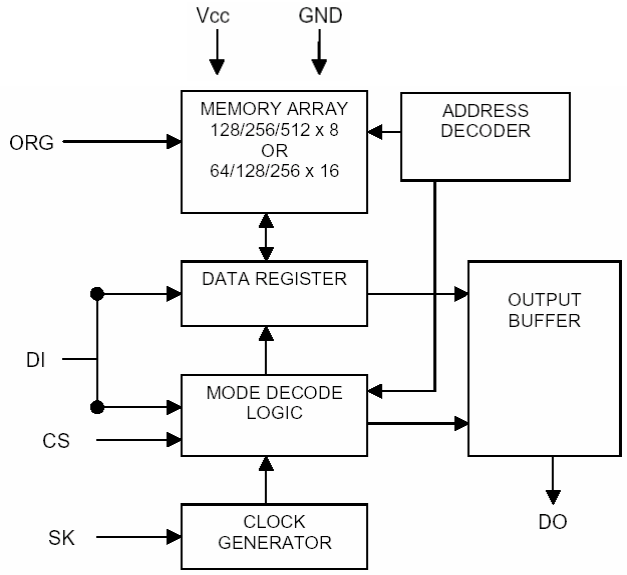
Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Gnd	Ground
Vcc	Power Supply
ORG	Internal Organization
NC	No Connect

Absolute Maximum Ratings

Parameter	Ratings	Unit
Voltage on Any Pin with Respect to Ground	-1.0 to Vcc +7.0	V
Maximum Operating Voltage	6.25	V
DC Output Current	5.0	mA
Operating Temperature Range	-55 ~ +125	℃
Storage Temperature Range	-65 ~ +150	℃

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of these specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2. Block Diagram



Notes

1. The ORG pin is used to select between x8 and x16.
When the pin is connected to Vcc, x16 mode is selected.
Otherwise, the ORG pin should be grounded in order to select x8 mode.

The interface foe the GSC93BC46/56/66 is accessed through four different signals:
Chip Select (CS), Data Input (DI), Data Output (DO), and Serial Data Clock (SK). The Chip Select (CS) signal must be pulled high before issuing a command through the Data Input (DI) pin. The Serial Data Clock (SK) signal is used in conjunction with the Data Input (DI) pin.

PIN Capacitance

Applicable over recommended operating range from T_A=25℃, f=1.0MHz, V_{CC}=+5V

Symbol	Test Condition	Max	Unit	Condition
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT}=0V
C_{IN}	Input Capacitance (CK, SK, DI)	5	pF	V_{IN}=0V

Note: 1. This parameter is characterized and not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_A=-40 ~ +85℃, V_{CC}=+1.8 ~ +5V (unless otherwise noted)

Parameter	Symbol	Test Condition	Min	TYP	Max	Unit
Supply Voltage	V_{CC1}		1.8	-	5.5	V
Supply Voltage	V_{CC2}		2.7	-	5.5	V
Supply Current	V_{CC3}		4.5	-	5.5	V
Supply Current V_{CC}=5.0V	I_{CC}	READ at 1MHz	-	0.5	2.0	mA
Supply Current V_{CC}=5.0V	I_{CC}	WRITE at 1MHz	-	0.5	2.0	mA
Standby Current V_{CC}=1.8V	I_{SB1}	CS=0V	-	0	0.1	µA
Standby Current V_{CC}=2.7V	I_{SB2}	CS=0V	-	6.0	10.0	µA
Standby Current V_{CC}=5.0V	I_{SB3}	CS=0V	-	17	30	µA
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-	0.1	3.0	µA
Output Leakage Current	I_{LO}	V_{IN}=0V to V_{CC}	-	0.1	3.0	µA
Input Low Level Input High Level	V_{IL1}(1) V_{IH1}(1)	2.7V< V_{CC} <5.5V	-0.6 2.0	-	0.8 V_{CC}+1	V
Input Low Level Input High Level	V_{IL2}(1) V_{IH2}(1)	1.8V< V_{CC} <2.7V	-0.6 V_{CC}x0.7	-	V_{CC}x0.3 V_{CC}+1	V
Output Low Level Output High Level	V_{OL1}(1) V_{OH1}(1)	2.7V< V_{CC} <5.5V; I_{OL}=2.1mA I_{OH}=-0.4mA	- 2.4	-	0.4 -	V
Output Low Level Output High Level	V_{OL2}(1) V_{OH2}(1)	1.8V< V_{CC} <2.7V; I_{OL}=0.15mA I_{OH}=-100uA	- V_{CC}-2	-	0.2 -	V

Note 1: V_{IL} and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from: T_A=-40 ~ +85℃, Vcc=As specified, C_L=1 TTL Gate & 100pF (unless otherwise noted)

Parameter	Symbol	Test Condition		Min	TYP	Max	Unit
Clock Frequency, SK	f_{SK}	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V		0 0 0	-	2 1 0.25	MHz
SK High Time	t_{SKH}	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V		250 250 1000	-	-	ns
SK Low Time	t_{SKL}	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V		250 250 1000	-	-	ns
Minimum CS Low Time	t_{CS}	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V		250 250 1000	-	-	ns
CS Setup Time	t_{CSS}	Relative To SK	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V	50 50 200	-	-	ns
DI Setup Time	t_{DIS}	Relative To SK	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V	100 100 400	-	-	ns
CS Hold Time	t_{CSH}	Relative To SK		0	-	-	ns
DI Hold Time	t_{DIH}	Relative To SK	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V	100 100 400	-	-	ns
Output Delay to “1”	t_{PD1}	AC Test	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V	-	-	250 250 1000	ns
Output Delay to “0”	t_{PD0}	AC Test	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V	-	-	250 250 1000	ns
CS to Status Valid	t_{SV}	AC Test	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V	-	-	250 250 1000	ns
CS to DO in High Impedance	t_{DF}	AC Test CS=V_{IL}	4.5V< V_{CC} <5.5V 2.7V< V_{CC} <5.5V 1.8V< V_{CC} <5.5V	-	-	100 100 400	ns
Write Cycle Time	t_{WP}		1.8V< V_{CC} <5.5V	-	3	10	ms
5.0V, 25℃	Endurance (1)			1M	-	-	Write Cycles

Note: 1. This parameter is characterized and not 100% tested.

Instruction set for the GSC93BC46

Instruction	SB	OP Code	Address		Data		Comment
			X8	X16	X8	X16	
READ	1	10	A_6 ~ A_0	A_5 ~ A_0			Reads data stored at specified memory location.
EWEN	1	00	11xxxxx	11xxxx			Write enable command (must be issued before any erase or write operation).
ERASE	1	11	A_6 ~ A_0	A_5 ~ A_0			Erases memory location A_n~A_0
WRITE	1	01	A_6 ~ A_0	A_5 ~ A_0	D_7 ~ D_0	D_{15} ~ D_0	Write to memory location A_n~A_0
ERAL	1	00	10xxxxx	10xxxx			Erases all memory locations. Valid only at V_{CC}=4.5V to 5.5V
WRAL	1	00	01xxxxx	01xxxx	D_7 ~ D_0	D_{15} ~ D_0	Write all memory locations. Valid only at V_{CC}=4.5V to 5.5V
EWDS	1	00	00xxxxx	00xxxx			Disables all erase or write instructions

Note : The X's in the address field represent don't care values and must be clocked.

Instruction set for the GSC93BC56/66

Instruction	SB	OP Code	Address		Data		Comment
			X8	X16	X8	X16	
READ	1	10	A_8 ~ A_0	A_7 ~ A_0			Reads data stored at specified memory location.
EWEN	1	00	11xxxxxxx	11xxxxxx			Write enable command (must be issued before any erase or write operation).
ERASE	1	11	A_8 ~ A_0	A_7 ~ A_0			Erases memory location A_n~A_0
WRITE	1	01	A_8 ~ A_0	A_7 ~ A_0	D_7~D_0	D_{15}~D_0	Write to memory location A_n~A_0
ERAL	1	00	10xxxxxxx	10xxxxxx			Erases all memory locations. Valid only at V_{CC}=4.5V to 5.5V
WRAL	1	00	01xxxxxxx	01xxxxxx	D_7~D_0	D_{15}~D_0	Write all memory locations. Valid only at V_{CC}=4.5V to 5.5V
EWDS	1	00	00xxxxxxx	00xxxxxx			Disables all erase or write instructions

Note : The X's in the address field represent don't care values and must be clocked.

Function Description

The GSC93BC46/56/66 support 7 different instructions, which must be clocked serially using the CS, SK and DI pins. Before sending each of these instructions, the CS pin must be pulled high followed by a START bit (logic '1'). The next sequence includes a 2-bit Op Code and usually an 8 or 16-bit address. The next description describes the various functions in the chip.

READ (READ): The Read (READ) instruction includes the Op Code ("10") followed by the memory address location to be read. After the instruction and address is sent, the data from the memory location can be clocked out using the serial output pin DO. The data changes on the rising edge of the clock, so the falling edge can be used to strobe the output.

Note that during shifting the last address bit, the DO pin is a dummy bit (logic "0").

ERASE/WRITE (EWEN)): When the chip is first powered-on, no erase or write instructions can be issued. Only when the Erase/Write Enable (EWEN) instruction is sent will the system be allowed to write to the chip. The EWEN command only needs to be issued once after being powered-on. To disable the chip again, the Erase/Write Disable (EWDS) command can be used.

ERASE (ERASE): The Erase (ERASE) instruction clears the designated memory location to a logic '1' state. After the Op Code and address location is inputted, the chip will enter into an erase cycle. When the cycle completes, the chip will automatically enter into standby mode.

WRITE (WRITE): The Write (WRITE) instruction is used to write to a specific memory location. If word mode (x16) is selected, then 16 bits of data will be written into the location. If byte mode (x8) is chosen, then 8 bits of data will be written into the location. The write cycle will begin automatically after the 8 or 16 bits are shifted into the chip.

ERASE ALL (ERAL): The Erase All (ERAL) instruction is primarily used for testing purposes and only functions when V_{CC}=4.5V to 5.5V. This instruction will clear the entire memory array to '1'.

WRITE ALL (WRAL): The Write All (WRAL) instruction will program the entire memory array according to the 8 or 16-bit data pattern provided. The instruction will only be valid when V_{CC}=4.5V to 5.5V.

ERASE/WRITE DISABLE (EWDS): The Erase/Write Disable (EWDS) instruction blocks any kind of erase or program operations from modifying the contents of the memory array. This instruction should be executed after erasing or programming to prevent accidental data loss.

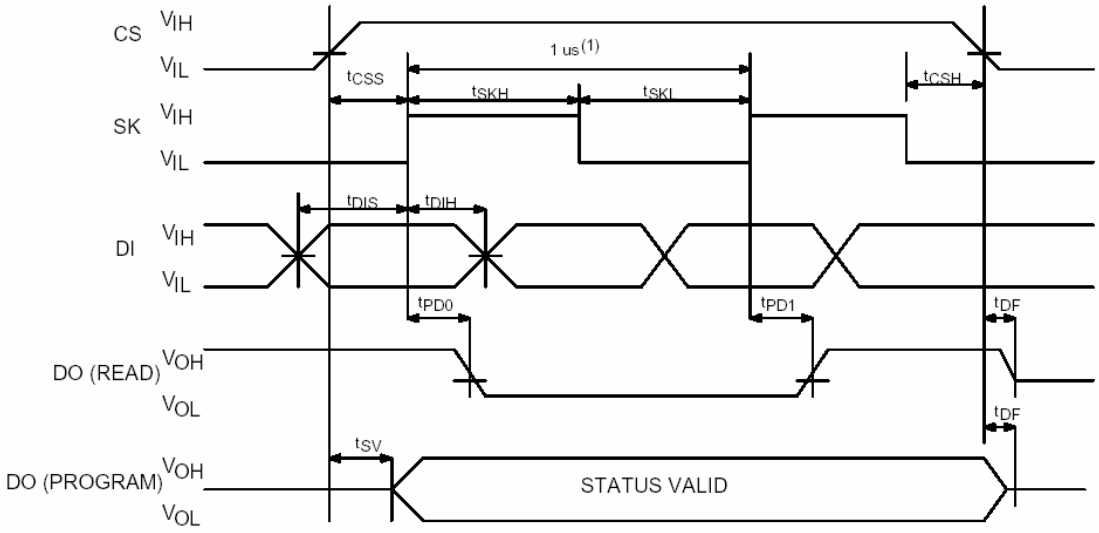
Note also that the READ instruction will operate regardless of whether the chip is disabled from program and write operations.

Ready/Busy

To determine whether the chip has completed an erase or write operation, the CS signal can be pulled LOW for a minimum of 250ns (t_{CS}) and then pulled back HIGH to enter Ready/Busy mode. If the chip is currently in the programming cycle, t_{WP}, then the DO pin will go low (logical "0"). When the write cycle completes, the DO pin is pulled high (logical "1") to indicate that the part can receive anther instruction. Note that the Ready/Busy polling cannot be done if the chip has already finished and returned back to standby mode.

Timing Diagrams

Synchronous Data Timing



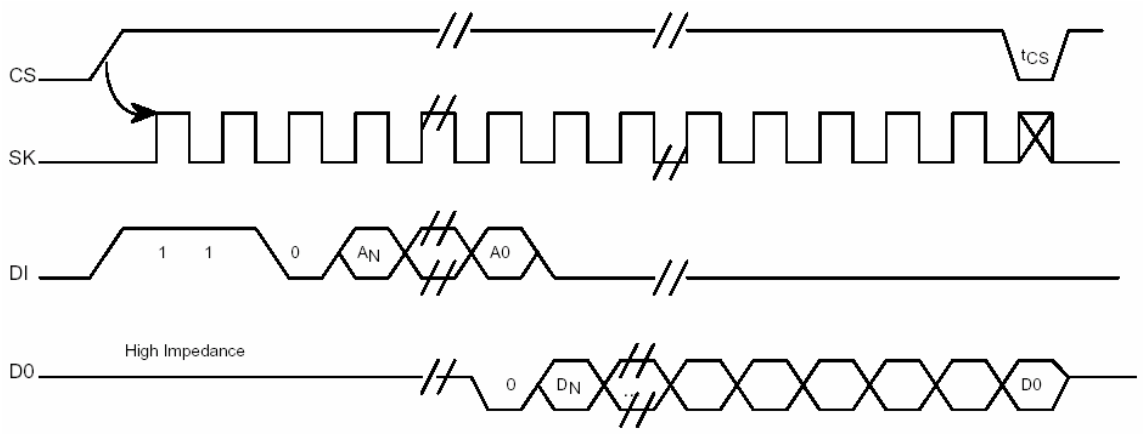
Note (1): This is the minimum SK period.

Organization Key for TIMING Diagrams

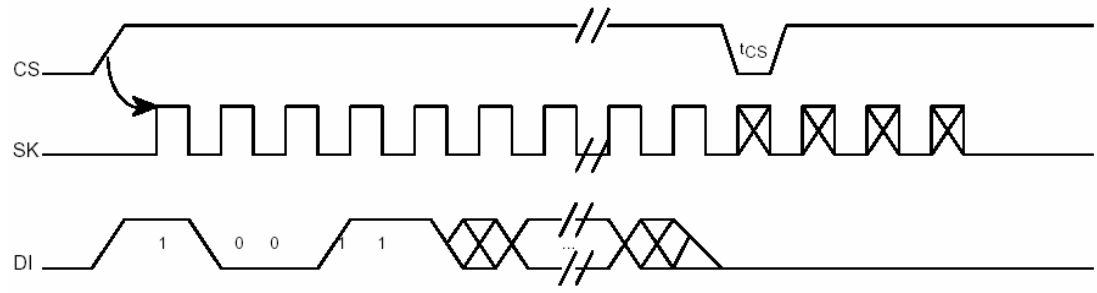
I/O	GSC93BC46(1K)		GSC93BC56(2K)		GSC93BC66(4K)	
	X8	X16	X8	X16	X8	X16
A_N	A_6	A_5	A_8(1)	A_7(2)	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}

Note:
1. A_8 is a DON'T CARE value, but the extra clock is required.
2. A_7 is a DON'T CARE value, but the extra clock is required.

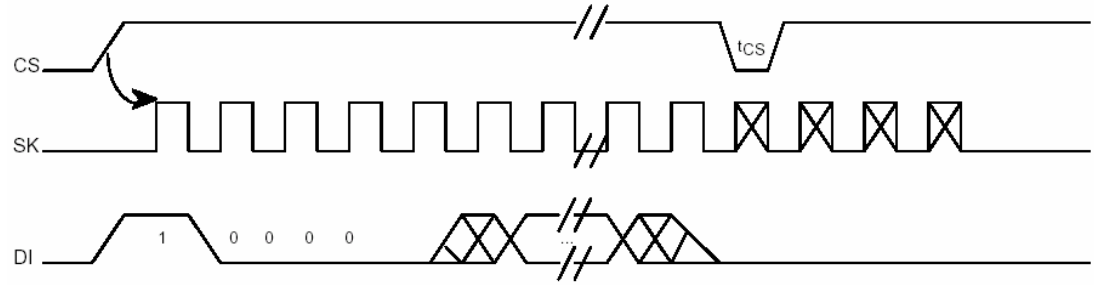
READ Timing



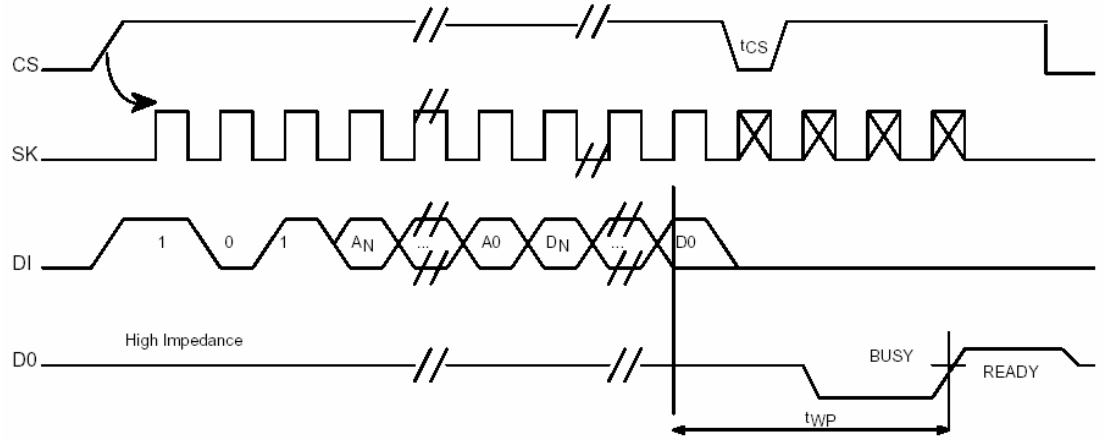
EWEN Timing



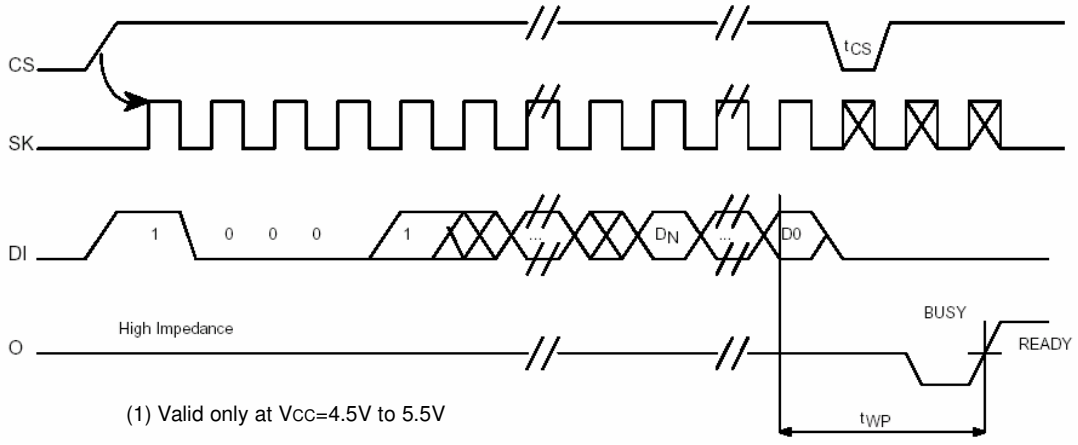
EWDS Timing



WRITE Timing

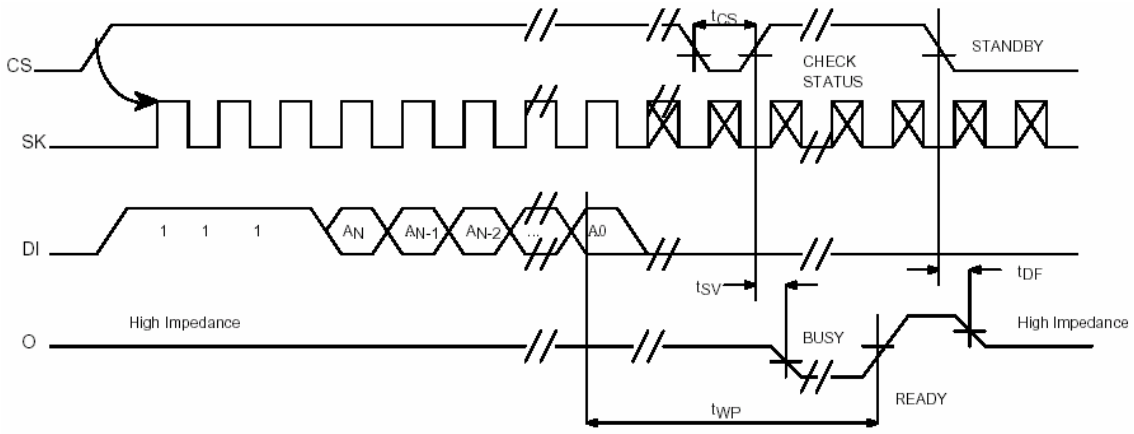


WRAL Timing (1)

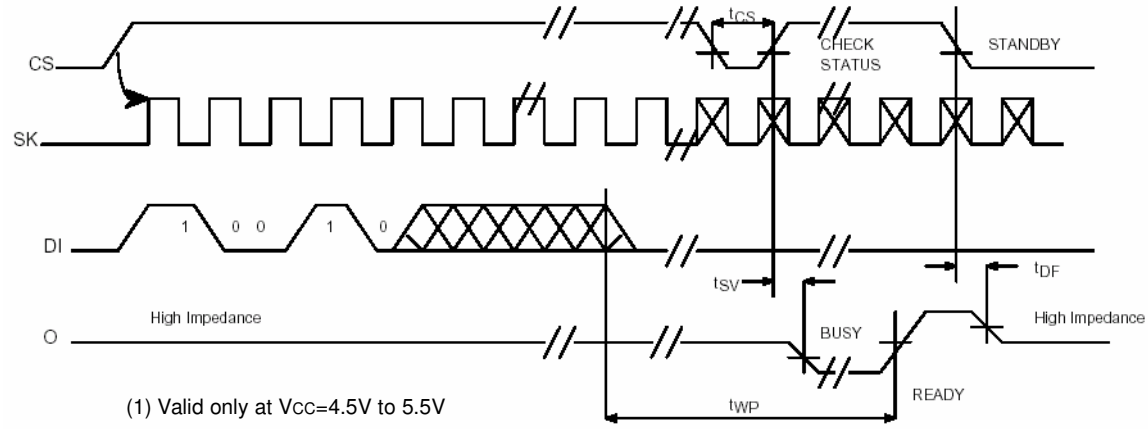


(1) Valid only at Vcc=4.5V to 5.5V

ERASE Timing



ERAL Timing (1)



(1) Valid only at Vcc=4.5V to 5.5V

GSC93BC46 Ordering Information

Ordering Code	Package	Pin Type	Operating Ranges
GSC93BC46AI	SOP-8	A	Industrial (-40 ~ +85℃)
GSC93BC46BI		B	

GSC93BC56 Ordering Information

Ordering Code	Package	Pin Type	Operating Ranges
GSC93BC56AI	SOP-8	A	Industrial (-40 ~ +85℃)
GSC93BC56BI		B	

GSC93BC66 Ordering Information

Ordering Code	Package	Pin Type	Operating Ranges
GSC93BC66AI	SOP-8	A	Industrial (-40 ~ +85℃)
GSC93BC66BI		B	

Product Ordering Information

GSC93BCXXYZ

G=GTM

SC=SOP-8

93=Device Type

Supply Voltage
BC=1.8V to 5.5V

Device Function
46=1 Kbit (128x8 or 64x16)
56=2 Kbit (256x8 or 128x16)
66=4 Kbit (512x8 or 256x16)

Pin Type
A=A-Type
B=B-Type

Temperature
I=Industrial (-40 ~ +85℃)

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