

# HM514260A/AL, HM51S4260A/AL Series

**262,144-Word x 16-Bit Dynamic Random Access Memory****■ DESCRIPTION**

The Hitachi HM514260A/AL are CMOS dynamic RAM organized as 262,144-word x 16-bit. HM514260A/AL have realized higher density, higher performance and various functions by employing 0.8  $\mu$ m CMOS process technology and some new CMOS circuit design technologies. The HM514260A/AL offer fast page mode as a high speed access mode.

Multiplexed address input permits the HM514260A/AL to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP and standard 400 mil 40-pin plastic TSOPII.

Internal refresh timer enables HM51S4260A/AL self refresh operation.

**■ FEATURES**

- Single 5V ( $\pm 10\%$ )
- High Speed
  - Access Time ..... 70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 825 mW/770 mW/688 mW (max)
  - Standby Mode ..... 11 mW (max)
  - 1.1 mW (max) (L-Version)
- Fast Page Mode Capability
- 512 Refresh Cycles ..... 8 ms
  - 128 ms (L-Version)
- 2  $\overline{\text{CAS}}$  Byte Control
- 2 Variations of Refresh
  - $\overline{\text{RAS}}$  Only Refresh
  - $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh
- Battery Back-up Operation (L-Version)
- Self-Refresh Operation (HM51S4260A/AL)

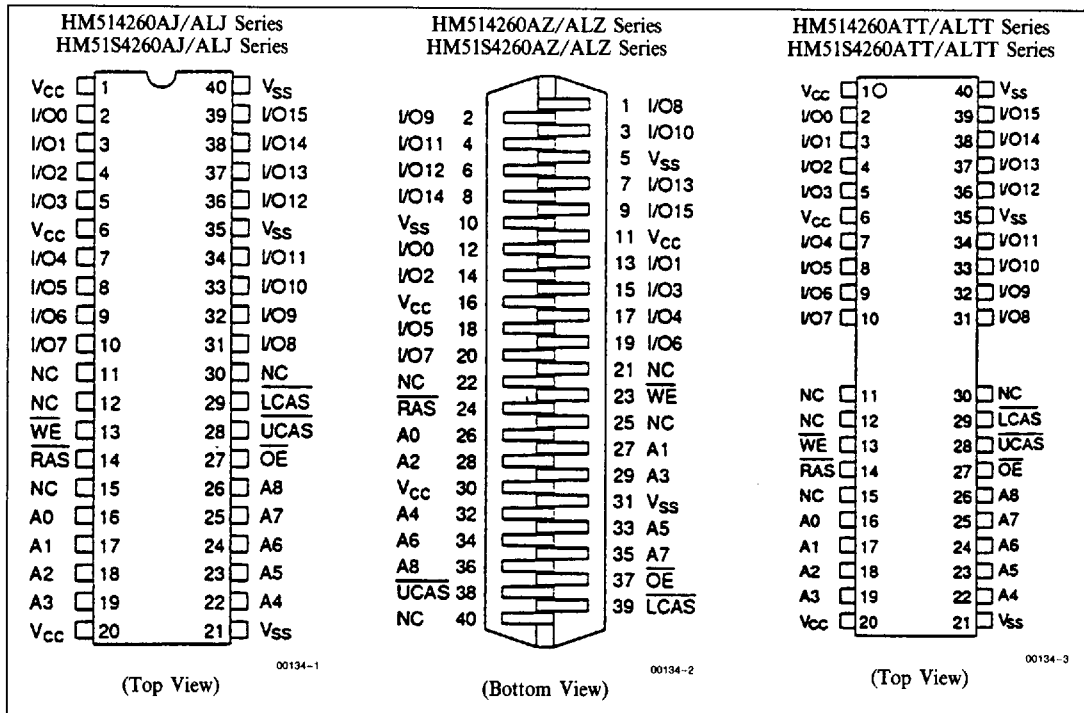
**■ ORDERING INFORMATION**

Part No.	Access Time	Package
HM514260AJ-7	70 ns	400 mil 40-pin
HM514260AJ-8	80 ns	Plastic SOJ
HM514260AJ-10	100 ns	(CP-40DA)
HM514260AZ-7	70 ns	475 mil 40-pin
HM514260AZ-8	80 ns	Plastic ZIP
HM514260AZ-10	100 ns	(ZP-40)
HM514260ATT-7	70 ns	400 mil 40-pin
HM514260ATT-8	80 ns	Plastic TSOPII
HM514260ATT-10	100 ns	(TTP-40DB)
HM514260ARR-7	70 ns	400 mil 40-pin
HM514260ARR-8	80 ns	Plastic TSOPII
HM514260ARR-10	100 ns	(TTP-40DB)
HM514260ALJ-7	70 ns	400 mil 40-pin
HM514260ALJ-8	80 ns	Plastic SOJ
HM514260ALJ-10	100 ns	(CP-40DA)
HM514260ALZ-7	70 ns	475 mil 40-pin
HM514260ALZ-8	80 ns	Plastic ZIP
HM514260ALZ-10	100 ns	(ZP-40)
HM514260ALTT-7	70 ns	400 mil 40-pin
HM514260ALTT-8	80 ns	Plastic TSOPII
HM514260ALTT-10	100 ns	(TTP-40DB)
HM514260ALRR-7	70 ns	400 mil 40-pin
HM514260ALRR-8	80 ns	Plastic TSOPII
HM514260ALRR-10	100 ns	(TTP-40DB)

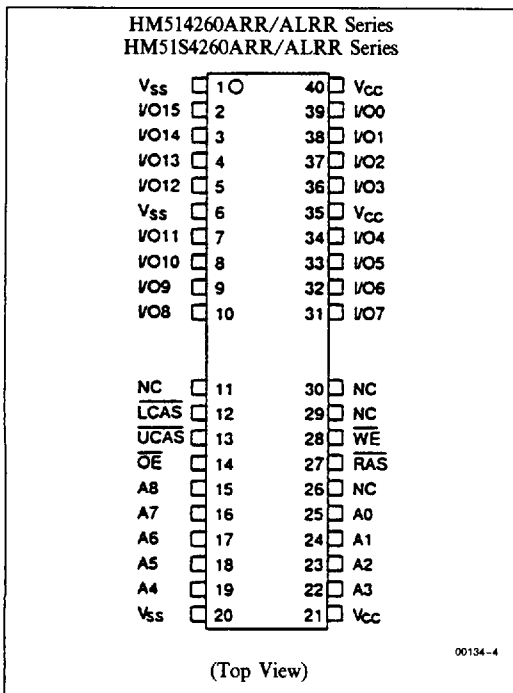
Part No.	Access Time	Package
HM51S4260AJ-7	70 ns	400 mil 40-pin
HM51S4260AJ-8	80 ns	Plastic SOJ
HM51S4260AJ-10	100 ns	(CP-40DA)
HM51S4260AZ-7	70 ns	475 mil 40-pin
HM51S4260AZ-8	80 ns	Plastic ZIP
HM51S4260AZ-10	100 ns	(ZP-40)
HM51S4260ATT-7	70 ns	400 mil 40-pin
HM51S4260ATT-8	80 ns	Plastic TSOPII
HM51S4260ATT-10	100 ns	(TTP-40DB)
HM51S4260ARR-7	70 ns	400 mil 40-pin
HM51S4260ARR-8	80 ns	Plastic TSOPII
HM51S4260ARR-10	100 ns	(TTP-40DB)
HM51S4260ALJ-7	70 ns	400 mil 40-pin
HM51S4260ALJ-8	80 ns	Plastic SOJ
HM51S4260ALJ-10	100 ns	(CP-40DA)
HM51S4260ALZ-7	70 ns	475 mil 40-pin
HM51S4260ALZ-8	80 ns	Plastic ZIP
HM51S4260ALZ-10	100 ns	(ZP-40)
HM51S4260ALTT-7	70 ns	400 mil 40-pin
HM51S4260ALTT-8	80 ns	Plastic TSOPII
HM51S4260ALTT-10	100 ns	(TTP-40DB)
HM51S4260ALRR-7	70 ns	400 mil 40-pin
HM51S4260ALRR-8	80 ns	Plastic TSOPII
HM51S4260ALRR-10	100 ns	(TTP-40DB)

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■ PIN ARRANGEMENT



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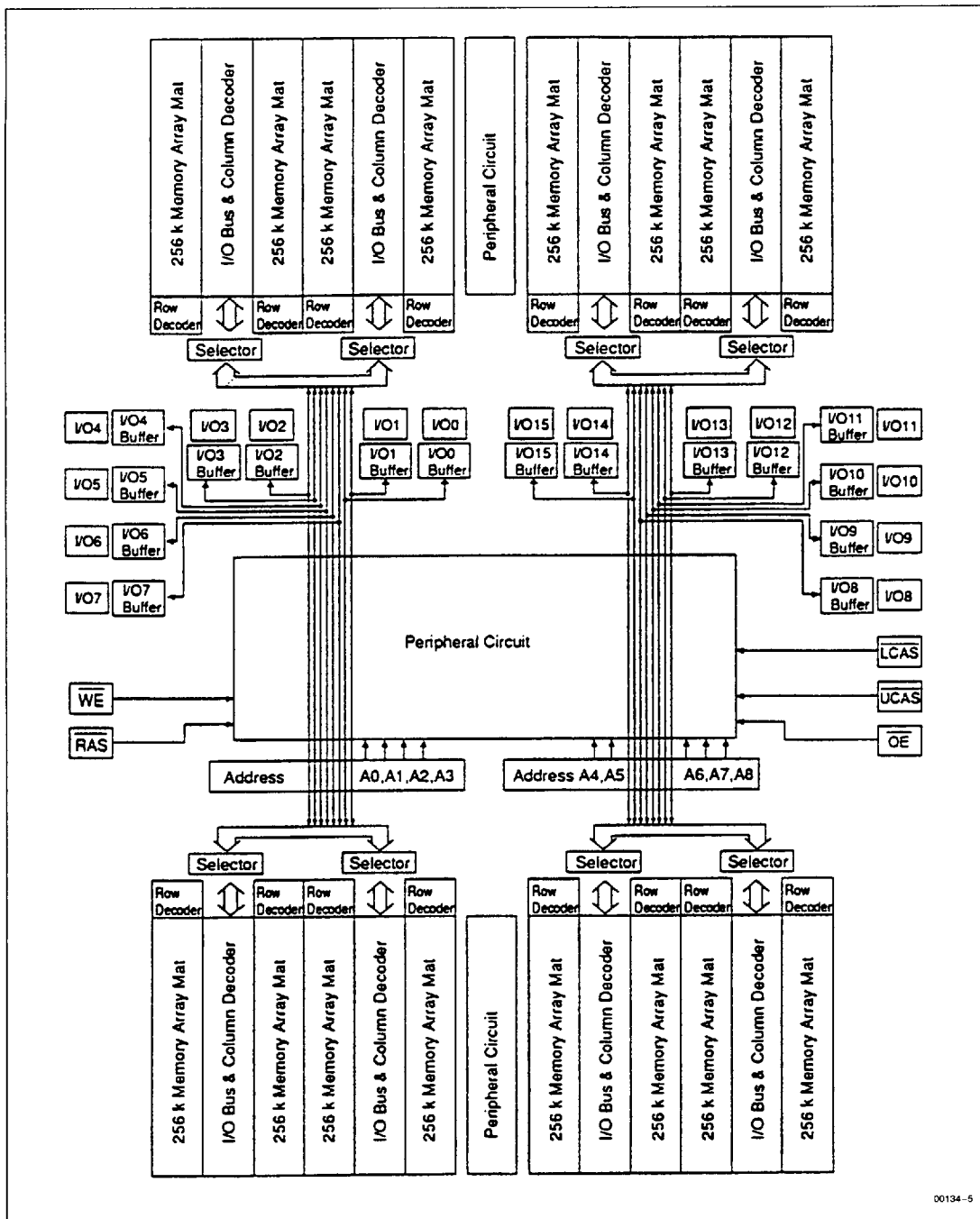


■ PIN DESCRIPTION

Pin Name	Function
A <sub>0</sub> -A <sub>8</sub>	Address Input —Row Address A <sub>0</sub> -A <sub>8</sub> —Column Address A <sub>0</sub> -A <sub>8</sub> —Refresh Address A <sub>0</sub> -A <sub>8</sub>
I/O <sub>0</sub> -I/O <sub>15</sub>	Data-in/Data-out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS/LCAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	Power (+ 5V)
V <sub>SS</sub>	Ground

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■ BLOCK DIAGRAM



00134-5

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**■ TRUTH TABLE**

Inputs					I/O		Operation
RAS	LCAS	UCAS	WE	OE	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	D <sub>out</sub>	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D <sub>out</sub>	Upper Byte Read
L	L	L	H	L	D <sub>out</sub>	D <sub>out</sub>	Word Read
L	L	H	L	H	D <sub>in</sub>	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D <sub>in</sub>	Upper Byte Write
L	L	L	L	H	D <sub>in</sub>	D <sub>in</sub>	Word Write
L	L	L	H	H	High-Z	High-Z	CBR Refresh or Self Refresh
H to L	L	H	—	—	High-Z	High-Z	
H to L	H	L	—	—	High-Z	High-Z	
H to L	L	L	—	—	High-Z	High-Z	

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**■ ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>T</sub>	-1.0 to +7.0	V
Supply Voltage Relative to V <sub>SS</sub>	V <sub>CC</sub>	-1.0 to +7.0	V
Short Circuit Output Current	I <sub>out</sub>	50	mA
Power Dissipation	P <sub>T</sub>	1.0	W
Operating Temperature	T <sub>opr</sub>	0 to +70	°C
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C

**■ ELECTRICAL CHARACTERISTICS**
**• Recommended DC Operating Conditions (T<sub>A</sub> = 0 to +70°C)<sup>2</sup>**

Parameter	Symbol	Min	Typ	Max	Unit	Note	
Supply Voltage	V <sub>SS</sub>	0	0	0	V		
	V <sub>CC</sub>	4.5	5.0	5.5	V	1	
Input High Voltage	V <sub>IH</sub>	2.4	—	6.5	V	1	
Input Low Voltage	(I/O Pin)	V <sub>IL</sub>	-1.0	—	0.8	V	1
	(Others)	V <sub>IL</sub>	-2.0	—	0.8	V	1

- Notes: 1. All voltage referenced to V<sub>SS</sub>.  
 2. The supply voltage with all V<sub>CC</sub> pins must be on the same level.  
 The supply voltage with all V<sub>SS</sub> pins must be on the same level.

**HM514260A/AL, HM51S4260A/AL Series**

• DC Electrical Characteristics (T<sub>A</sub> = 0 to +70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V)

Parameter	Symbol	HM514260A/AL-7 HM51S4260A/AL-7		HM514260A/AL-8 HM51S4260A/AL-8		HM514260A/AL-10 HM51S4260A/AL-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I <sub>CC1</sub>	—	150	—	140	—	125	mA	RAS Cycling LCAS or UCAS Cycling t <sub>RC</sub> = min	1, 2
Standby Current	I <sub>CC2</sub>	—	2	—	2	—	2	mA	TTL Interface RAS, LCAS, UCAS = V <sub>IH</sub> D <sub>out</sub> = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface RAS, LCAS, UCAS, WE OE ≥ V <sub>CC</sub> - 0.2V, D <sub>out</sub> = High-Z	
Standby Current (L-Version)		—	200	—	200	—	200	μA	CMOS Interface RAS, LCAS, OE, WE UCAS ≥ V <sub>CC</sub> - 0.2V, D <sub>out</sub> = High-Z	
RAS Only Refresh Current	I <sub>CC3</sub>	—	140	—	130	—	110	mA	t <sub>RC</sub> = min	2
Standby Current	I <sub>CC5</sub>	—	5	—	5	—	5	mA	RAS = V <sub>IH</sub> , LCAS or UCAS = V <sub>IL</sub> , D <sub>out</sub> = Enable	1
CAS Before RAS Refresh Current	I <sub>CC6</sub>	—	140	—	130	—	110	mA	t <sub>RC</sub> = min	2
Fast Page Mode Current	I <sub>CC7</sub>	—	130	—	120	—	110	mA	t <sub>PC</sub> = min	1, 3
Battery Back-up Current (Standby with CBR Refresh) (L-Version)	I <sub>CC10</sub>	—	300	—	300	—	300	μA	Standby: CMOS Interface D <sub>out</sub> = High-Z CBR Refresh: t <sub>RC</sub> = 250 μs t <sub>RAS</sub> ≤ 1 μs, LCAS, UCAS = V <sub>IL</sub> WE, OE = V <sub>IH</sub>	4
Self-Refresh Mode Current (HM51S4260A)	I <sub>CC11</sub>	—	1	—	1	—	1	mA	CMOS Interface RAS, LCAS, UCAS ≤ 0.2V D <sub>out</sub> = High-Z	
Self-Refresh Mode Current (HM51S4260AL)		—	200	—	200	—	200	μA	CMOS Interface RAS, LCAS, UCAS ≤ 0.2V D <sub>out</sub> = High-Z	
Input Leakage Current	I <sub>LI</sub>	-10	10	-10	10	-10	10	μA	0V ≤ V <sub>in</sub> ≤ 6.5V	
Output Leakage Current	I <sub>LO</sub>	-10	10	-10	10	-10	10	μA	0V ≤ V <sub>out</sub> ≤ 6.5V D <sub>out</sub> = Disable	
Output High Voltage	V <sub>OH</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High I <sub>out</sub> = -5.0 mA	
Output Low Voltage	V <sub>OL</sub>	0	0.4	0	0.4	0	0.4	V	Low I <sub>out</sub> = 4.2 mA	

- Notes:
- I<sub>CC</sub> depends on output load condition when the device is selected. I<sub>CC</sub> max is specified at the output open condition.
  - Address can be changed ≤ 1 time while RAS = V<sub>IL</sub>.
  - Address can be changed ≤ 1 time while LCAS and UCAS = V<sub>IH</sub>.
  - V<sub>IH</sub> ≥ V<sub>CC</sub> - 0.2V, 0 ≤ V<sub>IL</sub> ≤ 0.2V. Address can be changed ≤ 1 time while RAS = V<sub>IL</sub>.
  - All the V<sub>CC</sub> pins shall be supplied with the same voltage.  
All the V<sub>SS</sub> pins shall be supplied with the same voltage.

HM514260A/AL, HM51S4260A/AL Series

• Capacitance ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ )

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	$C_{I1}$	—	5	pF	1
Input Capacitance (Clocks)	$C_{I2}$	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2.  $\overline{LCAS}$  and  $\overline{UCAS} = V_{IH}$  to disable  $D_{out}$ .

• AC Characteristics ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ )<sup>1, 14, 15, 17, 18</sup>

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8V, 2.4V
- Output load: 2 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514260A/AL-7 HM51S4260A/AL-7		HM514260A/AL-8 HM51S4260A/AL-8		HM514260A/AL-10 HM51S4260A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	$t_{RC}$	130	—	150	—	180	—	ns	
RAS Precharge Time	$t_{RP}$	50	—	60	—	70	—	ns	
RAS Pulse Width	$t_{RAS}$	70	10000	80	10000	100	10000	ns	
CAS Pulse Width	$t_{CAS}$	20	10000	20	10000	25	10000	ns	23
Row Address Setup Time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row Address Hold Time	$t_{RAH}$	10	—	10	—	15	—	ns	
Column Address Setup Time	$t_{ASC}$	0	—	0	—	0	—	ns	19
Column Address Hold Time	$t_{CAH}$	15	—	15	—	20	—	ns	19
RAS to CAS Delay Time	$t_{RCD}$	20	50	20	60	25	75	ns	8
RAS to Column Address Delay Time	$t_{RAD}$	15	35	15	40	20	55	ns	9
RAS Hold Time	$t_{RSH}$	20	—	20	—	25	—	ns	
CAS Hold Time	$t_{CSH}$	70	—	80	—	100	—	ns	
CAS to RAS Precharge Time	$t_{CRP}$	15	—	15	—	15	—	ns	20, 24
$\overline{OE}$ to $D_{in}$ Delay Time	$t_{ODD}$	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from $D_{in}$	$t_{DZO}$	0	—	0	—	0	—	ns	
CAS Setup Time from $D_{in}$	$t_{DZC}$	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	$t_T$	3	50	3	50	3	50	ns	7
Refresh Period	$t_{REF}$	—	8	—	8	—	8	ms	
Refresh Period (L-Version)	$t_{REF}$	—	128	—	128	—	128	ms	

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HM514260A/AL, HM51S4260A/AL Series

Read Cycle

Parameter	Symbol	HM514260A/AL-7 HM51S4260A/AL-7		HM514260A/AL-8 HM51S4260A/AL-8		HM514260A/AL-10 HM51S4260A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t <sub>RAC</sub>	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t <sub>CAC</sub>	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t <sub>AA</sub>	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{OE}$	t <sub>OAC</sub>	—	20	—	20	—	25	ns	23
Read Command Setup Time	t <sub>RCS</sub>	0	—	0	—	0	—	ns	19
Read Command Hold Time to $\overline{CAS}$	t <sub>RCH</sub>	0	—	0	—	0	—	ns	16, 19
Read Command Hold Time to $\overline{RAS}$	t <sub>RRH</sub>	0	—	0	—	0	—	ns	16
Column Address to $\overline{RAS}$ Lead Time	t <sub>RAL</sub>	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t <sub>OFF1</sub>	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t <sub>OFF2</sub>	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to $D_{in}$ Delay Time	t <sub>CDD</sub>	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514260A/AL-7 HM51S4260A/AL-7		HM514260A/AL-8 HM51S4260A/AL-8		HM514260A/AL-10 HM51S4260A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t <sub>WCS</sub>	0	—	0	—	0	—	ns	10, 19
Write Command Hold Time	t <sub>WCH</sub>	15	—	15	—	20	—	ns	19
Write Command Pulse Width	t <sub>WP</sub>	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t <sub>RWL</sub>	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t <sub>CWL</sub>	20	—	20	—	25	—	ns	21
Data-in Setup Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	11
Data-in Hold Time	t <sub>DH</sub>	15	—	15	—	20	—	ns	11
$\overline{CAS}$ to $\overline{OE}$ Delay Time	t <sub>COD</sub>	—	0	—	0	—	0	ns	23

Read-Modify-Write Cycle

Parameter	Symbol	HM514260A/AL-7 HM51S4260A/AL-7		HM514260A/AL-8 HM51S4260A/AL-8		HM514260A/AL-10 HM51S4260A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t <sub>RWC</sub>	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t <sub>RWD</sub>	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t <sub>CWD</sub>	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t <sub>AWD</sub>	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ Hold Time from $\overline{WE}$	t <sub>OEH</sub>	20	—	20	—	25	—	ns	

**Refresh Cycle**

Parameter	Symbol	HM514260A/AL-7 HM51S4260A/AL-7		HM514260A/AL-8 HM51S4260A/AL-8		HM514260A/AL-10 HM51S4260A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
CAS Setup Time (CAS Before RAS Refresh Cycle)	t <sub>CSR</sub>	10	—	10	—	10	—	ns	19
CAS Hold Time (CAS Before RAS Refresh Cycle)	t <sub>CHR</sub>	10	—	10	—	10	—	ns	20
RAS Precharge to CAS Hold Time	t <sub>RPC</sub>	10	—	10	—	10	—	ns	19
CAS Precharge Time in Normal Mode	t <sub>CPN</sub>	10	—	10	—	10	—	ns	22

**Fast Page Mode Cycle**

Parameter	Symbol	HM514260A/AL-7 HM51S4260A/AL-7		HM514260A/AL-8 HM51S4260A/AL-8		HM514260A/AL-10 HM51S4260A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t <sub>PC</sub>	45	—	50	—	55	—	ns	
Fast Page Mode CAS Precharge Time	t <sub>CP</sub>	10	—	10	—	10	—	ns	22
Fast Page Mode RAS Pulse Width	t <sub>RASC</sub>	—	100000	—	100000	—	100000	ns	12
Access Time from CAS Precharge	t <sub>ACP</sub>	—	40	—	45	—	50	ns	3, 13, 20
RAS Hold Time from CAS Precharge	t <sub>RHCP</sub>	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle CAS Precharge to WE Delay Time	t <sub>CPW</sub>	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t <sub>PCM</sub>	95	—	100	—	110	—	ns	

**Self-Refresh Mode**

Parameter	Symbol	HM51S4260A/AL-7		HM51S4260A/AL-8		HM51S4260A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
RAS Pulse Width (Self-Refresh)	t <sub>RASS</sub>	100	—	100	—	100	—	μs	
RAS Precharge Time (Self-Refresh)	t <sub>RPS</sub>	130	—	150	—	180	—	ns	
CAS Hold Time (Self-Refresh)	t <sub>CHS</sub>	-50	—	-50	—	-50	—	ns	21

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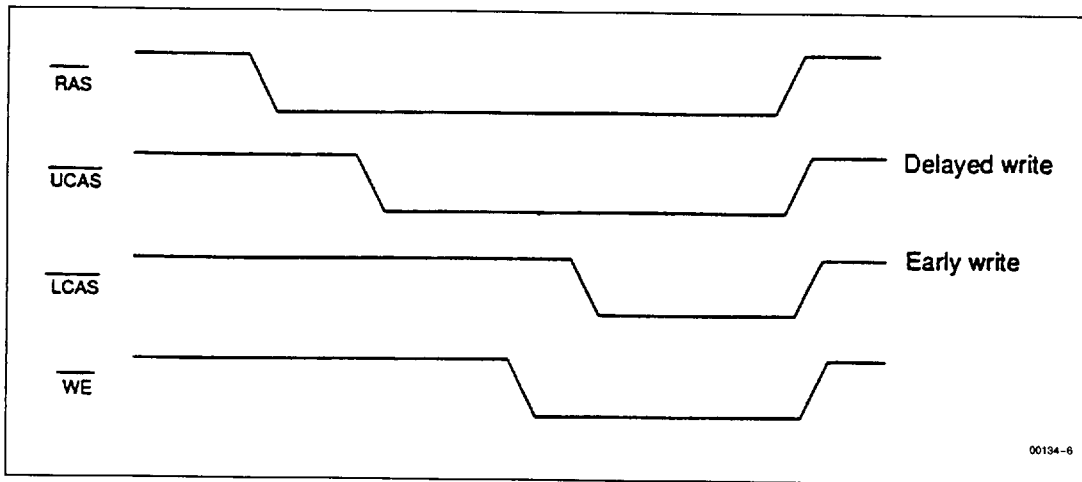
## HM514260A/AL, HM51S4260A/AL Series

- Notes:
1. AC measurements assume  $t_T = 5$  ns.
  2. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  4. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ .
  5. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \geq t_{RAD}(\text{max})$ .
  6.  $t_{OFF}(\text{max})$  defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
  7.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  8. Operation with the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RCD}(\text{max})$  is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
  9. Operation with the  $t_{RAD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RAD}(\text{max})$  is specified as a reference point only, if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
  10.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}(\text{min})$ ,  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{AWD} \geq t_{AWD}(\text{min})$  and  $t_{CPW} \geq t_{CPW}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  11. These parameters are referred to  $\overline{\text{CAS}}$  leading edge in an early write cycle and to  $\overline{\text{WE}}$  leading edge in a delayed write or a read-modify-write cycle.
  12.  $t_{RASC}$  defines  $\overline{\text{RAS}}$  pulse width in fast page mode cycles.
  13. Access time is determined by the longer of  $t_{AA}$  or  $t_{CAC}$  or  $t_{ACP}$ .
  14. An initial pause of 100  $\mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$  only refresh cycle or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles is required.
  15. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device.
  16. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  17. When both  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  go low at the same time, all 16-bits data are written into the device.  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  cannot be staggered within the same write/read cycles.
  18. All the  $V_{CC}$  and  $V_{SS}$  pins shall be supplied with the same voltages.
  19.  $t_{ASC}$ ,  $t_{CAH}$ ,  $t_{RCS}$ ,  $t_{RCH}$ ,  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{CSR}$  and  $t_{RPC}$  are determined by the earlier falling edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
  20.  $t_{CRP}$ ,  $t_{CHR}$ ,  $t_{ACP}$  and  $t_{CPW}$  are determined by the later rising edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
  21.  $t_{CWL}$  and  $t_{CHS}$  should be satisfied by both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
  22.  $t_{CPN}$  and  $t_{CP}$  are determined by the time that both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  are high.
  23. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{CC}/V_{SS}$  line noise, which causes to degrade  $V_{IH}(\text{min})/V_{IL}(\text{max})$  level.
  24.  $t_{CRP}$  is planned to be improved to match the standard DRAM specifications.
  25. If you use distributed CBR refresh mode with 15.6  $\mu\text{s}$  interval in normal read/write cycle, CBR refresh should be executed within 15.6  $\mu\text{s}$  immediately after exiting from and before entering into self refresh mode.
  26. IF you use  $\overline{\text{RAS}}$  only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6  $\mu\text{s}$  interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
  27. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

• Notes Concerning 2CAS Control

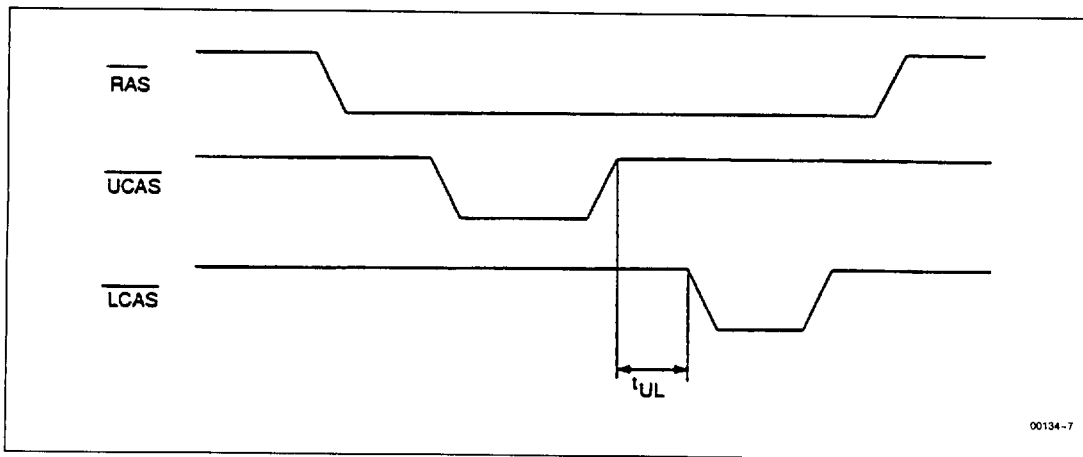
Please do not separate the UCAS/LCAS operation timing intentionally. However skew between UCAS/LCAS are allowed under the following conditions.

- (1) Each of the UCAS/LCAS should satisfy the timing specifications individually.
- (2) Different operation mode for upper/lower byte is not allowed; such as following.



2

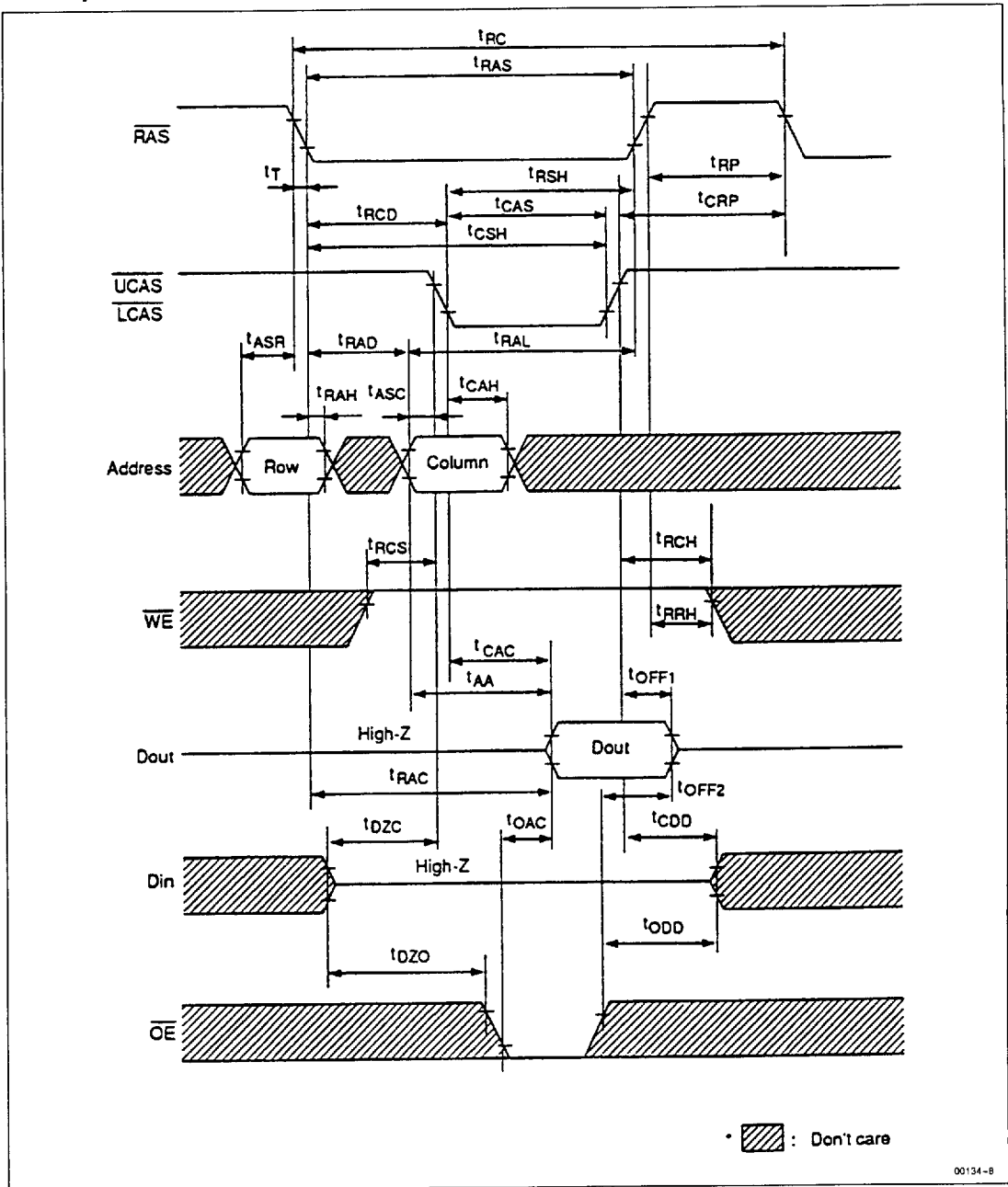
- (3) Closely separated upper/lower byte control is not allowed. However when the condition ( $t_{CP} \leq t_{UL}$ ) is satisfied, fast page mode can be performed.



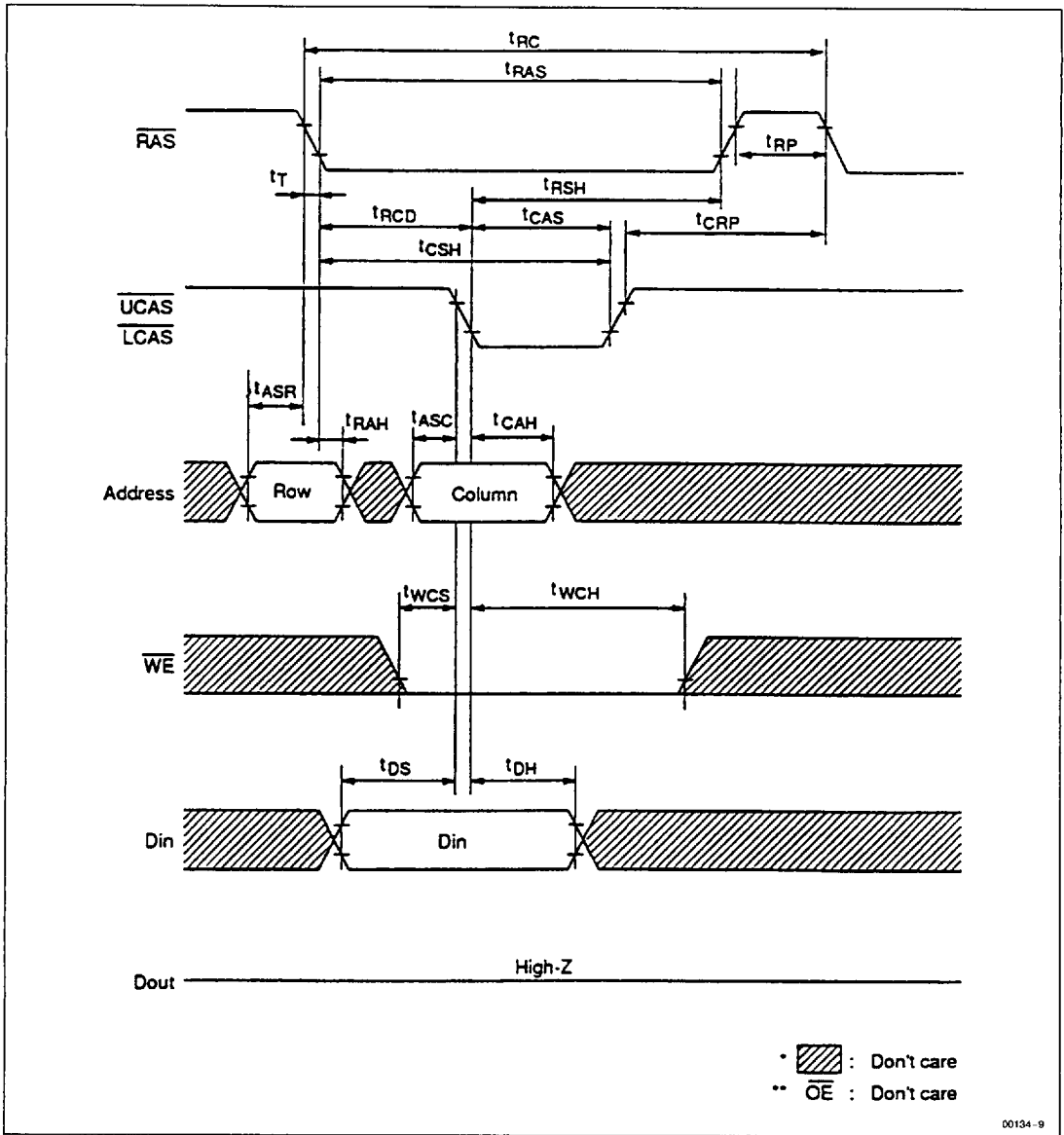
HM514260A/AL, HM51S4260A/AL Series

■ TIMING WAVEFORMS

• Read Cycle



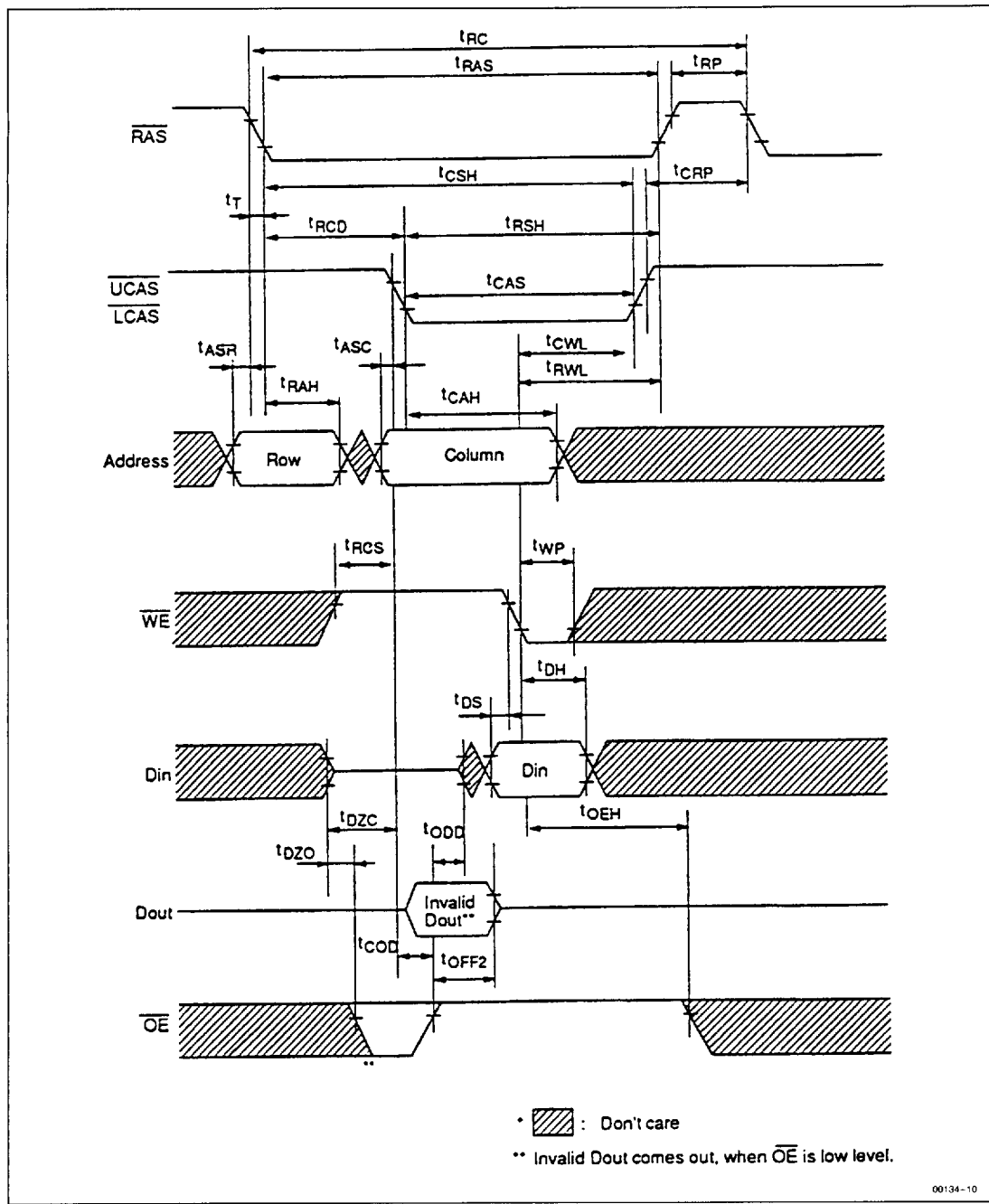
• Early Write Cycle



2

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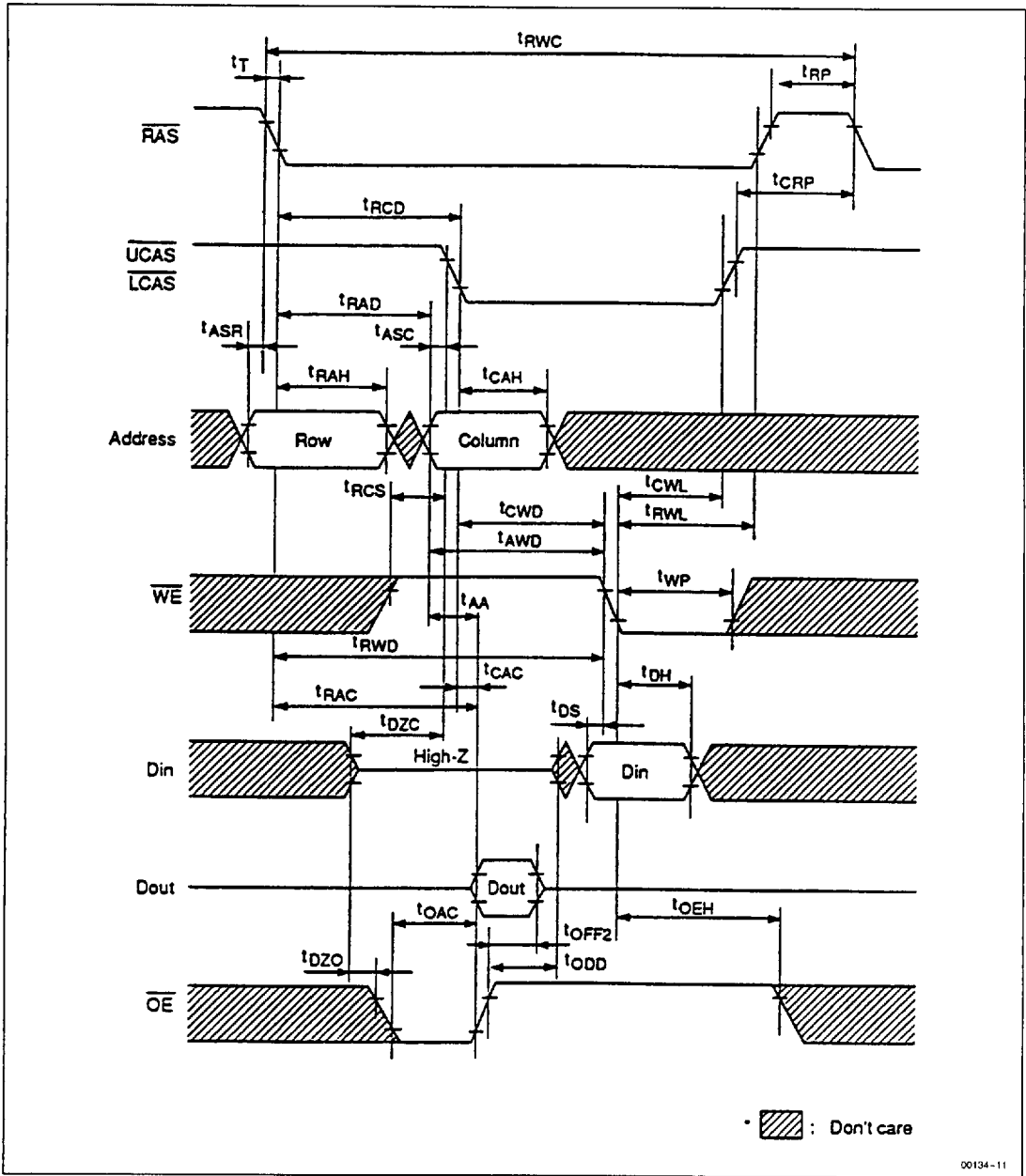
• Delayed Write Cycle



00134-10

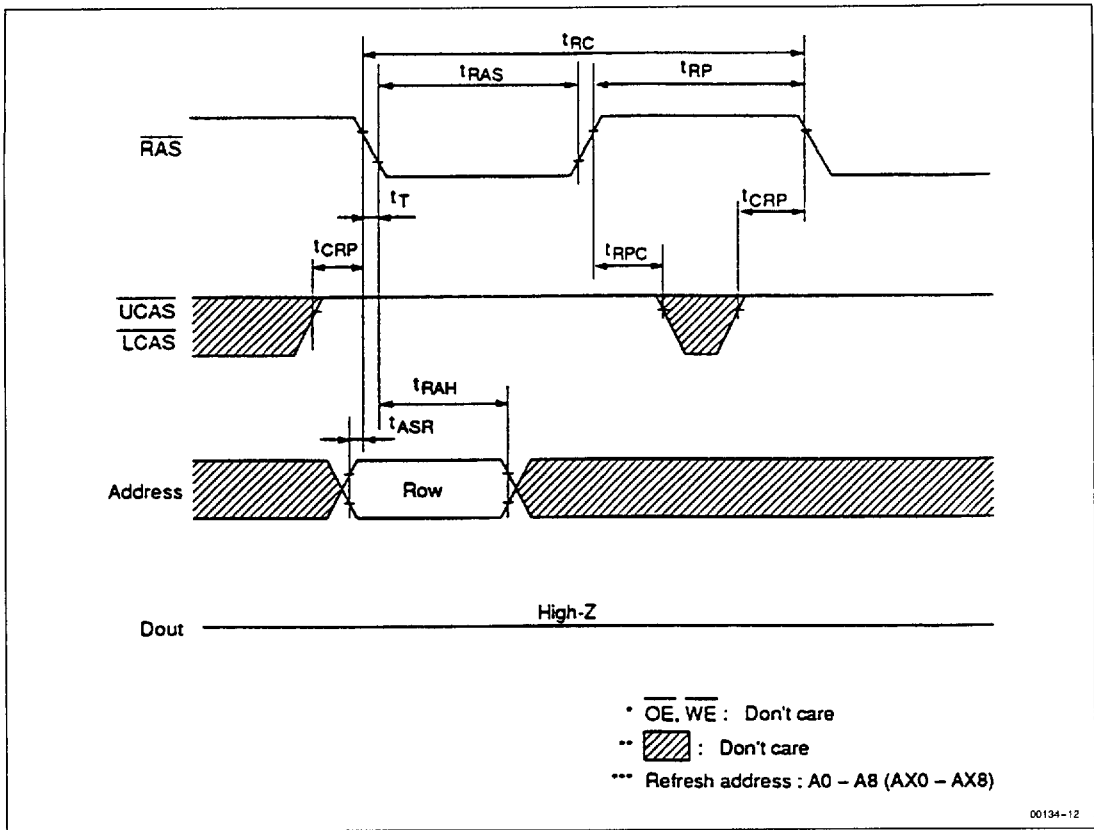
• Read-Modify-Write Cycle

2

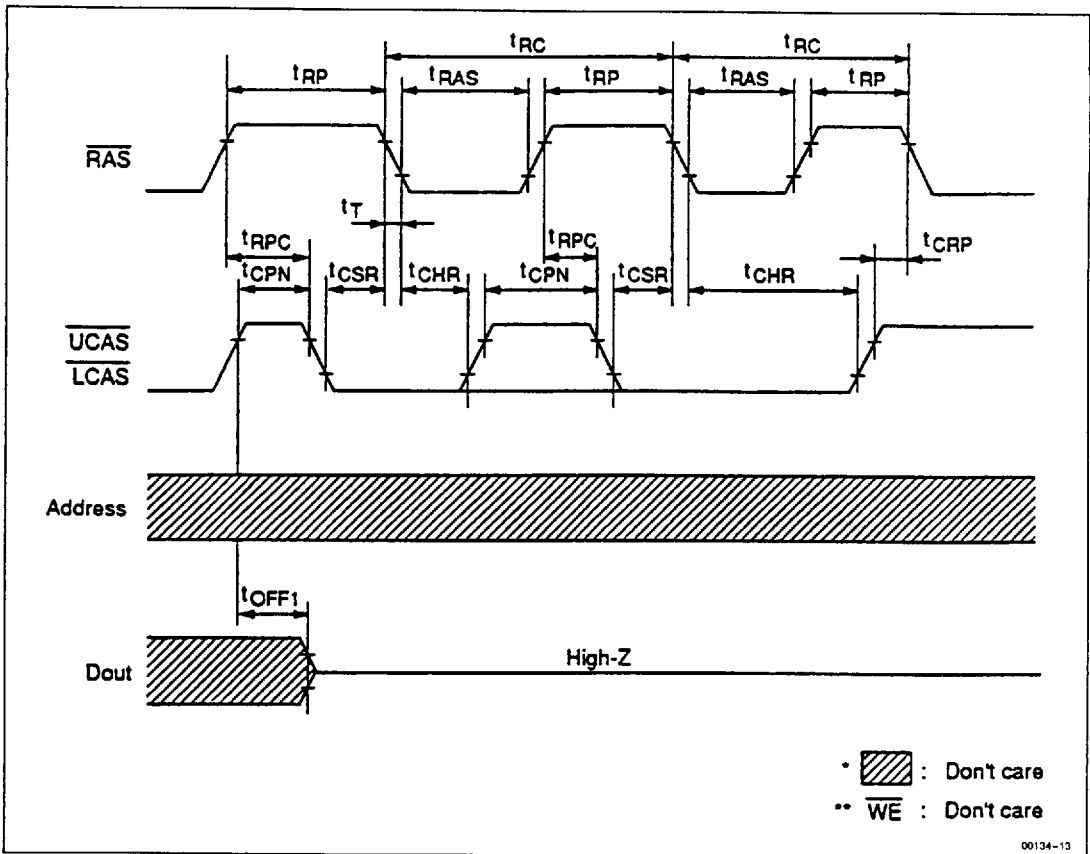


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• RAS Only Refresh Cycle



• CAS Before RAS Refresh Cycle

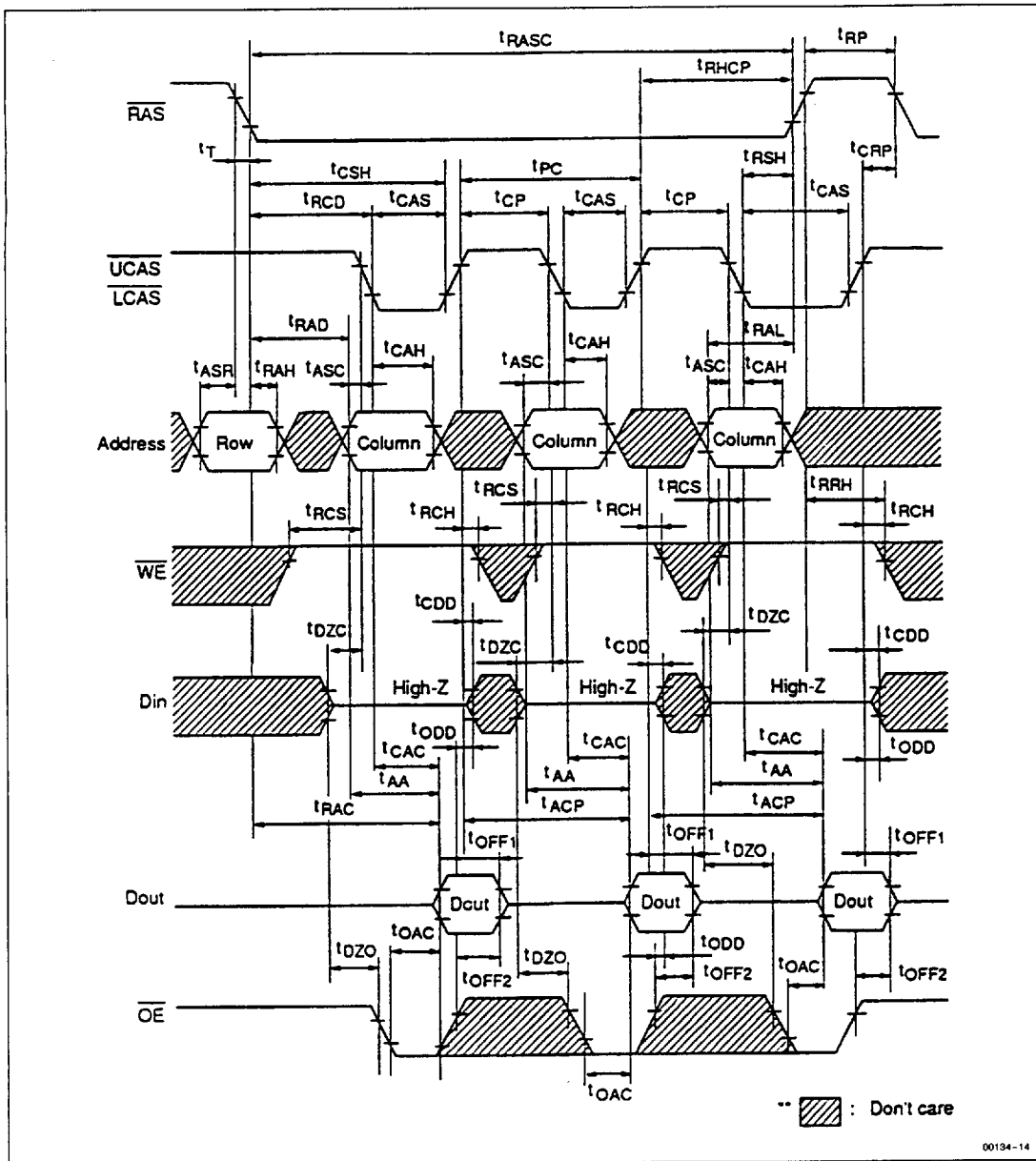


2

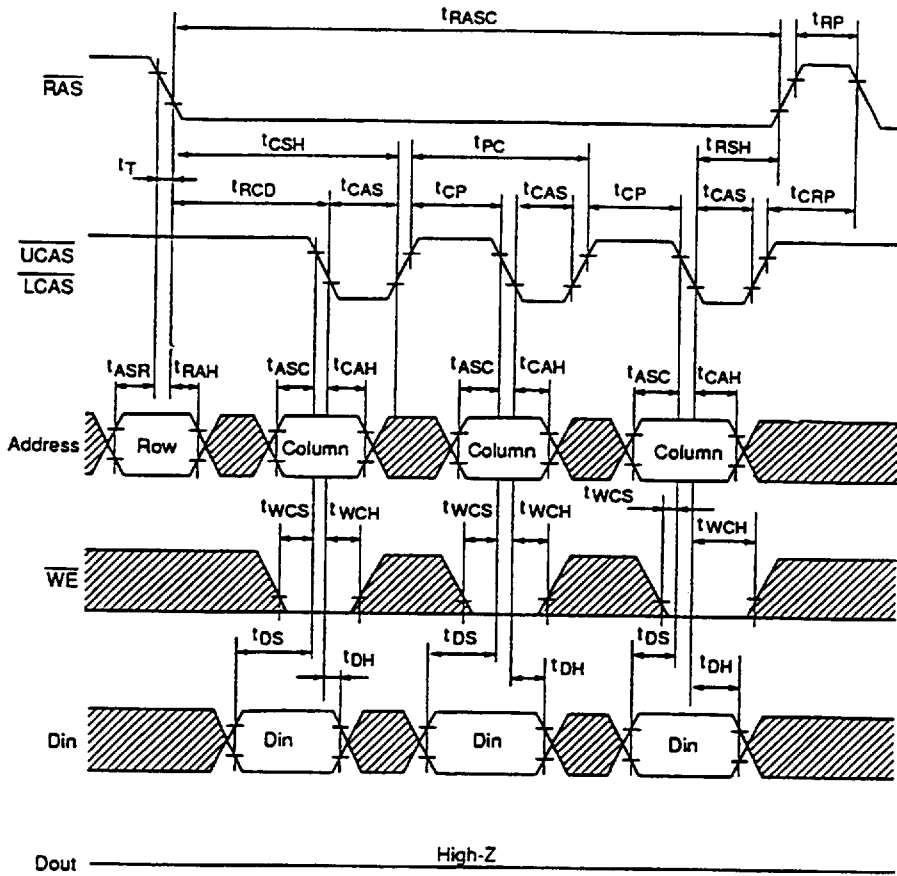


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• Fast Page Mode Read Cycle




• Fast Page Mode Early Write Cycle



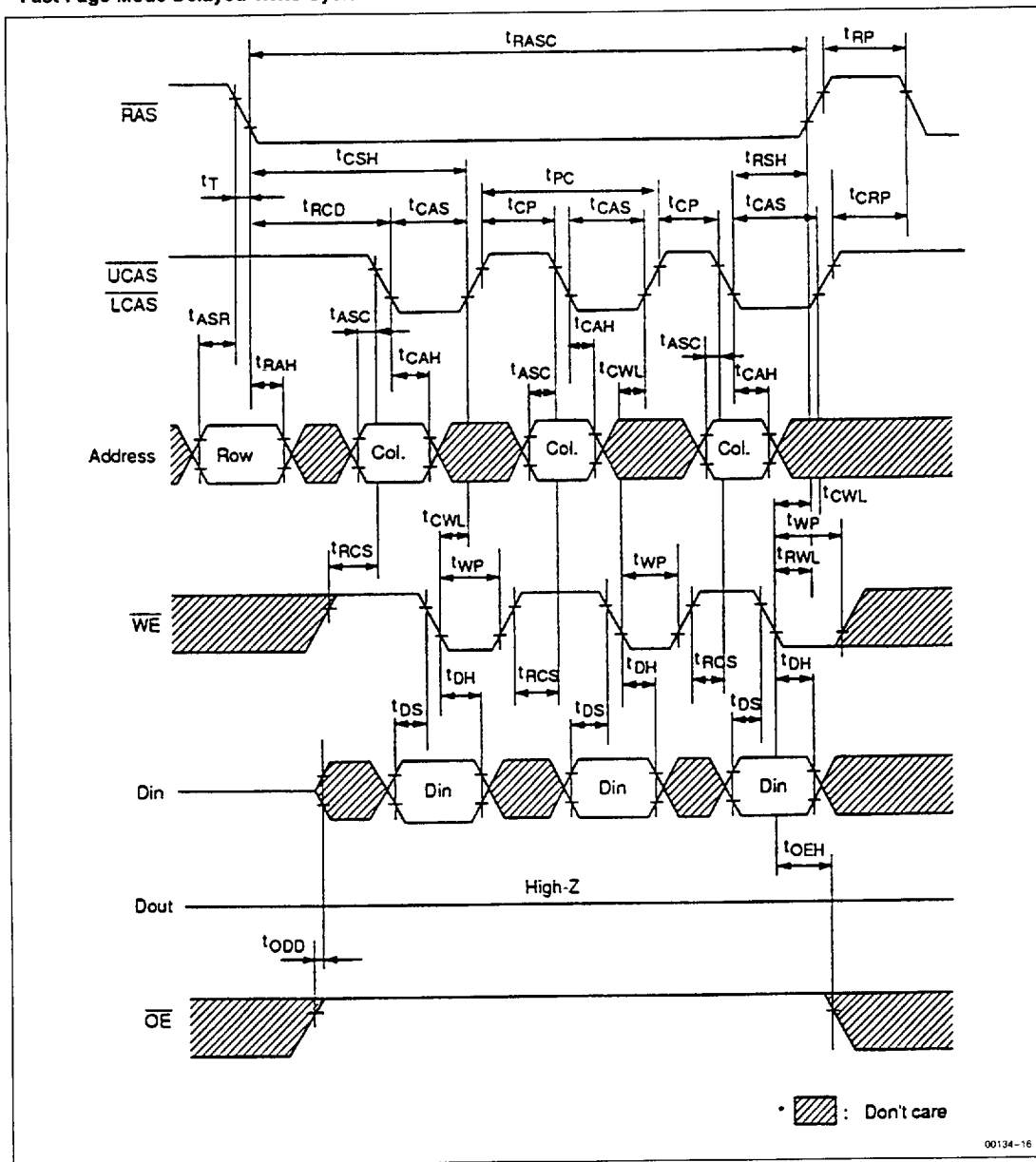
2

\*  $\overline{OE}$  : Don't care

\*\*  : Don't care

00134-15

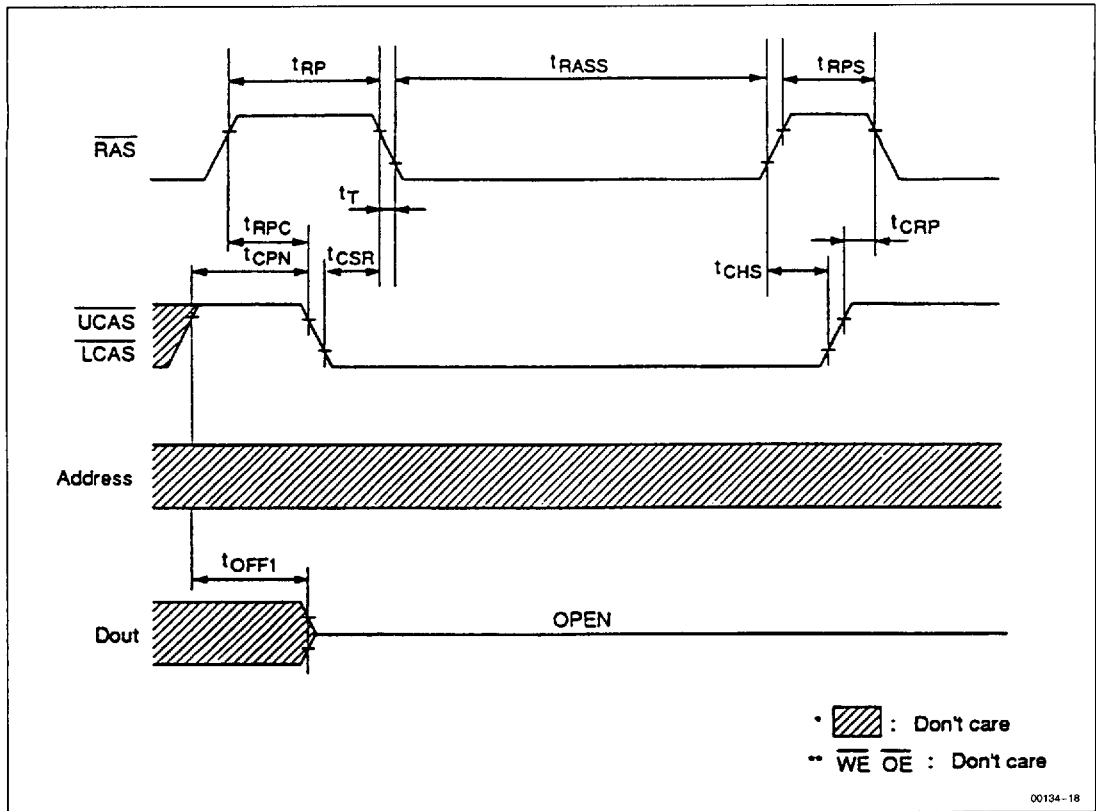
• Fast Page Mode Delayed Write Cycle





HM514260A/AL, HM51S4260A/AL Series

## • Self Refresh Cycle



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use  $t_{RASS}$  timing,  $10 \mu s \leq t_{RASS} \leq 100 \mu s$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{RASS} \geq 100 \mu s$ , then  $\overline{RAS}$  precharge time should use  $t_{RPS}$  instead of  $t_{RP}$ .
2. If you use  $\overline{RAS}$  only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with  $15.6 \mu s$  interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with  $15.6 \mu s$  interval in normal read/write cycle, CBR refresh should be executed within  $15.6 \mu s$  immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

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