HY51C4256

256K×4-Bit CMOS DRAM

M151201B-APR91

DESCRIPTION

The HY51C4256 is a high speed, low power 262,144×4 CMOS dynamic random access memory. Fabricated with HYUNDAI CMOS technology, HY51C4256 offers a fast page mode for high data bandwidth, fast usable speed, CMOS standby current and extended $\overline{RAS}$-only refresh for low standby power.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance.

Fast page mode operation allows random or sequencial access of all 512(×4)bits within a row simply by changing the column address. Because the column address access time is as fast as 50ns, a continuous data rate exceeding 20 MHz can be achieved.

The HY51C4256 offers high performance while relaxing many critical system timing requirements. These features make HY51C4256 ideally suited for graphics, digital signal processing, and high performance systems.

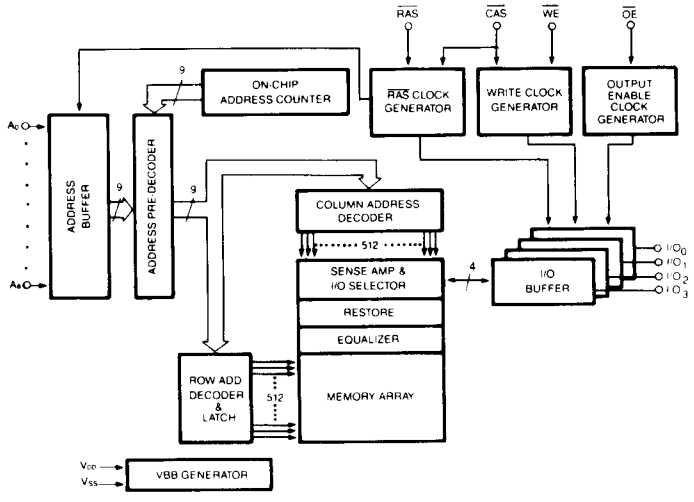
When $\overline{RAS}$ is $\geq V_{DD}-0.2V$, CMOS standby operation mode is active, and power drops to 1.5 mW (typically).

FEATURES

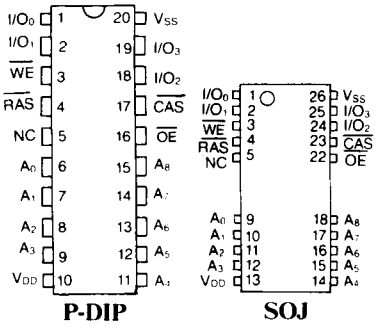
- **Low power dissipation**
  - **Operating current, 100ns : 75mA (max.)**
  - **TTL standby current : 2.5mA (max.)**
  - **CMOS standby current : 1.5mA (max.)**
- **Read-Modify-Write capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **Fast Page mode operation for a sustained data rate up to 20 MHz**
- **512 refresh cycles/8 ms**
- **High reliability 20 pin 300 mil P-DIP and 20/26 pin SOJ**
- **Fast access time and cycle time (ns)**

	HY51C4256-80	HY51C4256-10	HY51C4256-12
Max $\overline{RAS}$ Access Time, t_{RAC}	80	100	120
Max $\overline{CAS}$ Access Time, t_{CAC}	20	25	30
Min Fast Page Mode Cycle Time, t_{PC}	50	65	75
Min Cycle Time, t_{RC}	160	190	220

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_8	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature (Plastic)	−55 to 125	°C
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	1.0	W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" might cause permanent damage to the device.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY51C4256		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current (any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC} = t_{RC}$ (min.)	−80		95	mA	1,2
			−10		75		
			−12		70		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH}, other inputs ≥ V_{SS}			2.5	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC} = t_{RC}$ (min.)	−80		95	mA	2
			−10		75		
			−12		70		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−80		50	mA	1,2
			−10		40		
			−12		35		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD} - 0.2V$, $\overline{CAS}$ = V_{IH}, other inputs ≥ V_{SS}			1.5	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC} = t_{RC}$ (min)	−80		95	mA	2
			−10		75		
			−12		70		
V_{IL}	Input Low Voltage (all inputs)			−0.5	0.8	V	3
V_{IH}	Input High Voltage (all inputs)			2.4	V_{DD}+1	V	3
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH} = −5mA		2.4		V	

NOTES:
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in fast page mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} may undershoot to −1.0V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY51C4256						UNIT	NOTE
			80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	80	85K	100	85K	120	85K	ns	
2	t_{RC}	Random Read or Write Cycle Time	160		190		220		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	70		80		90		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	80		100		120		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	30		35		40		ns	
6	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	50	25	65	30	80	ns	2
7	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
8	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
9	t_{RAH}	Row Address Hold Time	15		15		20		ns	
10	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
11	t_{CAH}	Column Address Hold Time	15		20		25		ns	
12	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time in Read Cycle	30		35		40		ns	
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15		15		20		ns	
14	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		ns	7
15	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		ns	7
16	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	0		0		0		ns	
17	t_{OAC}	Access Time from $\overline{OE}$		20		25		30	ns	
18	t_{CAC}	Access Time from $\overline{CAS}$		30		35		40	ns	12
19	t_{RAC}	Access Time from $\overline{RAS}$		80		100		120	ns	3,4,5
20	t_{CAA}	Access Time from Column Address		40		45		55	ns	5,6,12
21	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low Impedance	0		0		0		ns	14,15
22	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High Impedance	0	20	0	25	0	30	ns	11,14,15
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	60		70		80		ns	
24	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	55	25	65	ns	1
25	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time in Write Cycle	30		35		40		ns	
26	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		35		40		ns	
27	t_{WCS}	Write Command Set-up Time	0		0		0		ns	8,9
28	t_{WCH}	Write Command Hold Time	15		20		25		ns	
29	t_{WP}	Write Command Pulse Width	15		20		25		ns	
30	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	60		70		80		ns	
31	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		35		40		ns	
32	t_{DS}	Data-In Set-up Time	0		0		0		ns	10
33	t_{DH}	Data-In Hold Time	15		20		25		ns	10
34	t_{WOH}	Write to $\overline{OE}$ Hold Time	20		25		30		ns	
35	t_{OED}	$\overline{OE}$ to Data Delay	20		25		30		ns	
36	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	220		265		305		ns	

#	SYMBOL	PARAMETER	HY51C4256						UNIT	NOTE
			80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
37	t_{RRW}	$\overline{RAS}$ Pulse Width (RMW)	140		175		205		ns	
38	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	60		70		80		ns	8
39	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	110		135		160		ns	8
40	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	90		110		125		ns	
41	t_{AWD}	Column Address to $\overline{WE}$ Delay	70		80		85		ns	8
42	t_{PCM}	Fast page mode Read-Modify-Write Cycle	50		65		75		ns	
43	t_{CP}	$\overline{CAS}$ Precharge Time	10		20		25		ns	
44	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	40		45		55		ns	
45	t_{CAP}	Access Time from Column Precharge		45		60		70	ns	12
46	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	60		70		80		ns	
47	t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10		10		10		ns	
48	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
49	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	20		30		40		ns	
50	t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	13
51	t_{RI}	Refresh Interval (512 Cycle)		8		8		8	ms	16

NOTES:

1. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then the access time is controlled by t_{CAA} and t_{CAC}.
2. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limit insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.) then the access time is controlled by t_{CAA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
4. Assume $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assume $t_{RAD} \geq t_{RAD}$ (max.).
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
8. t_{WCS}, t_{RWD}, t_{AWD}, t_{CWD} are not restrictive operating parameters.
9. t_{WCS} (min.) must be satisfied in the early write cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$.
11. t_{HZ} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
12. Access time is determined by the longer of t_{CAA}, t_{CAC}, or t_{CAP}.
13. t_T is measured between V_{IH} (min.) and V_{IL} (max.) AC Measurements assume $t_T = 5$ ns.
14. Assume tri-state test load (5 pF and a 380 Ohm Thevenin equivalent)
15. At any given temperature and voltage combination, coincident deselection/selection is permissible for wired-OR devices.
16. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycle (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only Refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

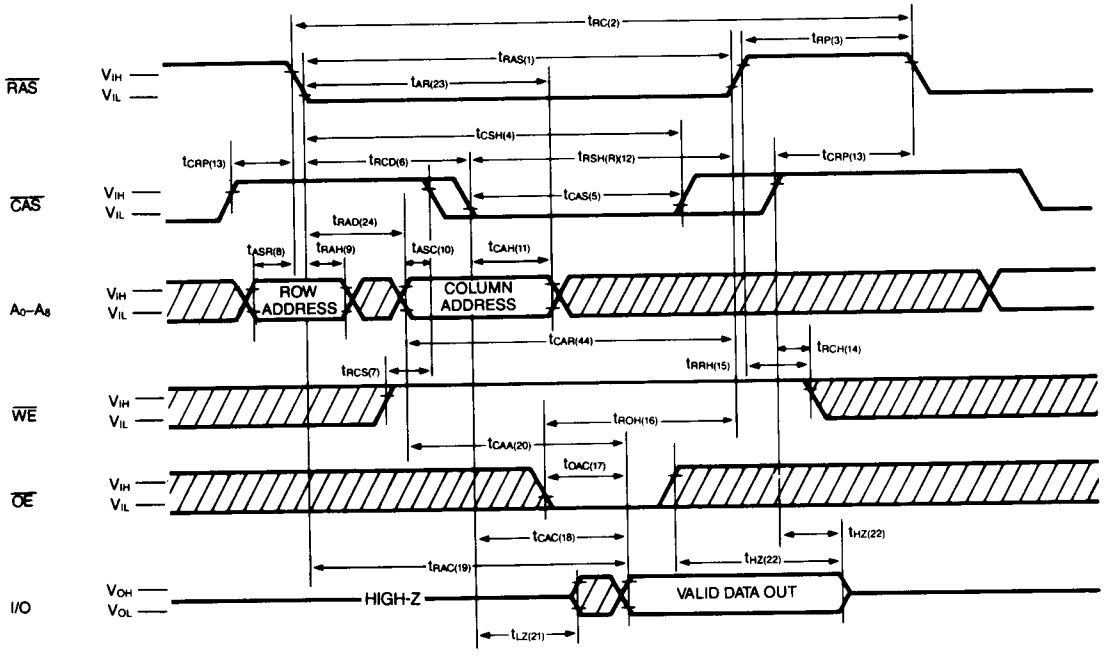
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data Input	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	8	pF
C_{OUT}	Data Output	—	8	pF

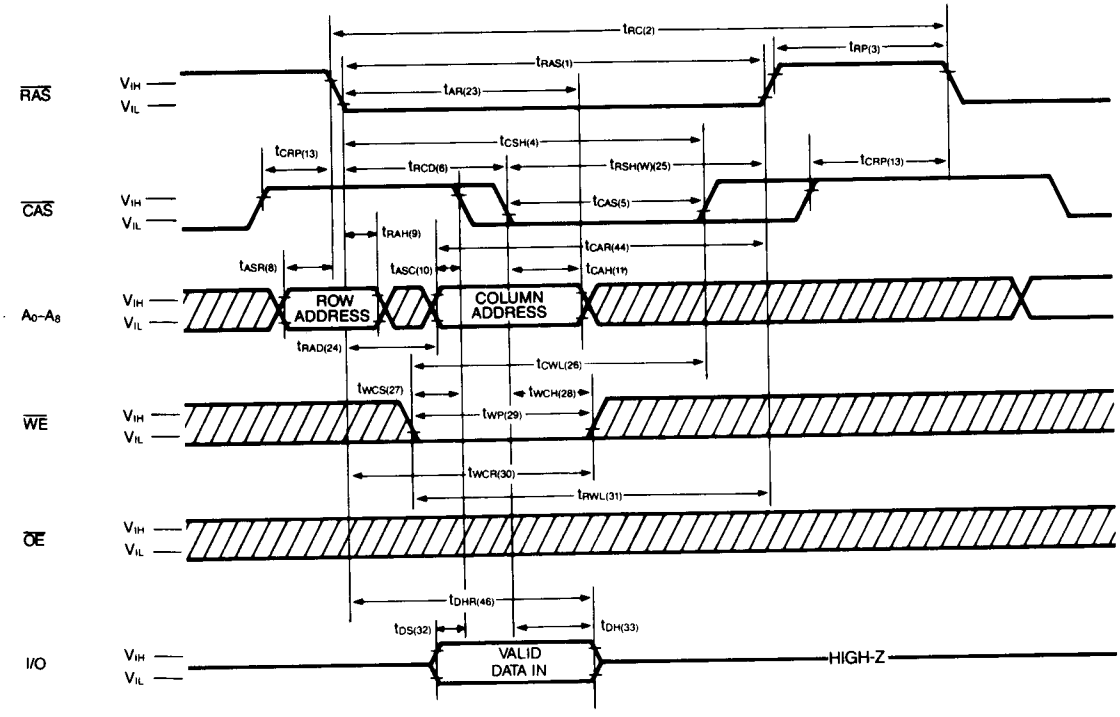
NOTE: Capacitance is measured at the worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAMS

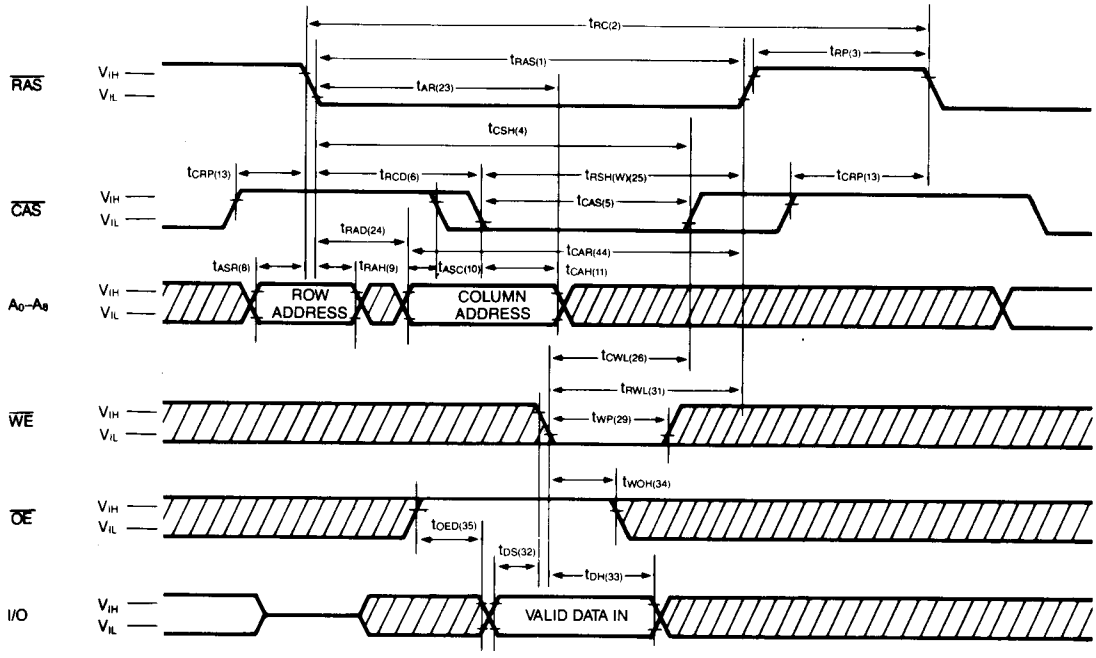
READ CYCLE



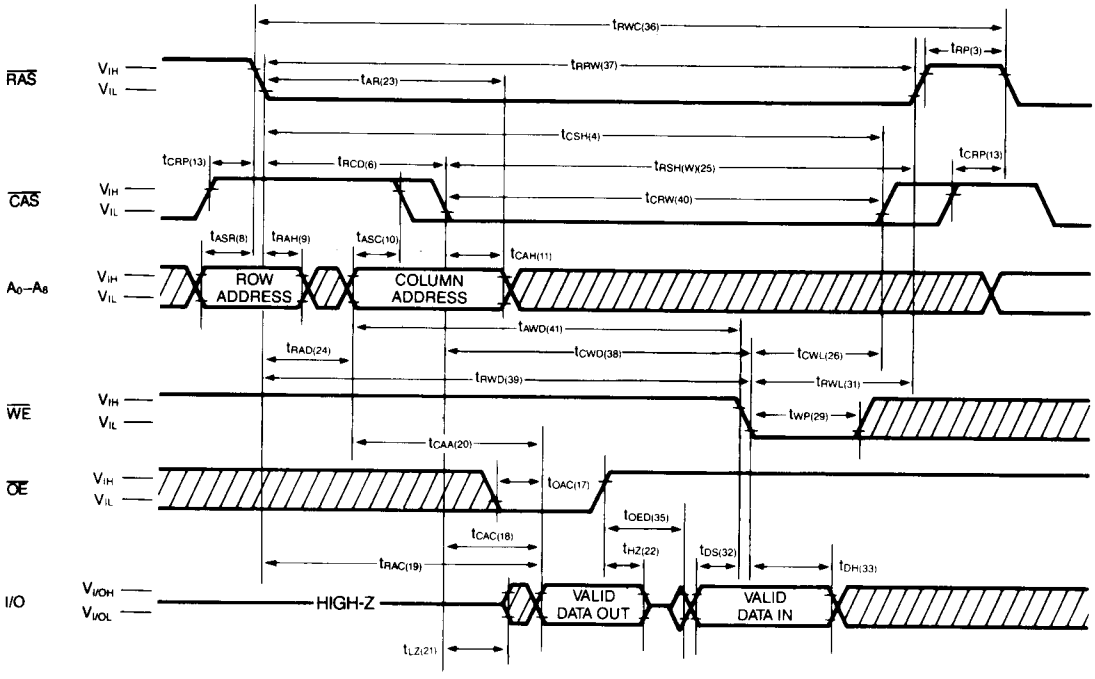
EARLY WRITE CYCLE



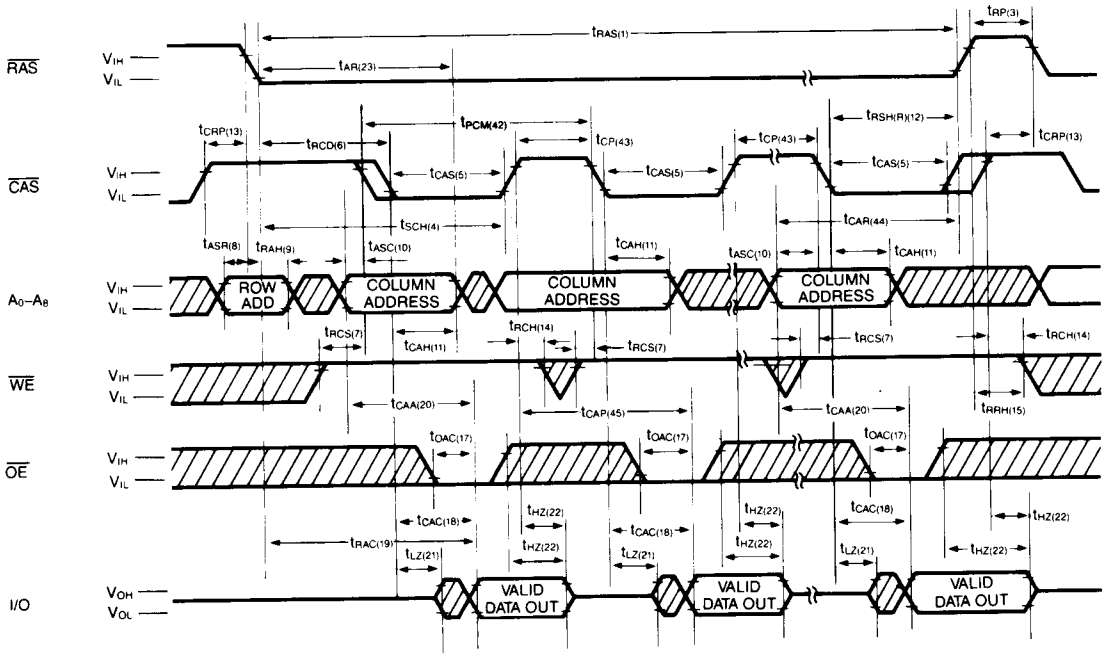
WRITE CYCLE ($\overline{OE}$ CONTROLLED)



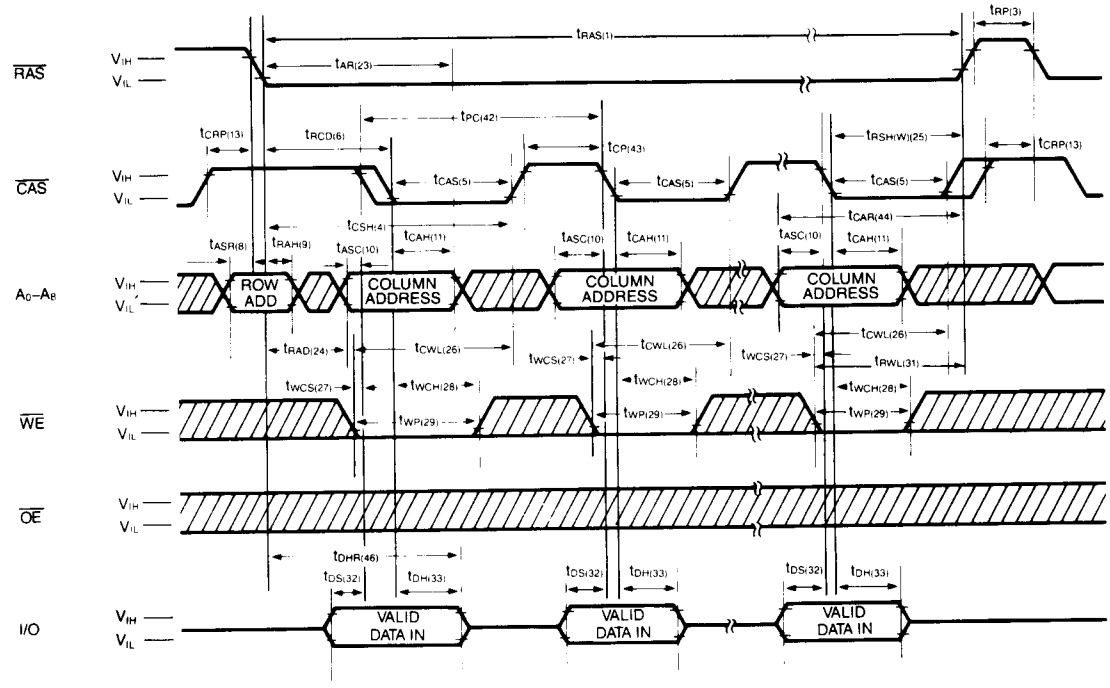
READ-MODIFY-WRITE CYCLE



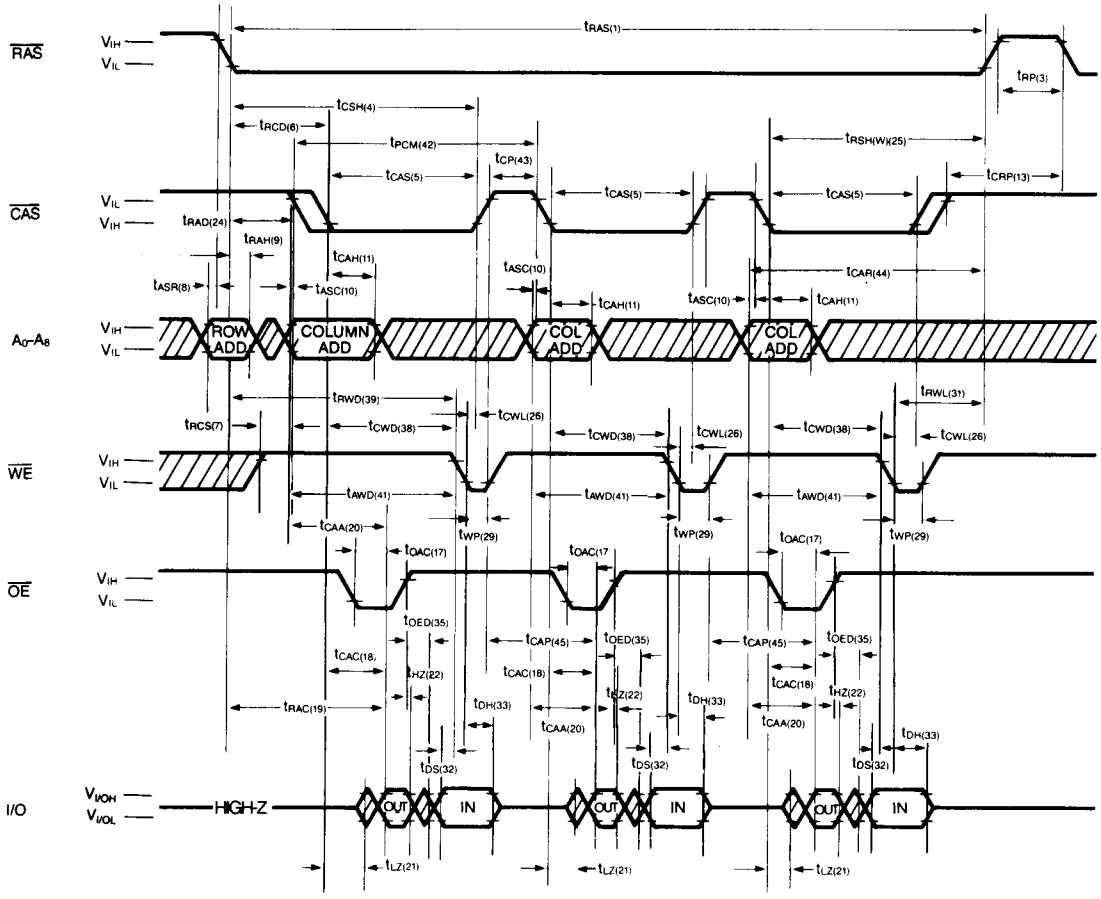
FAST PAGE MODE READ CYCLE



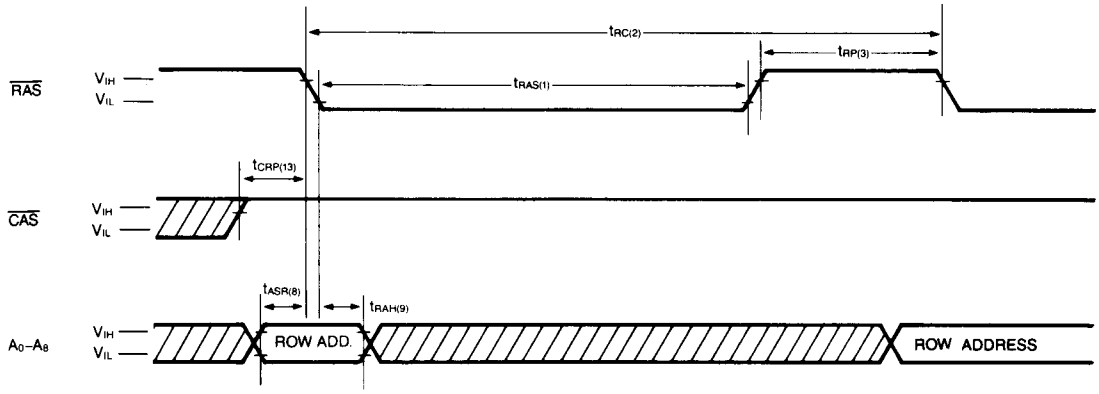
FAST PAGE MODE EARLY WRITE CYCLE



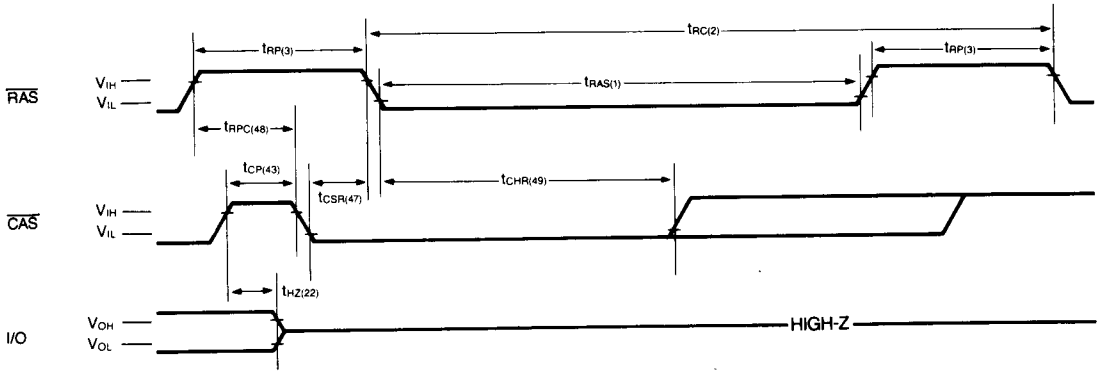
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE

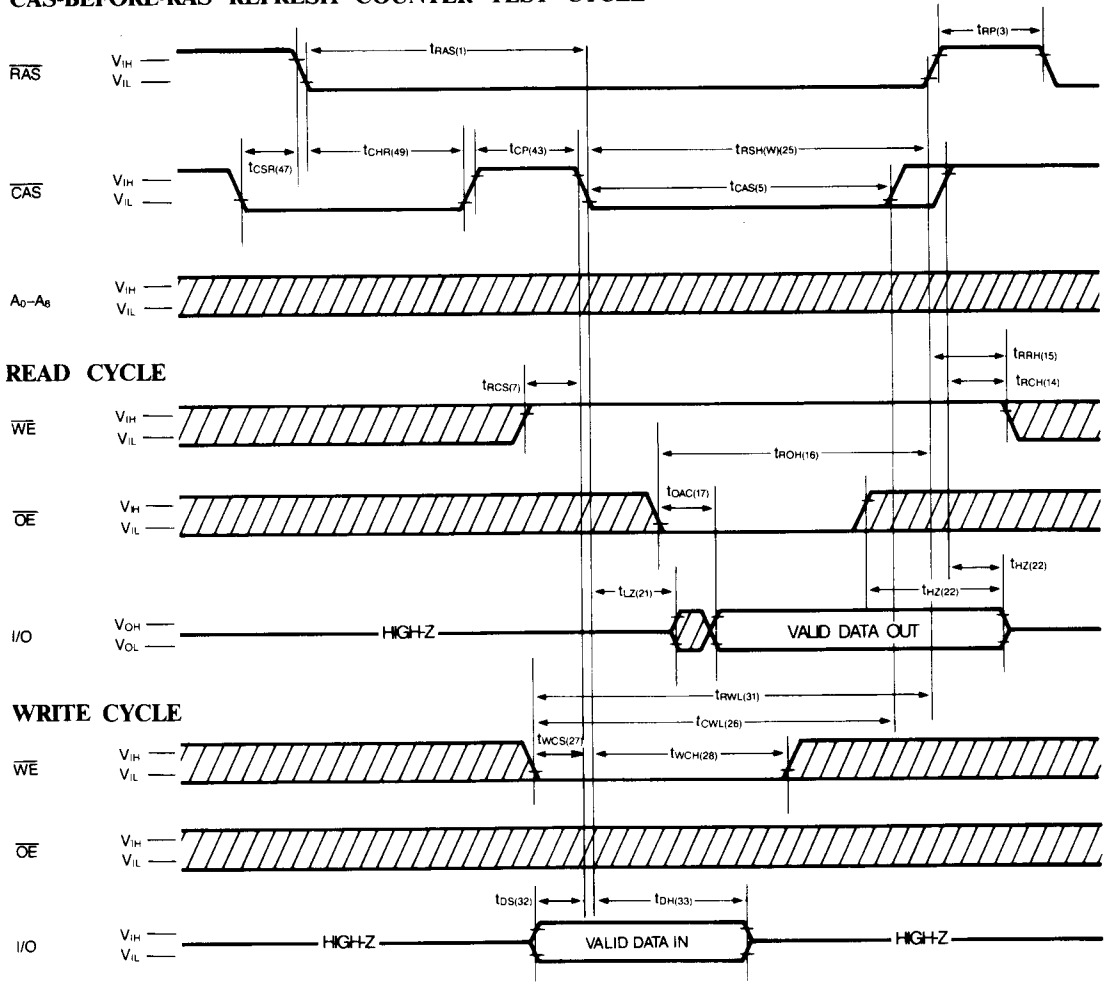


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

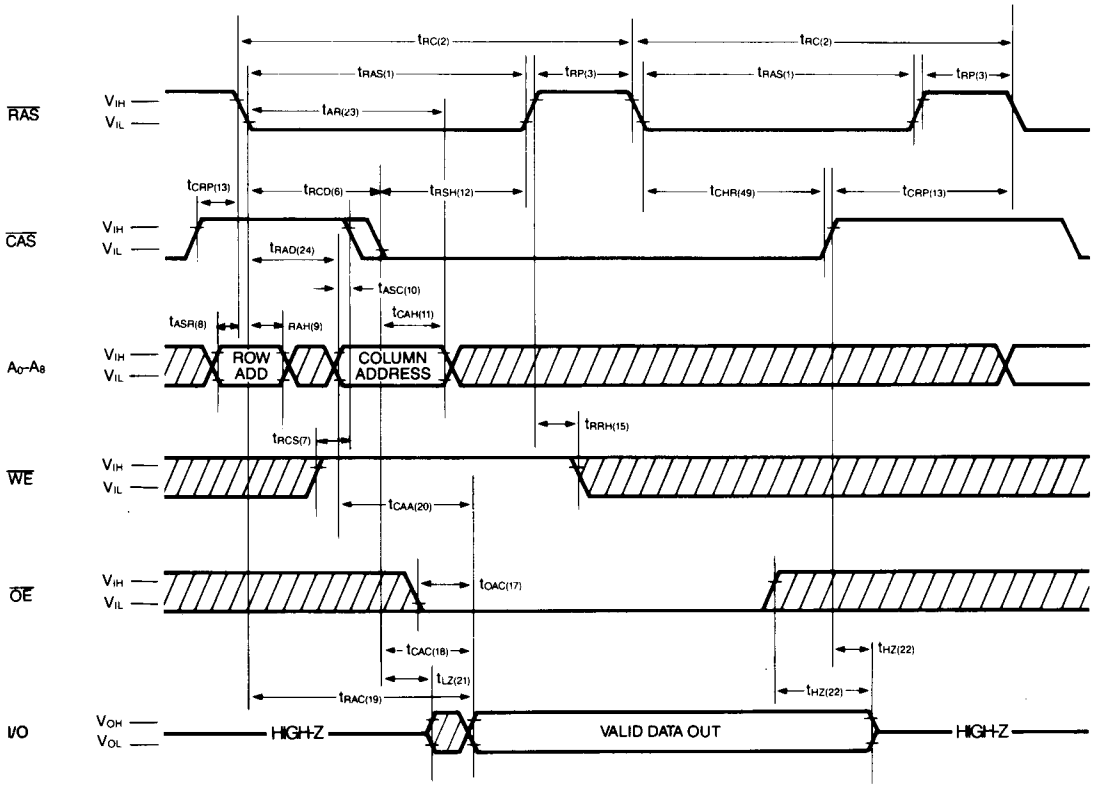


Note: $\overline{WE}$, $\overline{OE}$, A_0-A_8 = Don't care

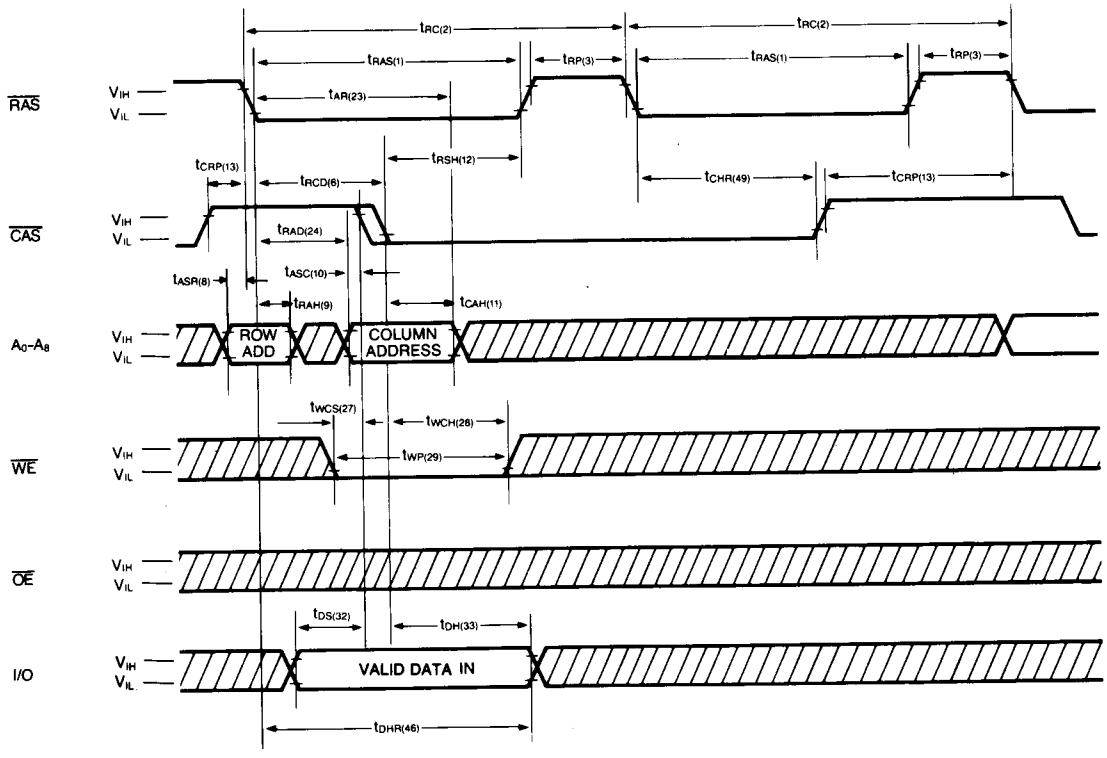
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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FUNCTIONAL DESCRIPTION

The HY51C4256 is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY51C4256 reads and writes 4 bits of data at a time by multiplexing a 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched by the Row Address Strobe($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, and t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out is controlled by the Out Enable($\overline{OE}$) and $\overline{CAS}$(See the write cycle description).

Data out becomes valid only when t_{RAC}, t_{CAA}, t_{OAC} and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{OAC} and t_{CAC} are all satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation.

The column address is latched by $\overline{CAS}$, The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Consequently, the write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. In a $\overline{CAS}$ controlled write cycle(the leading edge or $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ going high will maintain the I/O in the high impedance state, terminating with $\overline{WE}$ going high allows the output to go active, and $\overline{OE}$ must be brought high to allow for inputs on the I/O.

The HY51C4256 incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write function has been initiated, the HY51C4256 internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycle are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycles such as read, write, read-modify-write, or $\overline{RAS}$-Only refresh cycle will perform refresh.
2. $\overline{CAS}$-Before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters $\overline{CAS}$-Before-$\overline{RAS}$ refresh cycle. The HY51C4256 will use an internal nine bits counter output as the source of the row address and will ignore the external address inputs.

This $\overline{CAS}$-Before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is allowed. Also, the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does

not cause device selection and the state of the Data Output pin will remain in a high impedence state.

In order to guarantee the reliable operation of $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, an internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively (512 write cycles) and, then verify the data which have been written by 512 consecutive read cycle.

DATA RETENTION MODE

The HY51C4256 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY51C4256 power consumption is reduced to the low I_{DDS} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DDS})}{t_{RX}}$$

Where t_{RC}=Refersh Cycle Time
t_{RX}=Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a row. Following the entry cycle into fast page mode access time is t_{CAA} or t_{CAP} dependent. If the column adderess is valid prior to or coincident with the rising edge of $\overline{CAS}$, then the access time is determined by the rising edge of $\overline{CAS}$ specified by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{CAA}. For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustanined data rate over 20 MHz for applications that require high data rate such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate}=\frac{512}{t_{RC}+511\times t_{PC}}$$

DATA OUT OPERATION

The HY51C4256 input/output(I/O) is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables data to transfer into and from a selected row address. A $\overline{RAS}$ high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or a $\overline{CAS}$ low level enables the internal I/O data path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O data path and disables the output driver if the driver was enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path, nor on the output driver.

An $\overline{OE}$ low transiton or an $\overline{OE}$ low level enables the output driver when the I/O data path is enabled. An $\overline{OE}$ high transition or an $\overline{OE}$ high level disables the output driver, but does not disable the data latch when it has been enabled. A $\overline{WE}$ low level disables the output driver when a $\overline{CAS}$ low level occurs. If the $\overline{WE}$ low transition occurs after the $\overline{CAS}$ low transition such that the output driver is enable prior to the $\overline{WE}$ low transition, it is necessary to use $\overline{OE}$ to disable the output driver prior to the $\overline{WE}$ low transition to allow data in set-up time(t_{DS}). A $\overline{WE}$ high transition passes control of the output drive to $\overline{OE}$.

POWER ON

An initial pause of 200 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

The V_{DD} current (I_{DD}) requirement of the HY 51C4256 during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}=V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION