

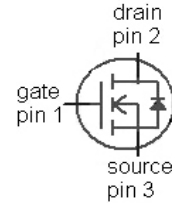
OptiMOS[®] 2 Power-Transistor


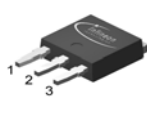
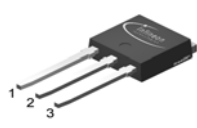
Features

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC¹⁾ for target applications
- N-channel, logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- 175 °C operating temperature

Product Summary

V_{DS}	25	V
$R_{DS(on),max}$	12.8	m Ω
I_D	30	A



Type	IPD13N03LA	IPF13N03LA	IPS13N03LA	IPU13N03LA
				
Package	P-TO252-3-11	P-TO252-3-23	P-TO251-3-11	P-TO251-3-21
Ordering Code	Q67042-S4159	Q67042-S4195	Q67042-S4248	Q67042-S4160
Marking	13N03LA	13N03LA	13N03LA	13N03LA

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}^{2)}$	30	A
		$T_C=100\text{ °C}$	30	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}^{3)}$	210	
Avalanche energy, single pulse	E_{AS}	$I_D=24\text{ A}$, $R_{GS}=25\ \Omega$	60	mJ
Reverse diode dv/dt	dv/dt	$I_D=30\text{ A}$, $V_{DS}=20\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=175\text{ °C}$	6	kV/ μs
Gate source voltage ⁴⁾	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	46	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	3.2	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	75	
		6 cm ² cooling area ⁵⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=20\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	0.1	1	μA
		$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=20\text{ A}$	-	17.5	21.9	m Ω
		$V_{GS}=10\text{ V}, I_D=30\text{ A}$	-	10.7	12.8	
Gate resistance	R_G		-	0.9	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=30\text{ A}$	18	36	-	S

¹⁾ J-STD20 and JESD22

²⁾ Current is limited by bondwire; with an $R_{thJC}=3.2\text{ K/W}$ the chip is able to carry 47 A.

³⁾ See figure 3

⁴⁾ $T_{j,max}=150\text{ }^\circ\text{C}$ and duty cycle $D<0.25$ for $V_{GS}<-5\text{ V}$

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	784	1043	pF
Output capacitance	C_{oss}		-	303	402	
Reverse transfer capacitance	C_{rss}		-	41	62	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=15\text{ A}, R_G=2.7\ \Omega$	-	5.4	8.0	ns
Rise time	t_r		-	4.6	6.9	
Turn-off delay time	$t_{d(off)}$		-	15	23	
Fall time	t_f		-	2.6	3.9	

Gate Charge Characteristics⁶⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=15\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	2.7	3.6	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.3	1.7	
Gate to drain charge	Q_{gd}		-	1.8	2.7	
Switching charge	Q_{sw}		-	3.3	4.7	
Gate charge total	Q_g		-	6.3	8.3	
Gate plateau voltage	$V_{plateau}$		-	3.4	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$	-	5.5	7.3	nC
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	6.6	8.7	

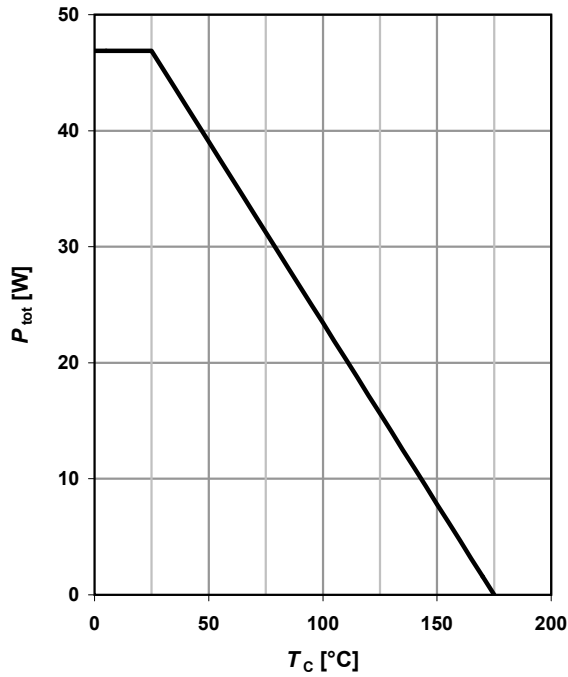
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	30	A
Diode pulse current	$I_{S,pulse}$		-	-	210	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=30\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.95	1.2	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

⁶⁾ See figure 16 for gate charge parameter definition

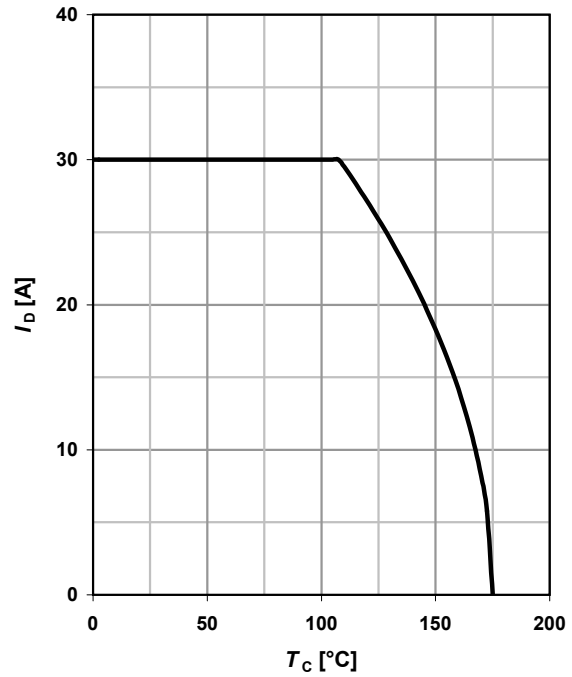
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

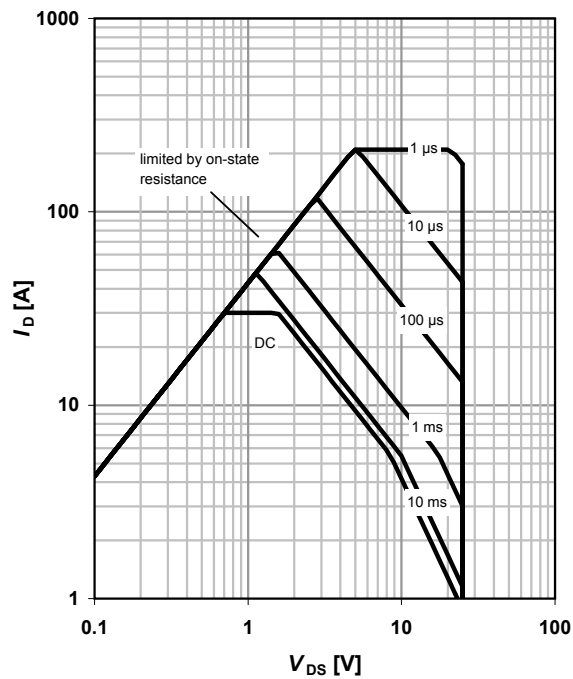
$$I_D = f(T_C); V_{\text{GS}} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

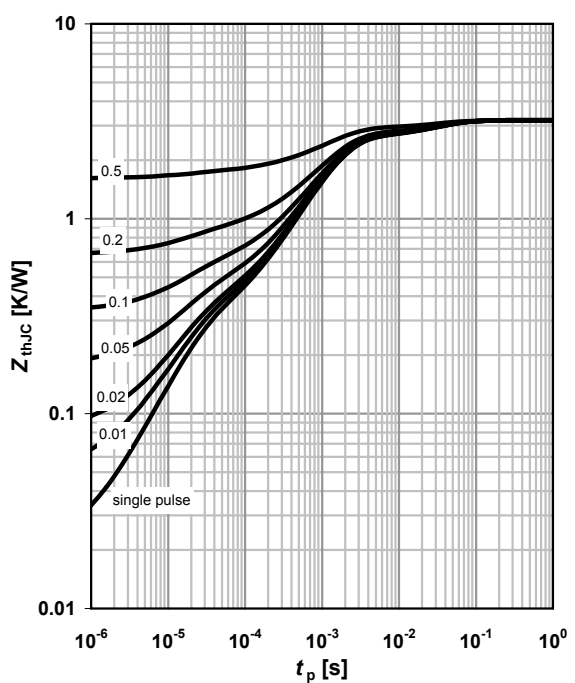
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

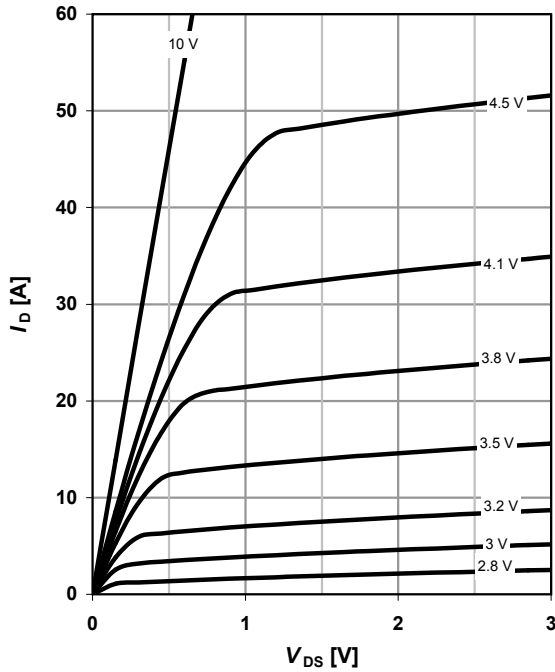
parameter: $D = t_p / T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

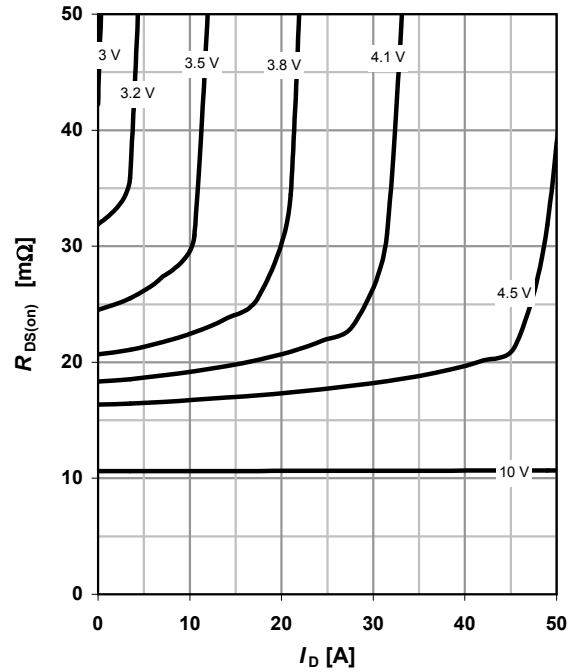
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

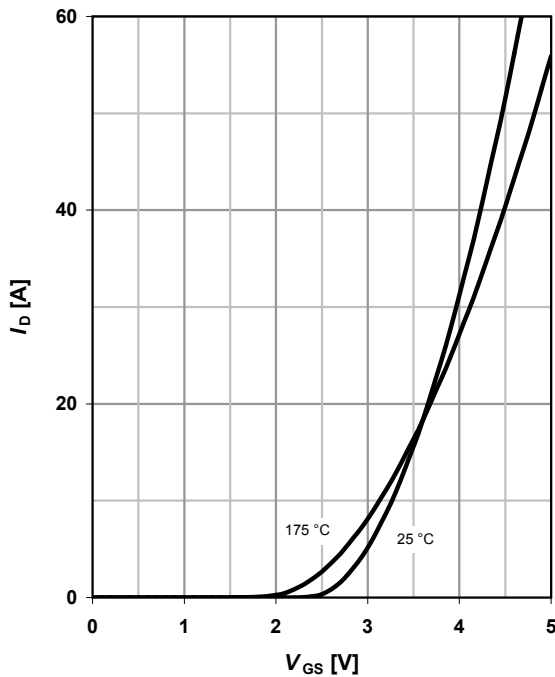
parameter: V_{GS}



7 Typ. transfer characteristics

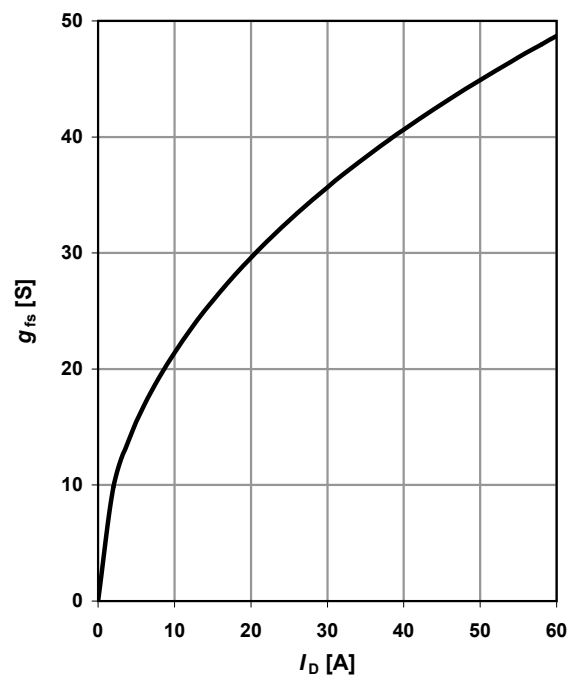
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



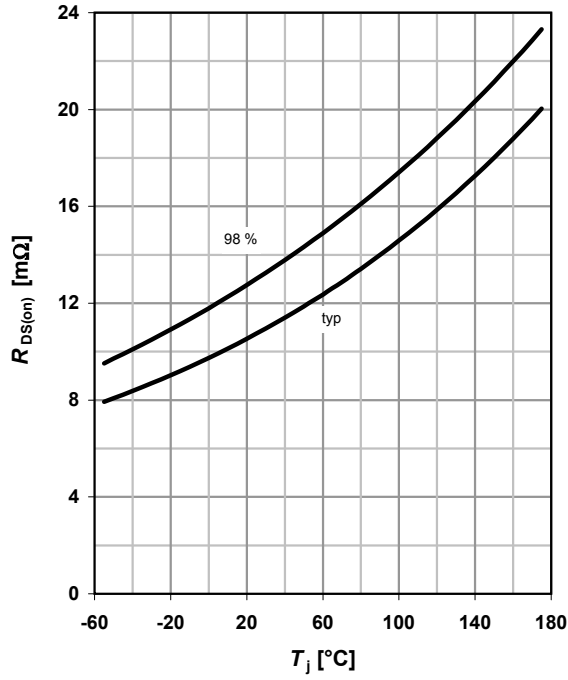
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



9 Drain-source on-state resistance

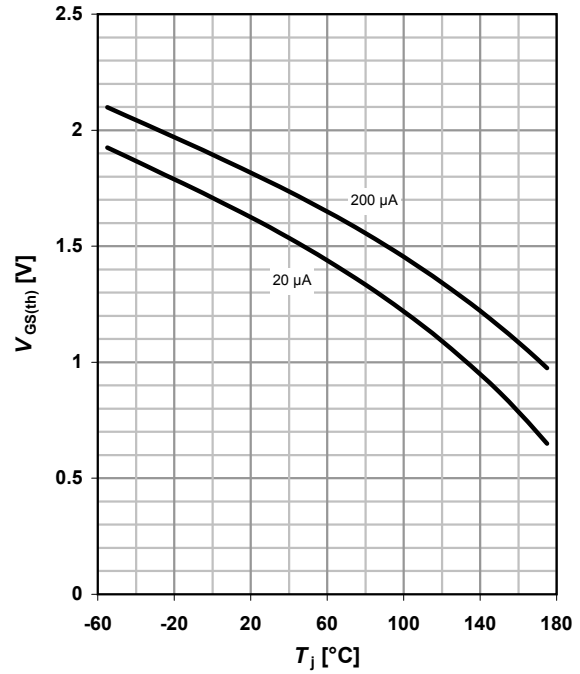
$$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

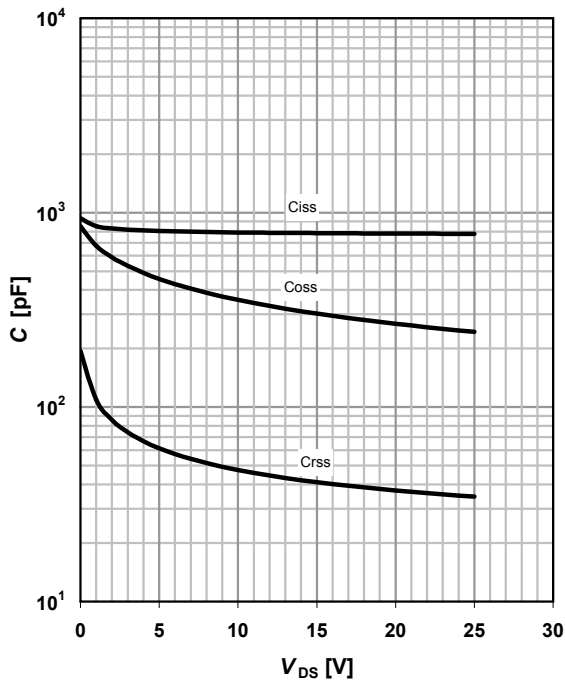
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. Capacitances

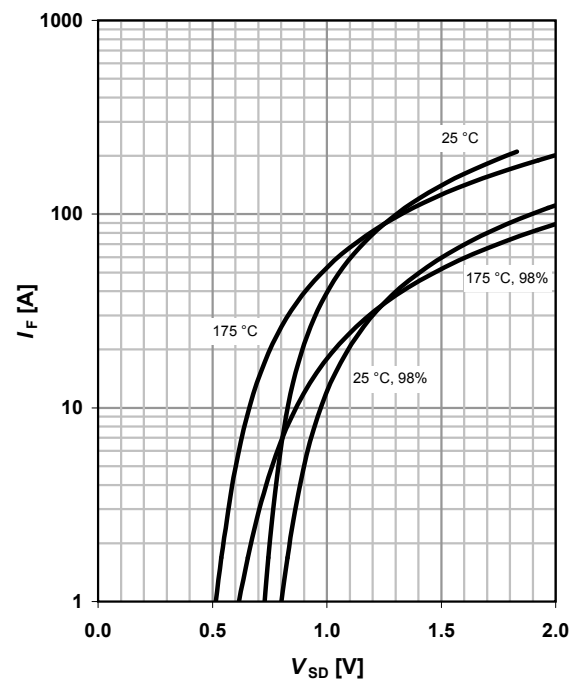
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

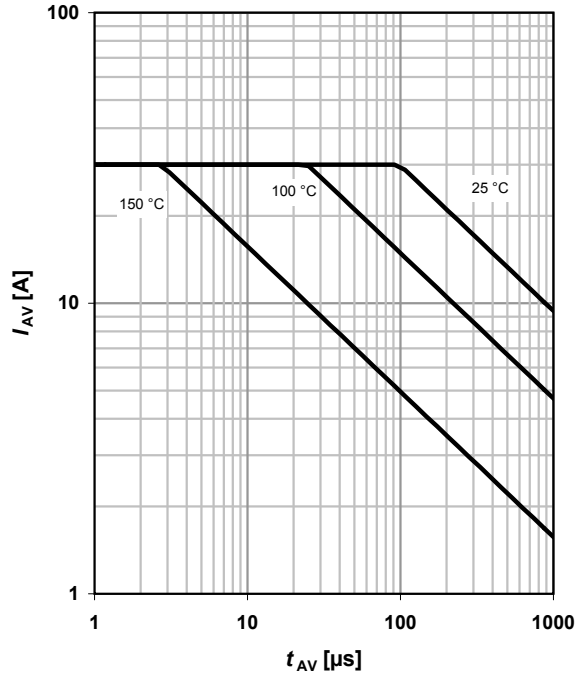
parameter: T_j



13 Avalanche characteristics

$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

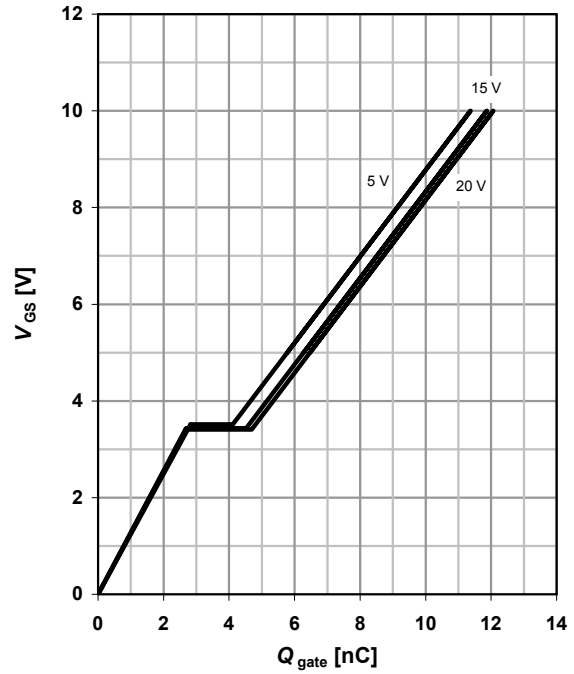
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

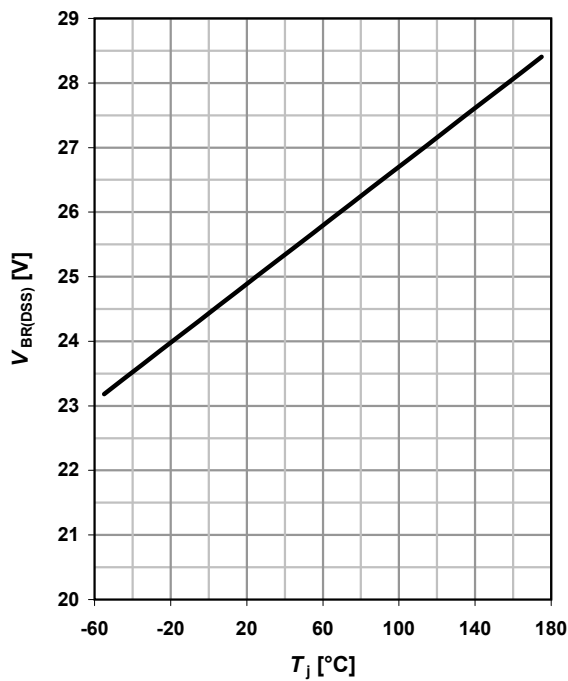
$$V_{GS} = f(Q_{\text{gate}}); I_D = 25 \text{ A pulsed}$$

parameter: V_{DD}



15 Drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

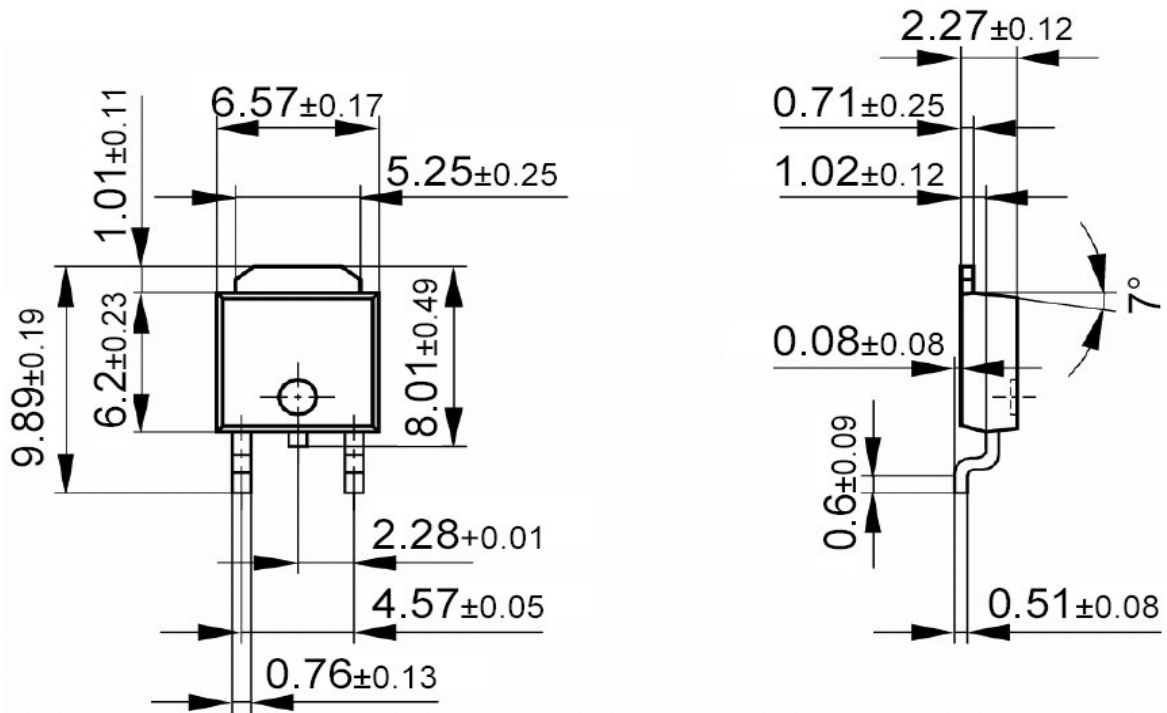


16 Gate charge waveforms

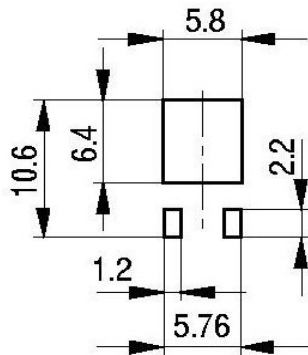


Package Outline

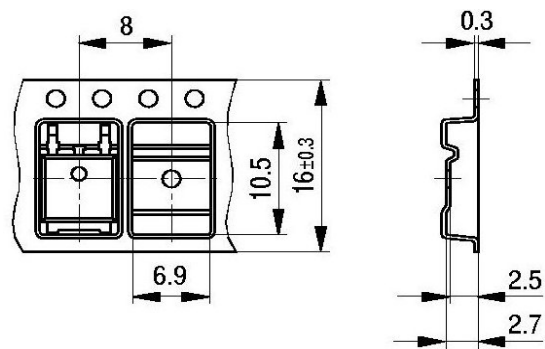
P-TO252-3-11: Outline



Footprint:



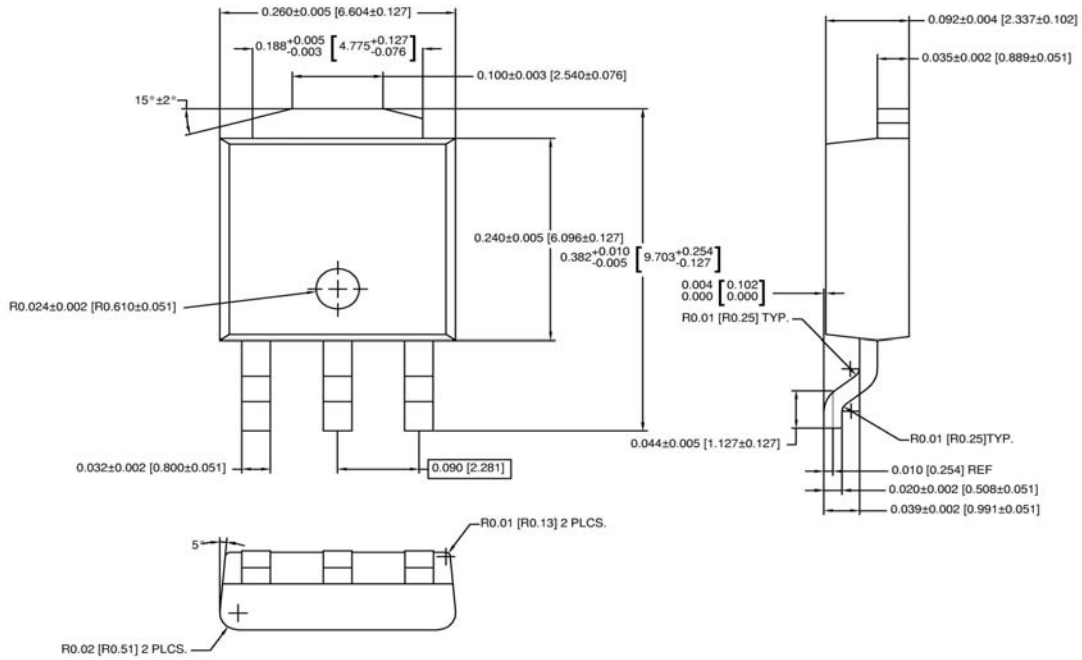
Packaging:



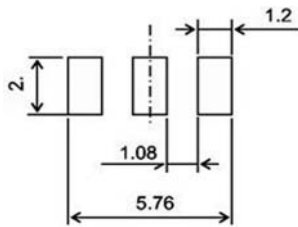
Dimensions in mm

Package Outline

P-TO252-3-23: Outline



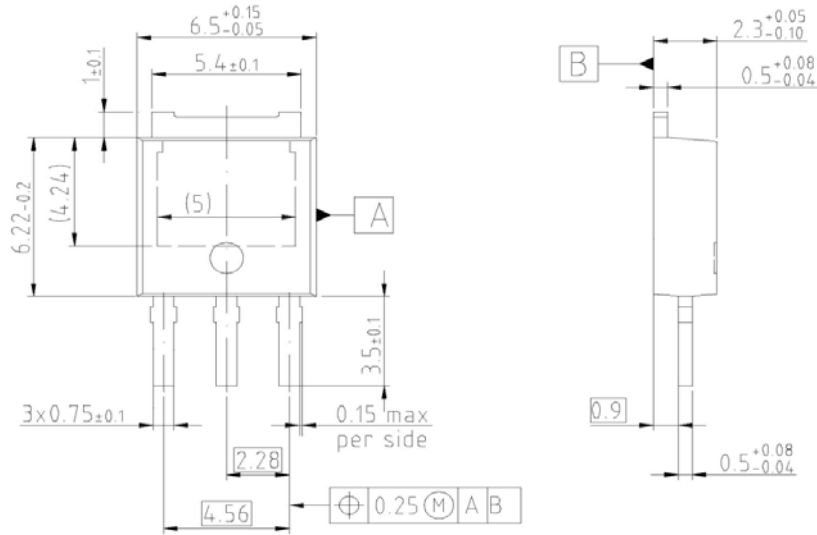
Footprint:



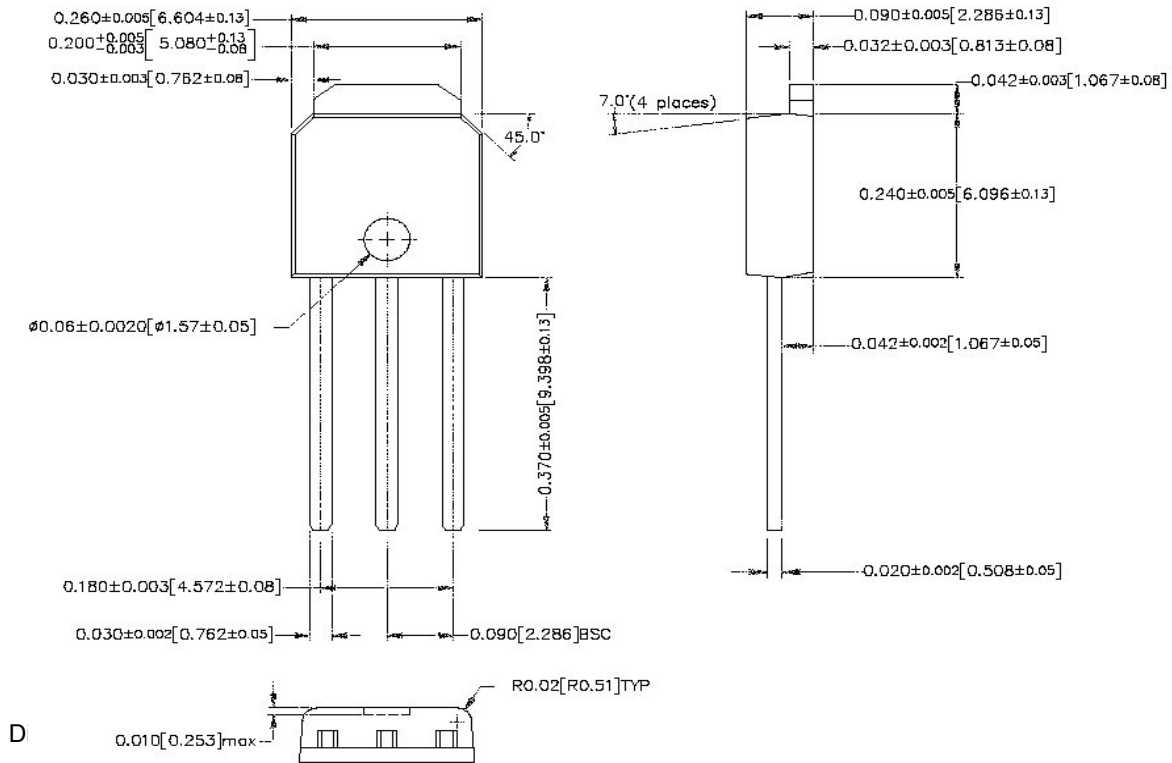
Dimensions in inch [mm]

Package Outline

P-TO251-3-11: Outline



P-TO251-3-21: Outline





IPD13N03LA IPF13N03LA

IPS13N03LA IPU13N03LA

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