# ISL6268

## High-Performance Notebook PWM Controller

FN6348
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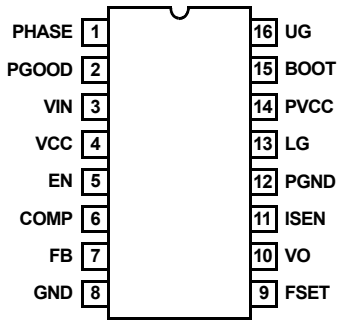
The ISL6268 IC is a Single-Phase Synchronous-Buck PWM controller featuring Intersil's Robust Ripple Regulator ($R^3$) technology that delivers truly superior dynamic response to input voltage and output load transients. Integrated MOSFET drivers and bootstrap diode result in fewer components and smaller implementation area.

Intersil's $R^3$ technology combines the best features of fixed-frequency PWM and hysteretic PWM while eliminating many of their shortcomings. $R^3$ technology employs an innovative modulator that synthesizes an AC ripple voltage signal $V_R$, analogous to the output inductor ripple current. The AC signal $V_R$ enters a window comparator where the lower threshold is the error amplifier output $V_{COMP}$, and the upper threshold is a programmable voltage reference $V_W$, resulting in generation of the PWM signal. The voltage reference $V_W$ sets the steady-state PWM frequency. Both edges of the PWM can be modulated in response to input voltage transients and output load transients, much faster than conventional fixed-frequency PWM controllers. Unlike a conventional hysteretic converter, the ISL6268 has an error amplifier that provides ±1% voltage regulation at the FB pin.

The ISL6268 has a 1.5ms digital soft-start and can be started into a pre-biased output voltage. A resistor divider is used to program the output voltage setpoint. The ISL6268 normally operates in continuous-conduction-mode (CCM), automatically entering diode-emulation-mode (DEM) at low load for optimum efficiency. In CCM the converter operates as a synchronous rectifier. In DEM the low-side MOSFET stays off, blocking negative current flow from the output inductor.

## Pinout

**ISL6268 (16 LD SSOP)**
TOP VIEW




## Features

- High performance $R^3$ technology
- Fast transient response
- ±1% regulation accuracy: -10°C to +100°C
- Wide input voltage range: +7.0V to +25.0V
- Output voltage range: +0.6V to +3.3V
- Wide output load range: 0A to 25A
- Diode emulation mode for increased light load efficiency
- Programmable PWM frequency: 200kHz to 600kHz
- Pre-biased output start-up capability
- Integrated MOSFET drivers and bootstrap diode
- Internal digital soft-start
- Power good monitor
- Fault protection
  - Undervoltage protection
  - Soft crowbar overvoltage protection
  - Low-side MOSFET $r_{DS(on)}$ overcurrent protection
  - Over-temperature protection
  - Fault identification by PGOOD pull-down resistance
- Pb-free plus anneal available (RoHS compliant)

## Applications

- PCI express graphical processing unit
- Auxiliary power rail
- VRM
- Network adapter

## Ordering Information

| PART NUMBER | PART MARKING | TEMP (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|
| ISL6268CAZ (Note) | 6268CAZ | -10 to +100 | 16 Ld QSOP (Pb-free) | M16.15A |
| ISL6268CAZ-T (Note) | 6268CAZ | 16 Ld QSOP Tape and Reel (Pb-free) | | M16.15A |

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Block Diagram

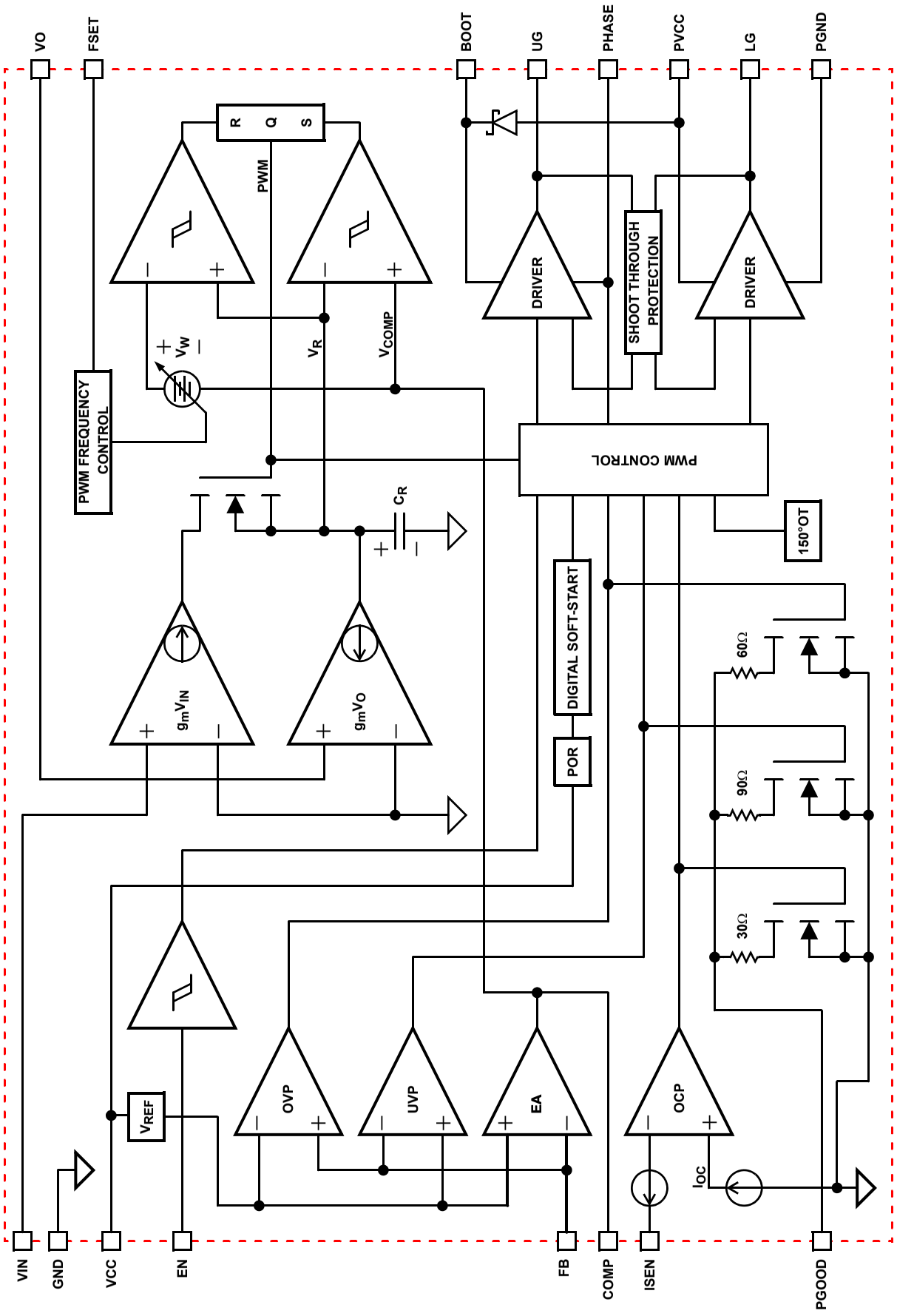
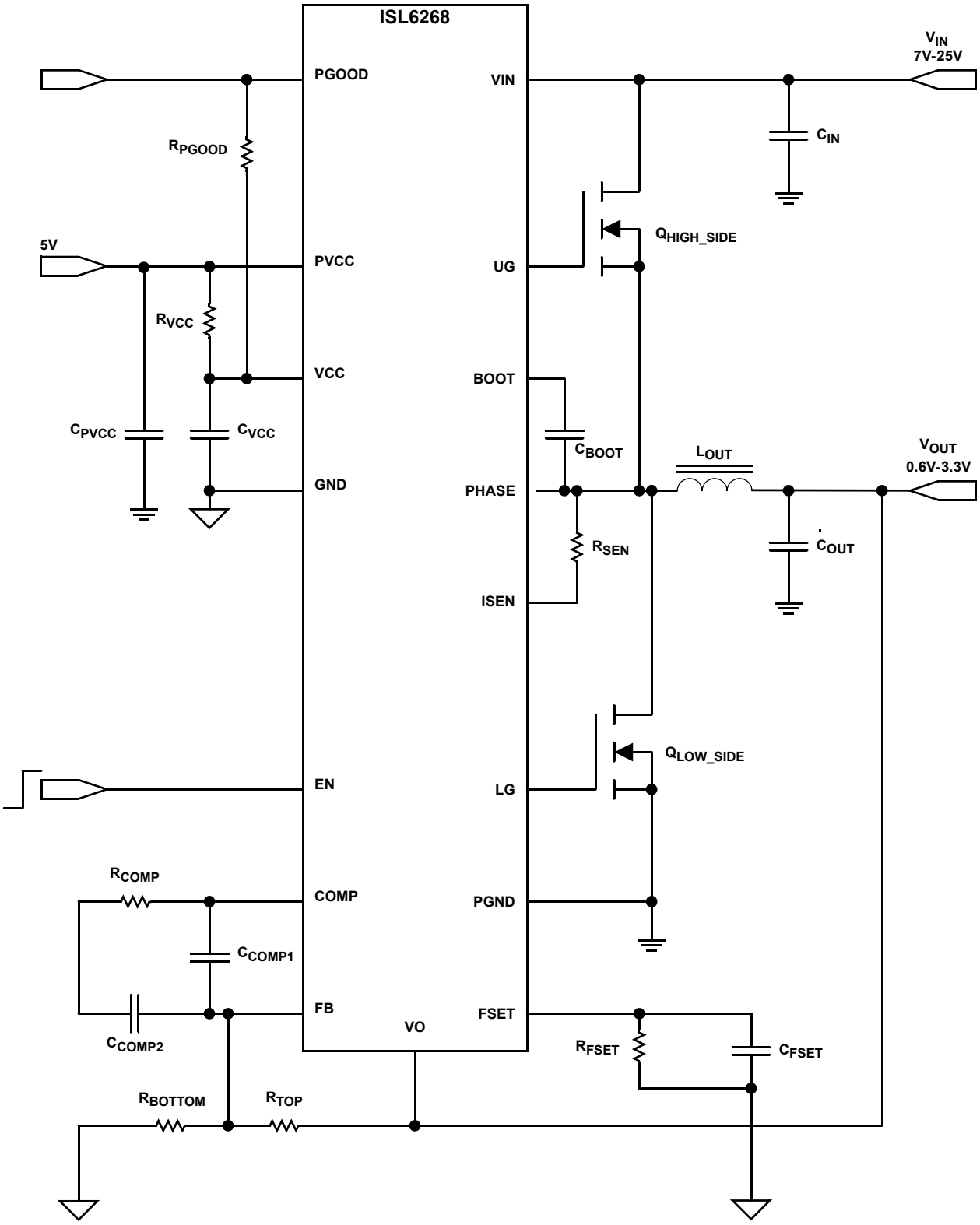



FIGURE 1. SCHEMATIC BLOCK DIAGRAM

## *Typical Application*



## Absolute Voltage Ratings

ISEN, VIN to GND . . . . . -0.3V to +28V
VCC, PGOOD to GND . . . . . -0.3V to +7.0V
PVCC to PGND . . . . . -0.3V to +7.0V
GND to PGND . . . . . -0.3V to +0.3V
EN . . . . . -0.3V to GND, VCC +3.3V
VO, FB, COMP, FSET . . . . . -0.3V to GND, VCC +0.3V
PHASE to GND (DC) . . . . . -0.3V to +28V
(<100ns Pulse Width, 10µJ) . . . . . -5.0V
BOOT to GND, or PGND . . . . . -0.3V to +33V
BOOT to PHASE . . . . . -0.3V to +7V
UG (DC) . . . . . -0.3V to PHASE, BOOT +0.3V
(<200ns Pulse Width, 20µJ) . . . . . -4.0V
LG (DC) . . . . . -0.3V to PGND, PVCC +0.3V
(<100ns Pulse Width, 4µJ) . . . . . -2.0V

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| QSOP Package | 105 |

Junction Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . +300°C

## Recommended Operating Conditions

Ambient Temperature Range . . . . . -10°C to +100°C
Supply Voltage (VIN to GND) . . . . . 7V to 25V
VCC to GND . . . . . .5V ±5%
PVCC to PGND . . . . . .5V ±5%

*CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.*

NOTES:

1. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications

These specifications apply for $T_A$ = -10°C to +100°C, unless otherwise stated.
All typical specifications $T_A$ = +25°C, VCC = 5V, PVCC = 5V

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VIN** | | | | | | |
| VIN Input Bias Current | $I_{VIN}$ | EN = 5V, VIN = 7V | - | 6.5 | 10 | µA |
| | | EN = 5V, VIN = 25V | - | 26 | 35 | µA |
| VIN Shutdown Current | $I_{VIN\_SHDN}$ | EN = GND, VIN = 25V | - | 0.1 | 1.0 | µA |
| **VCC and PVCC** | | | | | | |
| VCC Input Bias Current | $I_{VCC}$ | EN = 5V, FB = 0.65V, VIN = 7V to 25V | - | 1.7 | 2.5 | mA |
| VCC Shutdown Current | $I_{VCC\_SHDN}$ | EN = GND, VCC = 5V | - | 0.1 | 1.0 | µA |
| PVCC Shutdown Current | $I_{PVCC\_SHDN}$ | EN = GND, PVCC = 5V | - | 0.1 | 1.0 | µA |
| **VCC POR THRESHOLD** | | | | | | |
| Rising VCC POR Threshold Voltage | $V_{VCC\_THR}$ | | 4.35 | 4.45 | 4.55 | V |
| Falling VCC POR Threshold Voltage | $V_{VCC\_THF}$ | | 4.10 | 4.20 | 4.30 | V |
| **REGULATION** | | | | | | |
| Reference Voltage | $V_{REF}$ | | - | 0.6 | - | V |
| Regulation Accuracy | | FB connected to COMP | -1 | - | +1 | % |
| **PWM** | | | | | | |
| Frequency Range | $F_{SW}$ | | 200 | - | 600 | kHz |
| Frequency-Set Accuracy | | $F_{SW}$ = 300kHz | -12 | - | +12 | % |
| VO Range | $V_{VO}$ | | 0.60 | - | 3.30 | V |
| VO Input Leakage | $I_{VO}$ | VO = 0.60V | - | 1.3 | - | µA |
| | | VO = 3.30V | - | 7.0 | - | µA |
| **ERROR AMPLIFIER** | | | | | | |
| FB Input Bias Current | $I_{FB}$ | FB = 0.60V | -0.5 | - | +0.5 | µA |
| COMP Source Current | $I_{COMP\_SRC}$ | FB = 0.40V, COMP = 3.20V | - | 2.5 | - | mA |
| COMP Sink Current | $I_{COMP\_SNK}$ | FB = 0.80V, COMP = 0.30V | - | 0.3 | - | mA |
| COMP High Clamp Voltage | $V_{COMP\_HC}$ | FB = 0.40V, Sink 50µA | 3.10 | 3.40 | 3.65 | V |
| COMP Low Clamp Voltage | $V_{COMP\_LC}$ | FB = 0.80V, Source 50µA | 0.09 | 0.15 | 0.21 | V |

**Electrical Specifications** These specifications apply for $T_A$ = -10°C to +100°C, unless otherwise stated. All typical specifications $T_A$ = +25°C, VCC = 5V, PVCC = 5V **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER GOOD** | | | | | | |
| PGOOD Pull-Down Impedance | $R_{PG\_SS}$ | PGOOD = 5mA Sink | 75 | 95 | 125 | Ω |
| | $R_{PG\_UV}$ | PGOOD = 5mA Sink | 75 | 95 | 125 | Ω |
| | $R_{PG\_OV}$ | PGOOD = 5mA Sink | 50 | 63 | 85 | Ω |
| | $R_{PG\_OC}$ | PGOOD = 5mA Sink | 25 | 32 | 45 | Ω |
| PGOOD Leakage Current | $I_{PGOOD}$ | PGOOD = 5V | - | 0.1 | 1.0 | µA |
| PGOOD Maximum Sink Current (Note 2) | | | - | 5.0 | - | mA |
| PGOOD Soft-Start Delay | $T_{SS}$ | EN High to PGOOD High | 2.20 | 2.75 | 3.30 | ms |
| **GATE DRIVER** | | | | | | |
| UG Pull-Up Resistance | $R_{UGPU}$ | 200mA Source Current | - | 1.0 | 1.5 | Ω |
| UG Source Current (Note 2) | $I_{UGSRC}$ | UG - PHASE = 2.5V | - | 2.0 | - | A |
| UG Sink Resistance | $R_{UGPD}$ | 250mA Sink Current | - | 1.0 | 1.5 | Ω |
| UG Sink Current (Note 2) | $I_{UGSNK}$ | UG - PHASE = 2.5V | - | 2.0 | - | A |
| LG Pull-Up Resistance | $R_{LGPU}$ | 250mA Source Current | - | 1.0 | 1.5 | Ω |
| LG Source Current (Note 2) | $I_{LGSRC}$ | LG - PGND = 2.5V | - | 2.0 | - | A |
| LG Sink Resistance | $R_{LGPD}$ | 250mA Sink Current | - | 0.5 | 0.9 | Ω |
| LG Sink Current (Note 2) | $I_{LGSNK}$ | LG - PGND = 2.5V | - | 4.0 | - | A |
| UG to LG Deadtime | $t_{UGFLGR}$ | UG falling to LG rising, no load | - | 21 | - | ns |
| LG to UG Deadtime | $t_{LGFUGR}$ | LG falling to UG rising, no load | - | 14 | - | ns |
| **BOOTSTRAP DIODE** | | | | | | |
| Forward Voltage | $V_F$ | PVCC = 5V, $I_F$ = 2mA | - | 0.58 | - | V |
| Reverse Leakage | $I_R$ | $V_R$ = 25V | - | 0.2 | - | µA |
| **CONTROL INPUTS** | | | | | | |
| EN High Threshold | $V_{ENTHR}$ | | 2.0 | - | - | V |
| EN Low Threshold | $V_{ENTHF}$ | | - | - | 1.0 | V |
| EN Leakage | $I_{ENL}$ | EN = 0V | - | 0.1 | 1.0 | µA |
| | $I_{ENH}$ | EN = 5.0V | - | 0.1 | 1.0 | µA |
| **PROTECTION** | | | | | | |
| ISEN OCP Threshold | $I_{OC}$ | ISEN sourcing | 19 | 26 | 33 | µA |
| ISEN Short-Circuit Threshold | $I_{SC}$ | ISEN sourcing | - | 50 | - | µA |
| UVP Threshold | $V_{UV}$ | | 81 | 84 | 87 | % |
| OVP Rising Threshold | $V_{OVR}$ | | 113 | 116 | 119 | % |
| OVP Falling Threshold | $V_{OVF}$ | | 100 | 103 | 106 | % |
| OTP Rising Threshold (Note 2) | $T_{OTR}$ | | - | 150 | - | °C |
| OTP Hysteresis (Note 2) | $T_{OTHYS}$ | | - | 25 | - | °C |

NOTE:

2. Guaranteed by characterization.

## Functional Pin Descriptions

**PHASE (Pin 1)**

The PHASE pin detects the voltage polarity of the PHASE node and is also the current return path for the UG high-side MOSFET gate driver. Connect the PHASE pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor.

**PGOOD (Pin 2)**

The PGOOD pin is an open-drain output that indicates when the converter is able to supply regulated voltage. Connect the PGOOD pin to +5V through a pull-up resistor.

**VIN (Pin 3)**

The VIN pin measures the converter input voltage which is a required input to the $R^3$ PWM modulator. Connect across the drain of the high-side MOSFET to the GND pin.

**VCC (Pin 4)**

The VCC pin is the input bias voltage for the IC. Connect +5V from the VCC pin to the GND pin. Decouple with at least 1µF of a MLCC capacitor from the VCC pin to the GND pin.

**EN (Pin 5)**

The EN pin is the on/off switch of the IC. The soft-start sequence begins when the EN pin is pulled above the rising threshold voltage $V_{ENTHR}$ and VCC is above the power-on reset (POR) rising threshold voltage $V_{VCC\_THR}$. When the EN pin is pulled below the falling threshold voltage $V_{ENTHF}$, PWM immediately stops.

**COMP (Pin 6)**

The COMP pin is the output of the control-loop error amplifier. Compensation components for the control-loop connect across the COMP and FB pins.

**FB (Pin 7)**

The FB pin is the inverting input of the control-loop error amplifier. The converter output voltage regulates to 600mV from the FB pin to the GND pin. Program the desired output voltage with a resistor network connected across the VO, FB, and GND pins. Select the resistor values such that FB to GND is 600mV when the converter output voltage is at the programmed regulation value.

**GND (Pin 8)**

Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin, not the PGND pin.

**FSET (Pin 9)**

The FSET pin programs the PWM switching frequency. Program the desired PWM frequency with a resistor and a capacitor connected across the FSET and GND pins.

**VO (Pin 10)**

The VO pin measures the converter output voltage and is used exclusively as an input to the $R^3$ PWM modulator. Connect at the physical location where the best output voltage regulation is desired.

**ISEN (Pin 11)**

The ISEN pin programs the threshold of the OCP overcurrent fault protection. Program the desired OCP threshold with a resistor connected across the ISEN and PHASE pins. The OCP threshold is programmed to detect the peak current of the output inductor. The peak current is the sum of the DC and AC components of the inductor current.

**PGND (Pin 12)**

The PGND pin conducts the turn-off transient current through the LG gate driver. The PGND pin must be connected to complete the pull-down circuit of the LG gate driver. The PGND pin should be connected to the source of the low-side MOSFET through a low impedance path, preferably in parallel with the trace connecting the LG pin to the gate of the low-side MOSFET. The adaptive shoot-through protection circuit measures the low-side MOSFET gate-source voltage from the LG pin to the PGND pin.

**LG (Pin 13)**

The LG pin is the output of the low-side MOSFET gate driver. Connect to the gate of the low-side MOSFET.

**PVCC (Pin 14)**

The PVCC pin is the input voltage bias for the LG low-side MOSFET gate driver. Connect +5V from the PVCC pin to the PGND pin. Decouple with at least 1µF of an MLCC capacitor across the PVCC and PGND pins.

**BOOT (Pin 15)**

The BOOT pin stores the input voltage for the UG high-side MOSFET gate driver. Connect an MLCC capacitor across the BOOT and PHASE pins. The boot capacitor is charged through an internal boot diode connected from the PVCC pin to the BOOT pin, each time the PHASE pin drops below PVCC minus the voltage dropped across the internal boot diode.

**UG (Pin 16)**

The UG pin is the output of the high-side MOSFET gate driver. Connect to the gate of the high-side MOSFET.

## Theory of Operation

### Modulator

The ISL6268 is a hybrid of fixed frequency PWM control, and variable frequency hysteretic control. Intersil's $R^3$ technology can simultaneously affect the PWM switching frequency and PWM duty cycle in response to input voltage and output load transients. The term "Ripple" in the name "Robust Ripple Regulator" refers to the converter output inductor ripple current, not the converter output ripple voltage. The $R^3$ modulator synthesizes an AC signal $V_R$, which is an ideal representation of the output inductor ripple current. The duty-cycle of $V_R$ is the result of charge and discharge current through a ripple capacitor $C_R$. The current through $C_R$ is provided by a transconductance amplifier $g_m$ that measures the VIN and VO pin voltages. The positive slope of $V_R$ can be written as:

$$V_{RPOS} = (g_m)\cdot(V_{IN} - V_{OUT}) \quad \text{(EQ. 1)}$$

The negative slope of $V_R$ can be written as:

$$V_{RNEG} = g_m \cdot V_{OUT} \quad \text{(EQ. 2)}$$

where $g_m$ is the gain of the transconductance amplifier.

A window voltage $V_W$ is referenced with respect to the error amplifier output voltage $V_{COMP}$, creating an envelope into which the ripple voltage $V_R$ is compared. The amplitude of $V_W$ is set by a resistor connected across the FSET and GND pins. The $V_R$, $V_{COMP}$, and $V_W$ signals feed into a window comparator in which $V_{COMP}$ is the lower threshold voltage and $V_W$ is the higher threshold voltage. Figure 2 shows PWM pulses being generated as $V_R$ traverses the $V_W$ and $V_{COMP}$ thresholds . The PWM switching frequency is proportional to the slew rates of the positive and negative slopes of $V_R$; the PWM switching frequency is inversely proportional to the voltage between $V_W$ and $V_{COMP}$.

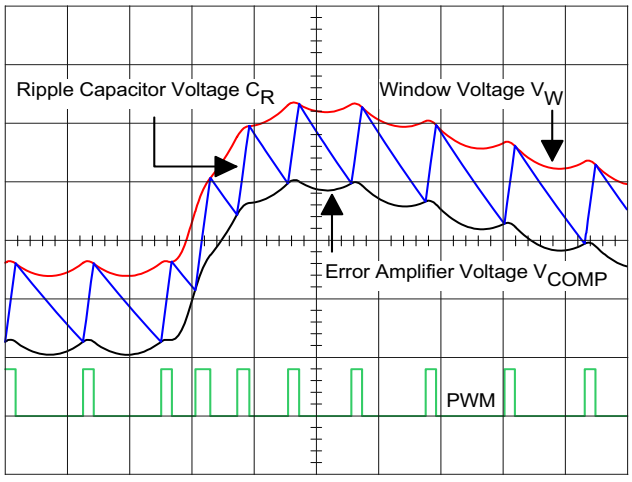



**FIGURE 2. MODULATOR WAVEFORMS DURING LOAD TRANSIENT**

### Power-On Reset

The ISL6268 is disabled until the voltage at the VCC pin has increased above the rising power-on reset (POR) $V_{CCR}$ threshold voltage. The controller will become once again disabled when the voltage at the VCC pin decreases below the falling POR $V_{CCF}$ threshold voltage.

### EN, Soft-Start, and PGOOD

The ISL6268 uses a digital soft-start circuit to ramp the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of the soft-start sequence has been selected to limit the inrush current through the output capacitors as they charge to the desired regulation voltage. When the EN pin is pulled above the rising EN threshold voltage $V_{ENTHR}$ the PGOOD Soft-Start Delay $T_{SS}$ begins and the output voltage begins to rise. The output voltage enters regulation in approximately 1.5ms and the PGOOD pin goes to high impedance once $T_{SS}$ has elapsed.

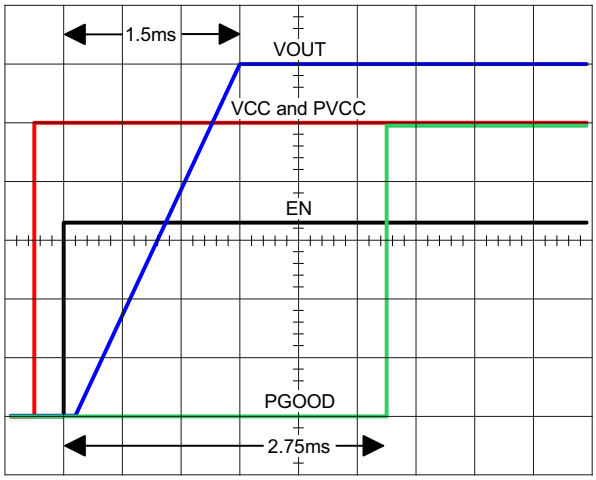



**FIGURE 3. SOFT-START SEQUENCE**

The PGOOD pin indicates when the converter is capable of supplying regulated voltage. The PGOOD pin is an undefined impedance if $V_{CC}$ has not reached the rising POR threshold $V_{CCR}$, or if $V_{CC}$ is below the falling POR threshold $V_{CCF}$. The ISL6268 features a unique fault-identification capability that can drastically reduce trouble-shooting time and effort. The pull-down resistance of the PGOOD pin corresponds to the fault status of the controller. During soft-start or if an undervoltage fault occurs, the PGOOD pull-down resistance is 95Ω, or 32Ω for an overcurrent fault, or 63Ω for an overvoltage fault.

**TABLE 1. PGOOD PULL-DOWN RESISTANCE**

| CONDITION | PGOOD RESISTANCE |
|---|---|
| VCC below POR | Undefined |
| Soft Start or Undervoltage | 95Ω |
| Overvoltage | 63Ω |
| Overcurrent | 32Ω |

The ISL6268 has internal gate-drivers for the high-side and low-side N-Channel MOSFETs. The LG gate-driver is optimized for low duty-cycle applications where the low-side MOSFET conduction losses are dominant, requiring a low $r_{DS(on)}$ MOSFET. The LG pull-down resistance is small in order to clamp the gate of the MOSFET below the $V_{GS(th)}$ at turn-off. The current transient through the gate at turnoff can be considerable because the switching charge of a low $r_{DS(on)}$ MOSFET can be large. Adaptive shoot-through protection prevents a gate-driver output from turning on until the opposite gate-driver output has fallen below approximately 1V. The dead-time shown in Figure 4 is extended by the additional period that the falling gate voltage stays above the 1V threshold. The high-side gate-driver output voltage is measured across the UG and PHASE pins while the low-side gate-driver output voltage is measured across the LG and PGND pins. The power for the LG gate-driver is sourced directly from the PVCC pin. The power for the UG gate-driver is sourced from a “boot” capacitor connected across the BOOT and PHASE pins. The boot capacitor is charged from a 5V bias supply through a “boot diode” each time the low-side MOSFET turns on, pulling the PHASE pin low. The ISL6268 has an integrated boot diode connected from the PVCC pin to the BOOT pin.

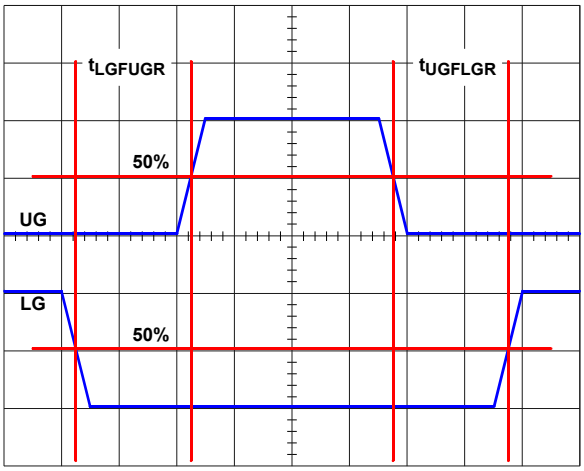



**FIGURE 4. LG AND UG DEAD-TIME**

### *Diode Emulation*

The ISL6268 normally operates in continuous conduction mode (CCM), minimizing conduction losses by forcing the low-side MOSFET to operate as a synchronous rectifier. An improvement in light-load efficiency is achieved by allowing the converter to operate in diode-emulation-mode (DEM), where the low-side MOSFET behaves as a smart-diode, forcing the device to block negative inductor current flow. Positive-going inductor current flows from either the source of the high-side MOSFET, or the drain of the low-side MOSFET. Negative-going inductor current usually flows into the drain of the low-side MOSFET. When the low-side MOSFET conducts positive inductor current, the phase voltage will be negative with respect to the GND and PGND pins. Conversely, when the low-side MOSFET conducts negative inductor current, the phase voltage will be positive with respect to the GND and PGND pins. Negative inductor current occurs when the output load current is less than half the inductor ripple current. Sinking negative inductor through the low-side MOSFET lowers efficiency through unnecessary conduction losses. Efficiency can be further improved with a reduction of unnecessary switching losses by reducing the PWM frequency. It is characteristic of the $R^3$ architecture for the PWM frequency to decrease while in diode emulation. The extent of the frequency reduction is proportional to the reduction of load current. Upon entering DEM, the PWM frequency makes an initial step-reduction because of a 33% step-increase of the window voltage $V_W$. The converter will automatically enter DEM after the PHASE pin has detected positive voltage, while the LG gate-driver pin is high, for eight consecutive PWM pulses. The converter will return to CCM on the following cycle after the PHASE pin detects negative voltage, indicating that the body diode of the low-side MOSFET is conducting positive inductor current.

### *Overcurrent and Short Circuit Protection*

The overcurrent protection (OCP) and short circuit protection (SCP) setpoint is programmed with resistor $R_{SEN}$ that is connected across the ISEN and PHASE pins. The PHASE pin is connected to the drain terminal of the low-side MOSFET.

The SCP setpoint is internally set to twice the OCP setpoint. When an OCP or SCP fault is detected, the PGOOD pin will pull down to 32Ω and latch off the converter. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage $V_{ENTHF}$ or if $V_{CC}$ has decayed below the falling POR threshold voltage $V_{VCC\_THF}$.

The OCP circuit does not directly detect the DC load current leaving the converter. The OCP circuit detects the peak of positive-flowing output inductor current. The low-side MOSFET drain current $I_D$ is assumed to be equal to the positive output inductor current when the high-side MOSFET is off. The inductor current develops a negative voltage across the $r_{DS(on)}$ of the low-side MOSFET that is measured shortly after the LG gate-driver output goes high. The ISEN pin sources the OCP sense current $I_{SEN,}$ through the OCP programming resistor $R_{SEN,}$ forcing the ISEN pin to 0V with respect to the GND pin. The negative voltage across the PHASE and GND pins is nulled by the voltage dropped across $R_{SEN}$ as $I_{SEN}$ conducts through it. An OCP fault occurs if $I_{SEN}$ rises above

the OCP threshold current $I_{OC}$ while attempting to null the negative voltage across the PHASE and GND pins. $I_{SEN}$ must exceed $I_{OC}$ on all the PWM pulses that occur within 20µs. If $I_{SEN}$ falls below $I_{OC}$ on a PWM pulse before 20µs has elapsed, the timer will be reset. An SCP fault will occur within 10µs when $I_{SEN}$ exceeds twice $I_{OC}$. The relationship between $I_D$ and $I_{SEN}$ is written as:

$$I_{SEN} \cdot R_{SEN} = I_D \cdot r_{DS(on)} \quad \text{(EQ. 3)}$$

The value of $R_{SEN}$ is then written as:

$$R_{SEN} = \frac{\left(I_{FL} + \frac{I_{PP}}{2}\right) \cdot OC_{SP} \cdot r_{DS(on)}}{I_{OC}} \quad \text{(EQ. 4)}$$

where:

- $R_{SEN}$ (Ω) is the resistor used to program the overcurrent setpoint
- $I_{SEN}$ is the current sense current that is sourced from the ISEN pin
- $I_{OC}$ is the $I_{SEN}$ threshold current sourced from the ISEN pin that will activate the OCP circuit
- $I_{FL}$ is the maximum continuous DC load current
- $I_{PP}$ is the inductor peak-to-peak ripple current
- $OC_{SP}$ is the desired overcurrent setpoint expressed as a multiplier relative to $I_{FL}$

### *Overvoltage Protection*

When an OVP fault is detected, the PGOOD pin will pull down to 63Ω and latch-off the converter. The OVP fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage $V_{ENTHF}$ or if $V_{CC}$ has decayed below the falling POR threshold voltage $V_{VCC\_THF}$.

The OVP fault detection circuit triggers after the voltage across the FB and GND pins has increased above the rising overvoltage threshold $V_{OVR}$. After the converter has latched-off in response to an OVP fault, the LG gate-driver output will retain the ability to toggle the low-side MOSFET on and off in response to the output voltage transversing the $V_{OVR}$ and $V_{OVF}$ thresholds.

### *Undervoltage Protection*

When a UVP fault is detected, the PGOOD pin will pull down to 95Ω and latch-off the converter. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage $V_{ENTHF}$ or if $V_{CC}$ has decayed below the falling POR threshold voltage $V_{VCC\_THF}$. The UVP fault detection circuit triggers after the voltage across the FB and GND pins has fallen below the undervoltage threshold $V_{UV}$.

### *Over-Temperature*

When the temperature of the ISL6268 increases above the rising threshold temperature $T_{OTR}$, the IC will enter an OTP state that suspends the PWM , forcing the LG and UG gate-driver outputs low. The status of the PGOOD pin does not change nor does the converter latch-off. The PWM remains suspended until the IC temperature falls below the hysteresis temperature $T_{OTHYS}$ at which time normal PWM operation resumes. The OTP state can be reset if the EN pin is pulled below the falling EN threshold voltage $V_{ENTHF}$ or if $V_{CC}$ decays below the falling POR threshold voltage $V_{VCC\_THF}$. All other protection circuits function normally during OTP. It is likely that the IC will detect an UVP fault because in the absence of PWM, the output voltage immediately decays below the undervoltage threshold $V_{UV}$; the PGOOD pin will pull down to 95Ω and latch-off the converter. The UVP fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage $V_{ENTHF}$ or if $V_{CC}$ has decayed below the falling POR threshold voltage $V_{VCC\_THF}$.

### *Programming the Output Voltage*

When the converter is in regulation there will be 600mV from the FB pin to the GND pin. Connect a two-resistor voltage divider across the VO pin and the GND pin with the output node connected to the FB pin. Scale the voltage-divider network such that the FB pin is 600mV with respect to the GND pin when the converter is regulating at the desired output voltage. The output voltage can be programmed from 600mV to 3.3V.

Programming the output voltage is written as:

$$V_{REF} = V_{OUT} \cdot \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \quad \text{(EQ. 5)}$$

where:

- $V_{OUT}$ is the desired output voltage of the converter
- $V_{REF}$ is the voltage that the converter regulates to between the FB pin and the GND pin
- $R_{TOP}$ is the voltage-programming resistor that connects from the FB pin to the VO pin. In addition to setting the output voltage, this resistor is part of the loop compensation network
- $R_{BOTTOM}$ is the voltage-programming resistor that connects from the FB pin to the GND pin

Beginning with $R_{TOP}$ between 1kΩ to 5kΩ, calculating $R_{BOTTOM}$ is written as:

$$R_{BOTTOM} = \frac{V_{REF} \cdot R_{TOP}}{V_{OUT} - V_{REF}} \quad \text{(EQ. 6)}$$

### *Programming the PWM Switching Frequency*

The ISL6268 does not use a clock signal to produce PWM. The PWM switching frequency $F_{SW}$ is programmed by the resistor $R_{FSET}$ that is connected from the FSET pin to the GND pin. The approximate PWM switching frequency is written as:

$$F_{SW} = \frac{1}{K \cdot R_{FSET}} \quad \text{(EQ. 7)}$$

Estimating the value of $R_{FSET}$ is written as:

$$R_{FSET} = \frac{1}{K \cdot F_{SW}} \quad \text{(EQ. 8)}$$

where:

- $F_{SW}$ is the PWM switching frequency
- $R_{FSET}$ is the $F_{SW}$ programming resistor
- $K = 75 \times 10^{-12}$

It is recommended that whenever the control loop compensation network is modified, $F_{SW}$ should be checked for the correct frequency and if necessary, adjust $R_{FSET}$.

### *Compensation Design*

The LC output filter has a double pole at its resonant frequency that causes the phase to abruptly roll downward. The $R^3$ modulator used in the ISL6268 makes the LC output filter resemble a first order system in which the closed loop stability can be achieved with a Type II compensation network.

Your local Intersil representative can provide a PC-based tool that can be used to calculate compensation network component values and help simulate the loop frequency response. The compensation network consists of the internal error amplifier of the ISL6268 and the external components R1, R2, C1, and C2, as well as the frequency setting components $R_{FSET}$ and $C_{FSET}$ (all identified in Figure 5).

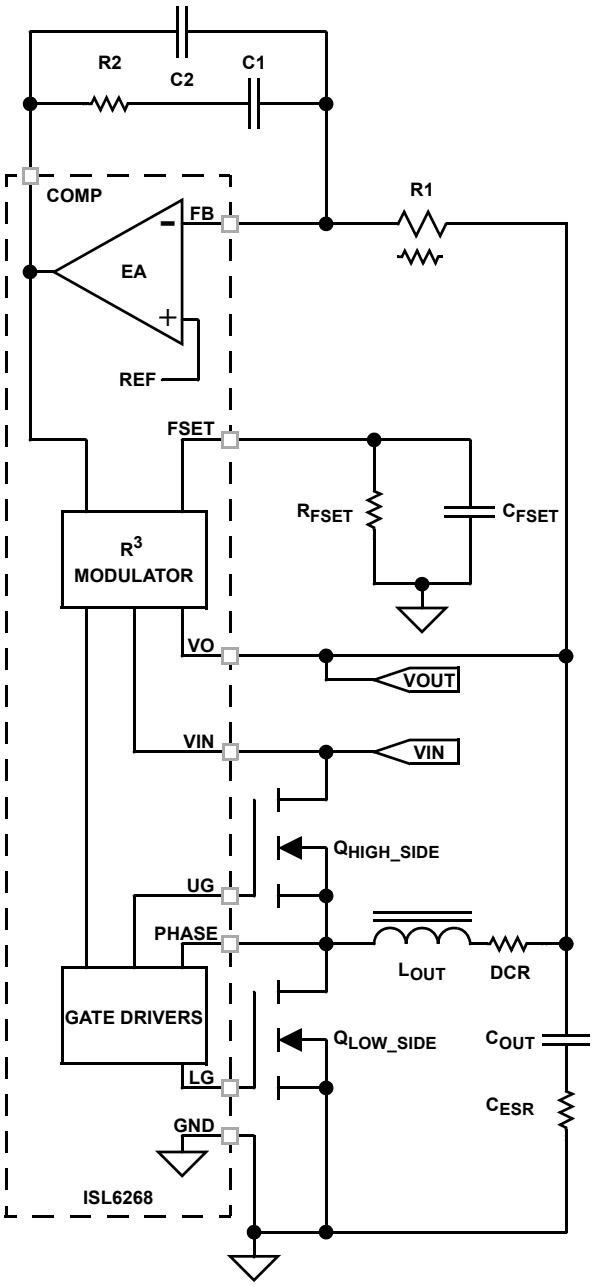



**FIGURE 5. COMPENSATION REFERENCE CIRCUIT**

## General Application Design

This document is intended to provide a high-level explanation of the steps necessary to create a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following sections. In addition to this document, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts.

### Selecting the LC Output Filter

The duty cycle of an ideal buck converter is a function of the input and the output voltage. This relationship is written as:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 9)}$$

The output inductor peak-to-peak ripple current is written as:

$$I_{PP} = \frac{V_{OUT} \cdot (1 - D)}{F_{SW} \cdot L_{OUT}} \quad \text{(EQ. 10)}$$

A typical step-down DC/DC converter will have an $I_{PP}$ of 20% to 40% of the maximum DC output load current. The value of $I_{PP}$ is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding. The DC copper loss of the inductor can be estimated by:

$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR \quad \text{(EQ. 11)}$$

where $I_{LOAD}$ is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperature. A saturated inductor could cause destruction of circuit components, as well as nuisance OCP faults.

A DC/DC buck regulator must have output capacitance $C_{OUT}$ into which ripple current $I_{PP}$ can flow. Current $I_{PP}$ develops a corresponding ripple voltage $V_{PP}$ across $C_{OUT}$, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written as:

$$\Delta V_{ESR} = I_{PP} \cdot ESR \quad \text{(EQ. 12)}$$

and

$$\Delta V_{C} = \frac{I_{PP}}{8 \cdot C_{OUT} \cdot F_{SW}} \quad \text{(EQ. 13)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors will need to be paralleled to reduce the total ESR until the required $V_{PP}$ is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors constructed with reverse package geometry are available. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that $I_{PP}$ is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at $F_{SW}$. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

### Selection of the Input Capacitor

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. Figure 6 is a graph of the input RMS ripple current, normalized relative to output load current, as a function of duty cycle that is adjusted for converter efficiency. The ripple current calculation is written as:

$$I_{IN\_RMS} = \frac{\sqrt{\left(I_{MAX}^{2} \cdot (D - D^{2})\right) + \left(x \cdot I_{MAX}^{2} \cdot \frac{D}{12}\right)}}{I_{MAX}} \quad \text{(EQ. 14)}$$

where:

- $I_{MAX}$ is the maximum continuous $I_{LOAD}$ of the converter
- x is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of $I_{MAX}$ (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter which is written as:

$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF} \quad \text{(EQ. 15)}$$

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

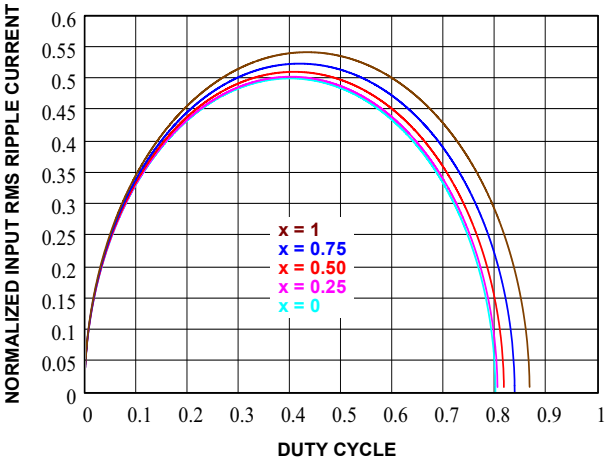



**FIGURE 6. NORMALIZED RMS INPUT CURRENT FOR x = 0.8**

### MOSFET Selection and Considerations

Typically, a MOSFET cannot tolerate even brief excursions beyond their maximum drain to source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum $V_{DS}$ rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

There are several power MOSFETs readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low switch charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET which has the drain-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with $V_{IN} - V_{OUT} - V_L$ across it. The preferred low-side MOSFET emphasizes low $r_{DS(on)}$ when fully saturated to minimize conduction loss.

For the low-side MOSFET, (LS), the power loss can be assumed to be conductive only and is written as:

$$P_{CON\_LS} \approx I_{LOAD}^2 \cdot r_{DS(on)\_LS} \cdot (1 - D) \quad \text{(EQ. 16)}$$

For the high-side MOSFET, (HS), its conduction loss is written as:

$$P_{CON\_HS} = I_{LOAD}^2 \cdot r_{DS(on)\_HS} \cdot D \quad \text{(EQ. 17)}$$

For the high-side MOSFET, its switching loss is written as:

$$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot T_{ON} \cdot F_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot T_{OFF} \cdot F_{SW}}{2} \quad \text{(EQ. 18)}$$

where:

- $I_{VALLEY}$ is the difference of the DC component of the inductor current minus half of the inductor ripple current
- $I_{PEAK}$ is the sum of the DC component of the inductor current plus half of the inductor ripple current
- $T_{ON}$ is the time required to drive the device into saturation
- $T_{OFF}$ is the time required to drive the device into cut-off

### Selecting The Bootstrap Capacitor

The selection of the bootstrap capacitor is written as:

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad \text{(EQ. 19)}$$

where:

- $Q_g$ is the total gate charge required to turn on the high-side MOSFET
- $\Delta V_{BOOT}$, is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on

As an example, suppose the high-side MOSFET has a total gate charge $Q_g$ of 25nC at $V_{GS}$ = 5V, and a $\Delta V_{BOOT}$ of 200mV. The calculated bootstrap capacitance is 0.125µF. For a comfortable margin, select a capacitor that is double the calculated capacitance; in this example, 0.22µF will suffice. Use an X7R or X5R ceramic capacitor.

### Layout Considerations

As a general rule, power should be on the bottom layer of the PCB and weak analog or logic signals are on the top layer of the PCB. The ground-plane layer should be adjacent to the top layer to provide shielding. The ground plane layer should have an island located under the IC, the compensation components, and the FSET components. The island should be connected to the rest of the ground plane layer at one point.

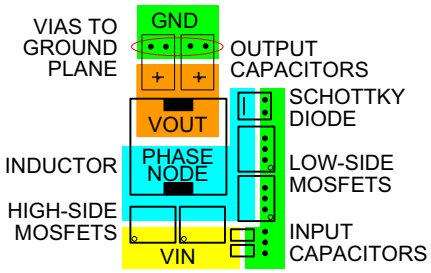



**FIGURE 7. TYPICAL POWER COMPONENT PLACEMENT**

### Signal Ground and Power Ground

The GND pin is the signal ground for analog and logic signals of the IC. For a robust thermal and electrical conduction path, connect the GND pin to the island of ground plane under the top layer using several vias. Connect the input capacitors, the output capacitors, and the source of the lower MOSFETs to the power ground plane.

**PGND (Pin 12)**

This is the return path for the pull-down of the LG low-side MOSFET gate driver. Ideally, PGND should be connected to the source of the low-side MOSFET with a low-resistance, low-inductance path.

**VIN (Pin 3)**

The VIN pin should be connected close to the drain of the high-side MOSFET, using a low resistance and low inductance path.

**VCC (Pin 4)**

For best performance, place the decoupling capacitor very close to the VCC and GND pins.

**PVCC (Pin 14)**

For best performance, place the decoupling capacitor very close to the PVCC and PGND pins, preferably on the same side of the PCB as the ISL6268 IC.

**EN (Pin 5), and PGOOD (Pin 2)**

These are logic inputs that are referenced to the GND pin. Treat as a typical logic signal.

**COMP (Pin 6), FB (Pin 7), and VO (Pin 10)**

For best results, use an isolated sense line from the output load to the VO pin. The input impedance of the FB pin is high, so place the voltage programming and loop compensation components close to the VO, FB, and GND pins keeping the high impedance trace short.

**FSET (Pin 9)**

This pin requires a quiet environment. The resistor $R_{FSET}$ and capacitor $C_{FSET}$ should be placed directly adjacent to this pin. Keep fast moving nodes away from this pin.

**ISEN (Pin 11)**

Route the connection to the ISEN pin away from the traces and components connected to the FB pin, COMP pin, and FSET pin.

**LG (Pin 13)**

The signal going through this trace is both high dv/dt and high di/dt, with high peak charging and discharging current. Route this trace in parallel with the trace from the PGND pin. These two traces should be short, wide, and away from other traces. There should be no other weak signal traces in proximity with these traces on any layer.

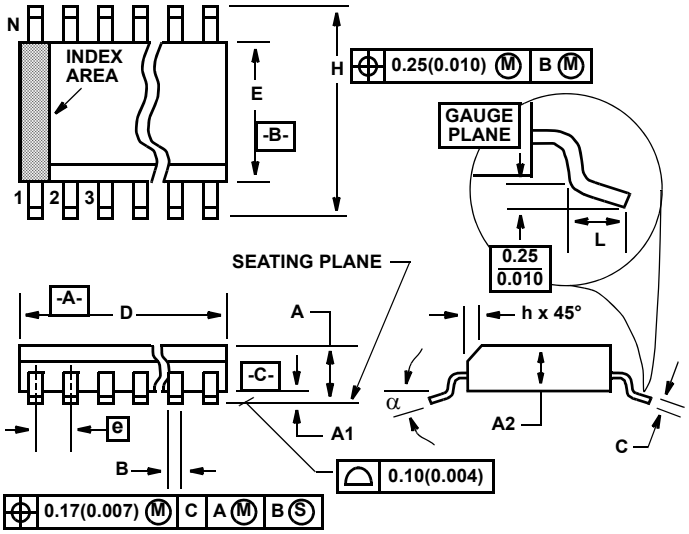
**BOOT (Pin 15), UG (Pin 16), and PHASE (Pin 1)**

The signals going through these traces are both high dv/dt and high di/dt, with high peak charging and discharging current. Route the UG and PHASE pins in parallel with short and wide traces. There should be no other weak signal traces in proximity with these traces on any layer.

### *Copper Size for the Phase Node*

The parasitic capacitance and parasitic inductance of the phase node should be kept very low to minimize ringing. It is best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application. An MLCC should be connected directly across the drain of the upper MOSFET and the source of the lower MOSFET to suppress the turn-off voltage spike.

## *Shrink Small Outline Plastic Packages (SSOP)*
## *Quarter Size Outline Plastic Packages (QSOP)*




### M16.15A

**16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150" WIDE BODY)**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.061 | 0.068 | 1.55 | 1.73 | - |
| A1 | 0.004 | 0.0098 | 0.102 | 0.249 | - |
| A2 | 0.055 | 0.061 | 1.40 | 1.55 | - |
| B | 0.008 | 0.012 | 0.20 | 0.31 | 9 |
| C | 0.0075 | 0.0098 | 0.191 | 0.249 | - |
| D | 0.189 | 0.196 | 4.80 | 4.98 | 3 |
| E | 0.150 | 0.157 | 3.81 | 3.99 | 4 |
| e | 0.025 BSC | | 0.635 BSC | | - |
| H | 0.230 | 0.244 | 5.84 | 6.20 | - |
| h | 0.010 | 0.016 | 0.25 | 0.41 | 5 |
| L | 0.016 | 0.035 | 0.41 | 0.89 | 6 |
| N | 16 | | 16 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 2 6/04

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.