64Kx8 Bit High Speed CMOS Static RAM

FEATURES

- Fast Access Time 55,70,85 ns (max.)
- Low Power Dissipation
  - Standby (CMOS): 550μW (max.) L Version
    110μW (max.) LL Version
  - Operating : 385mW(max.)
- Single 5V±10% Power Supply
- TTL compatible inputs and outputs
- Fully Static Operation
  - No clock or refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM68512LG/LG-L : 32-pin SOP (525mil)
  - KM68512LT/LT-L : 32-pin TSOP (Standard)

GENERAL DESCRIPTION

The KM68512L/L-L is a 524,288-bit high- speed Static Random Access Memory organized as 65,536 words by 8 bits.

The KM68512L/L-L uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

It is particularly well suited for use in high-density high-speed system and low power applications.

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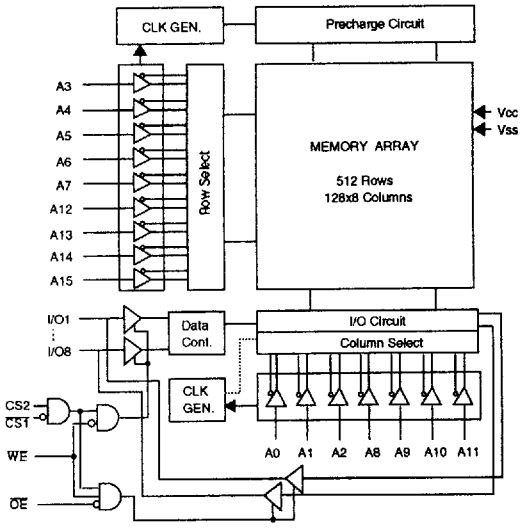
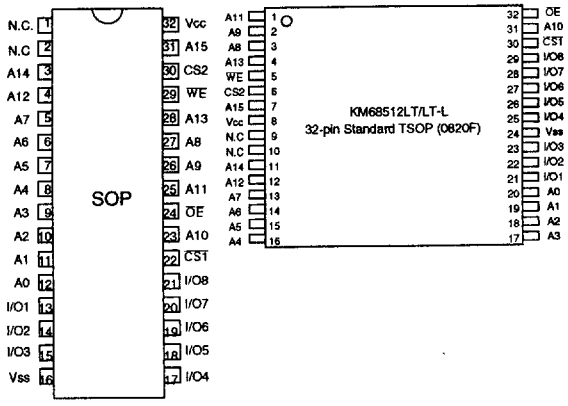
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$,CS2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1~I/O_8	Data Inputs/Outputs
V_{CC}	Power(+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10sec (Lead only)	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=-0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5	V
Input Low Voltage	V_{IL}	-0.3 *	-	0.8	V

* V_{IL}(Min.)= -3.0V for ≤50 ns Pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, Vcc=5V ± 10%, unless otherwise specified)

Item	Symbol	Test Condition		Min.	* Typ	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to Vcc		-1	-	1	µA
DC Operating Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2= V_{IH} V_{IN}-V_{IL} or V_{IH}, $I_{I/O}$=0mA		-	7	15	mA
Average Operating Current	I_{CC1}	Cycle Time=1µs, 100% Duty, $\overline{CS1}$≤0.2V, CS2≥Vcc-0.2V, $I_{I/O}$=0mA, V_{IL}≤0.2V, V_{IH}≥Vcc-0.2V		-	-	10	mA
	I_{CC2}	Min Cycle, 100% Duty $\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA		-	-	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}		-	-	3	mA
	I_{SB1}	$\overline{CS1}$≥Vcc-0.2V	L	-	2	100	µA
		CS2≥Vcc-0.2V or CS2≤0.2V	L - L	-	1	20	µA
Output Low Voltage	V_{OL}	Iol=2.1 mA		-	-	0.4	V
Output High Voltage	V_{OH}	Ioh=-1.0 mA		2.4	-	-	V

* Typ : Vcc=5V, Ta=25°C

CAPACITANCE *(f=1MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

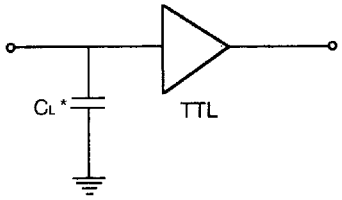
* Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

(T_A=0 to 70 °C, V_{CC}=5V ±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.8 to2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L*=100pF+1TTL

C_L* = 30pF for KM68512L-5/5L



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68512L-5 KM68512L-5 L		KM68512L-7 KM68512L-7 L		KM68512L-8 KM68512L-8 L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	55	-	70	-	80	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	80	ns
Chip Select to Output	t_{CO1},t_{CO2}	-	55	-	70	-	80	ns
Output Enable to Valid Output	t_{OE}	-	25	-	35	-	45	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	5	-	5	-	5	-	ns
Output Enable to Low-Z Output	t_{OLZ}	10	-	10	-	10	-	ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2},	0	20	0	25	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	0	30	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns

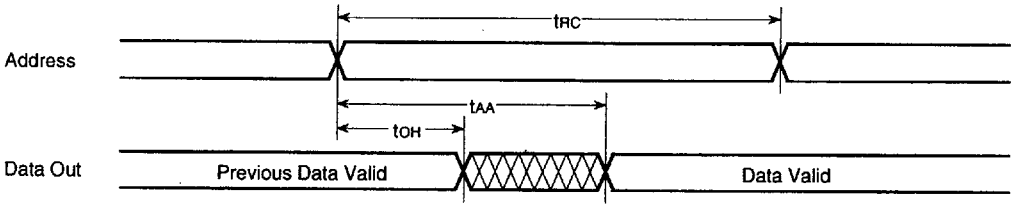
WRITE CYCLE

Farameter	Symbol	KM68512L-5 KM68512L-5 L		KM68512L-7 KM68512L-7 L		KM68512L-8 KM68512L-8 L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	55	-	70	-	85	-	ns
Chip Select to End of Write	tCW	45	-	60	-	70	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	45	-	60	-	70	-	ns
Write Pulse Width	tWP	40	-	50	-	55	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	20	0	25	0	30	ns
Data to Write Time Overlap	tDW	25	-	30	-	35	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	5	-	5	-	5	-	ns

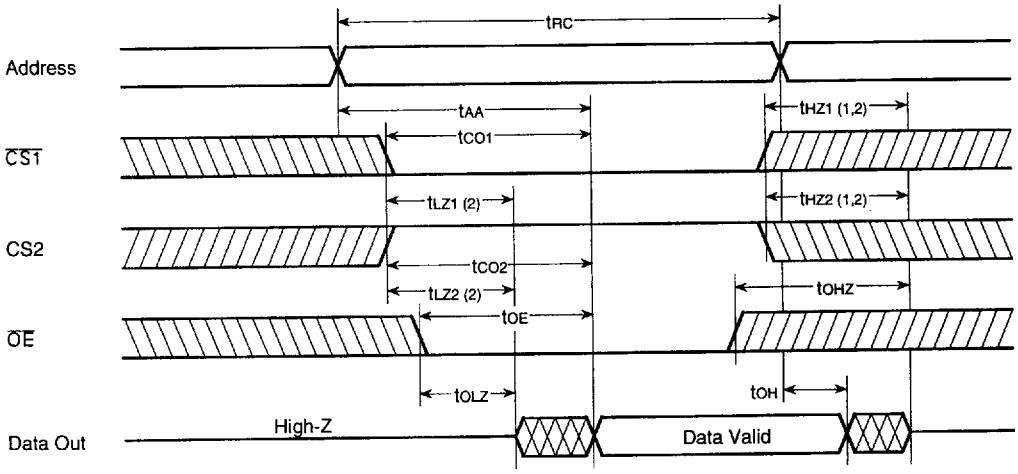
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS1}$=$\overline{OE}$=VIL, CS2=$\overline{WE}$=VIH)



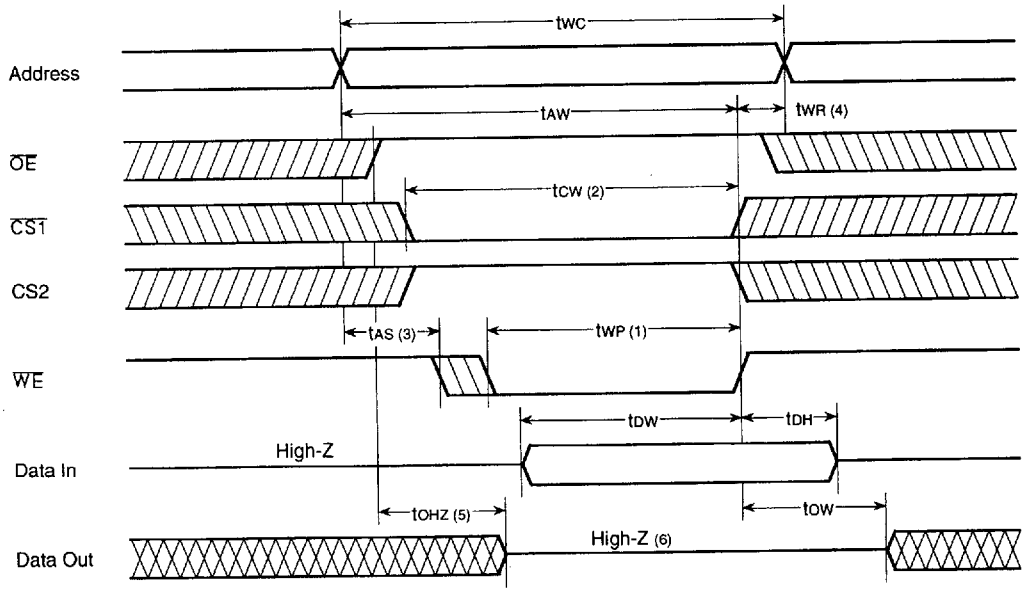
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



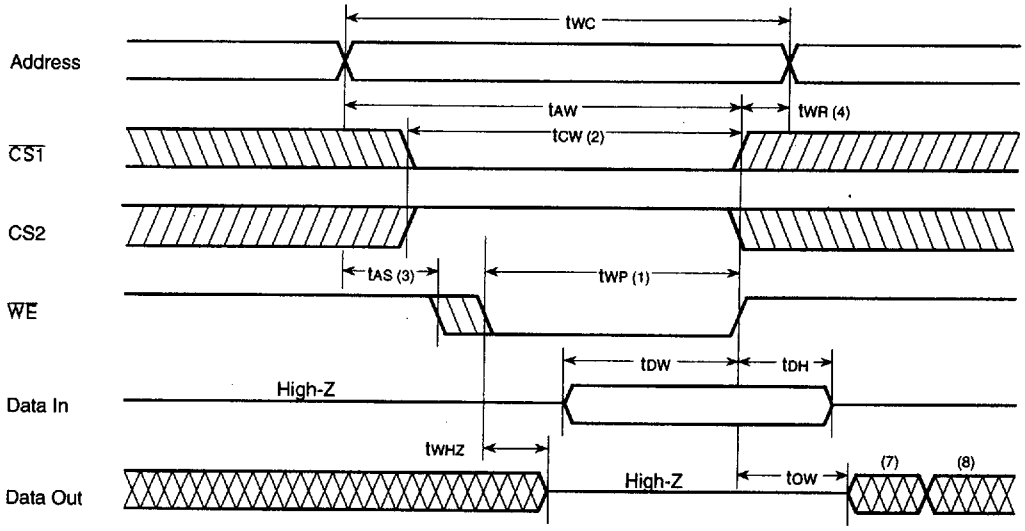
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are referenced to the VOH or VOL.
2. At any given temperature and voltage condition tHZ(max) is less than tLZ(min) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ Low Fixed)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured form the end of write to the address change.
5. During this period,I/O pins are in the output state, therefore, the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X	X	X	Power down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

Note : X means Don't Care.

DATA RETENTION CHARACTERISTICS (Ta= 0 to 70 °C)

PARAMETER	SYMBOL	TEST CONDITION		MIN	TYP	MAX	UNIT
Vcc for Data Retention	Vdr	*$\overline{CS1}$≥Vcc-0.2V		2.0	-	5.5	V
Data Retention Current	Idr	Vcc=3.0V	L		1	50	μA
		$\overline{CS1}$≥VCC-0.2V	L-L		0.5	10	μA
Data Retention Set-up Time	tSDR	See Data Retention		0	-	-	ns
Recovery Time	tRDR	Waveforms (below)		5	-	-	ms

* $\overline{CS1}$≥Vcc-0.2,CS2≥VCC-0.2($\overline{CS1}$ Controlled) or CS2≤0.2(CS2 Controlled)

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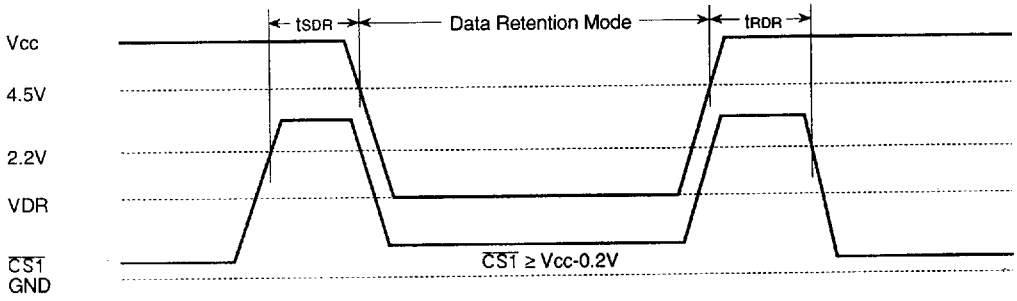
DATA RETENTION WAVEFORM 1 ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM 2 (CS2 Controlled)