

## Transition-Mode PFC Controller with Fault Condition Protection

REV. 00

### General Description

The LD7591 is a voltage mode PFC controller operating on transition mode, with several integrated functions of protection, such as OVP, OCP, and Brown-in protection. It reduces the components counts and is available in a SOP-8 or DIP-8 package. Those make it an ideal design for low cost applications.

It provides functions of low startup current, over voltage protection, open feedback protection, disable function, over current protection, under voltage lockout and integrated LEB of current sensing. Unlike the traditional current mode PFC controller, LD7591 is free from extra rectified AC line voltage information to minimize the power loss.

The LD7591 will be disabled if INV pin voltage falls below 0.45V and the operating current rises over 65 $\mu$ A

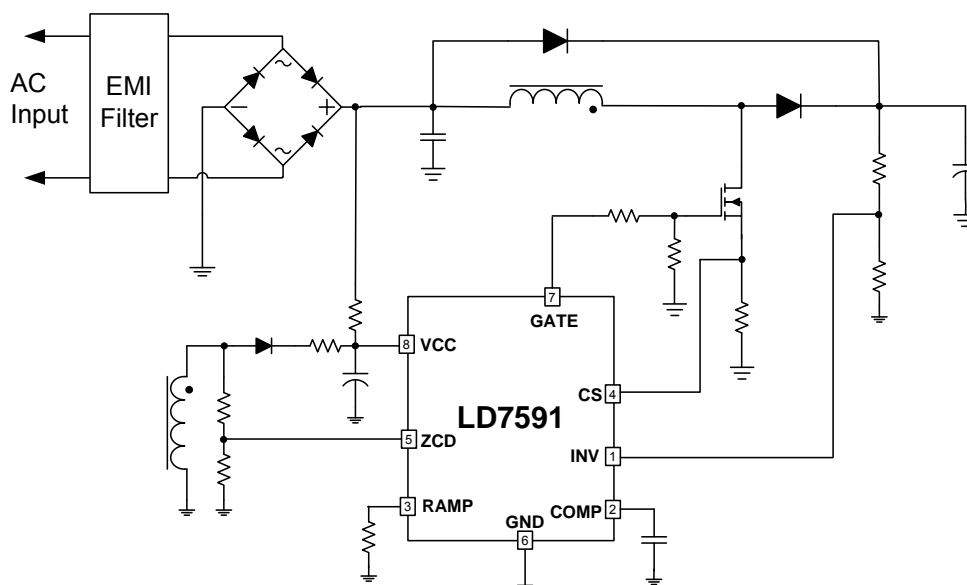
### Features

- Transition mode of PFC pre-regulator
- Voltage mode control
- Programmable max. on-time
- Low Startup Current (<30 $\mu$ A)
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Open-Feedback Protection and Disable Function
- OVP (Over Voltage Protection)
- OCP (Cycle by cycle current limiting)
- 800/-1200mA Driving Capability
- Internal OTP function

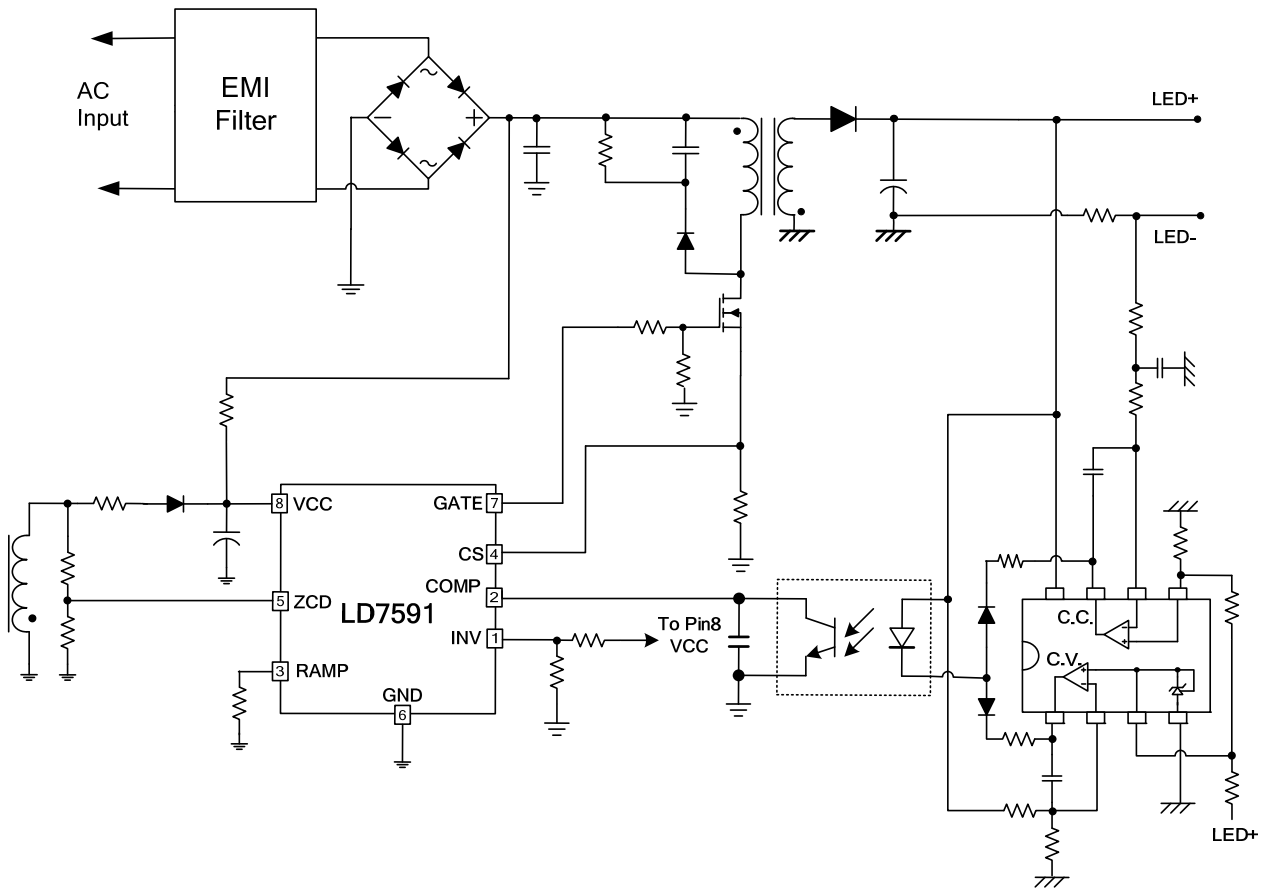
### Applications

- Adaptor of Output above 65W.
- Open Frame Switching Power Supply
- LCD TV Power Supply
- LED Power Supply

### Typical Application for Boost PFC

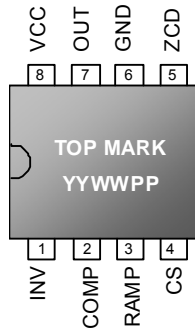


## Typical Application for LED (Flyback PFC)



## Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code (D:2004, E:2005...)  
 WW: Week code  
 PP: Production code

## Ordering Information

Part number	Package		Top Mark	Shipping
LD7591 GS	SOP-8	Green package	LD7591GS	2500 /tape & reel
LD7591 GN	DIP-8	Green package	LD7591GN	3600 /tube /Carton

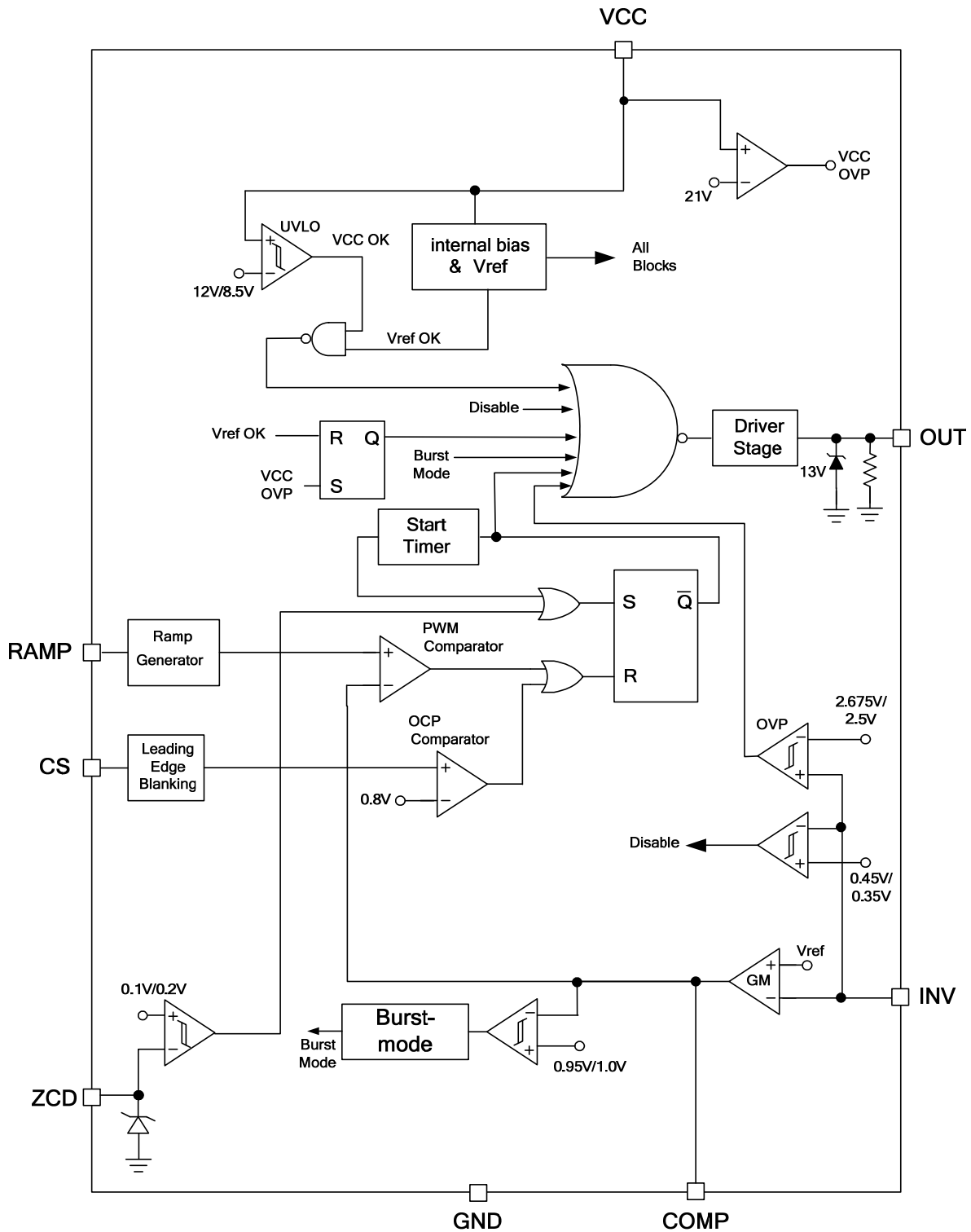
## Pin Descriptions

Pin	NAME	FUNCTION
1	INV	Output voltage feed back control
2	COMP	Output of the error amplifier for voltage loop compensation to achieve stable
3	RAMP	Ramp generator, connecting a resistor to GND pin to set the saw tooth signal
4	CS	Current sense pin, connect to sense the MOSFET current for OCP
5	ZCD	Detecting zero crossing of input signal
6	GND	Ground
7	OUT	Gate drive output to drive the external MOSFET
8	VCC	Power source VCC pin

## Recommended Operating Conditions

Item	Min.	Max.	Unit
Vcc pin capacitor	22	47	μF
Comp pin capacitor	0.1	4.7	μF
RAMP pin resistor	4.7k	100k	Ω

**Block Diagram**



## Absolute Maximum Ratings

Supply Voltage VCC .....	-0.3 ~26V
OUT .....	-0.3 ~VCC +0.3V
COMP, INV, CS, RAMP, ZCD .....	-0.3 ~7V
Maximum Junction Temperature .....	150°C
Operating Junction Temperature Range .....	-40°C to 125°C
Operating Ambient Temperature Range .....	-40°C to 85°C
Storage Temperature Range .....	-65°C to 150°C
Package Thermal Resistance (SO-8, $\theta_{JA}$ ) .....	160°C/W
Package Thermal Resistance (DIP-8, $\theta_{JA}$ ) .....	100°C/W
Power Dissipation (SOT-8, at Ambient Temperature = 85°C) .....	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C) .....	650mW
Lead temperature (Soldering, 10sec) .....	260°C
ESD Voltage Protection, Human Body Model .....	2.5 KV
ESD Voltage Protection, Machine Model .....	250 V
Gate Output Current .....	800mA/-1200mA

### Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Electrical Characteristics

( $V_{CC}=14.0V$ ,  $T_A = 25^{\circ}C$  unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Voltage (VCC Pin)</b>					
Startup Current	$V_{CC} < UVLO$ ON		20	30	$\mu A$
Operating Current (with 1nF load on OUT pin)	$V_{COMP}=0V$		2.0		mA
	$V_{COMP}=3V$		2.5		mA
	$V_{CC}$ OVP		0.45		mA
	$V_{INV}=0V$		65	95	$\mu A$
UVLO (off)		7.5	8.5	9.5	V
UVLO (on)		11.0	12.0	13.0	V
VCC OVP Level		19.5	21	22.5	V
<b>Error Amplifier (Comp Pin)</b>					
Feedback Input Voltage, $V_{REF}$		2.465	2.500	2.535	V
Input Bias Current	$V_{INV}=1V\sim 4V$	-0.5		0.5	$\mu A$
Transconductance			140		$\mu mho$
Output Sink Current	$V_{INV}= V_{REF} +0.1V$		14		$\mu A$
Output Source Current	$V_{INV}= V_{REF} -0.1V$		-14		$\mu A$
Output Source Current	$V_{INV}= V_{REF} -0.5V$		-200		$\mu A$
Output Upper Clamp Voltage	$V_{INV}= V_{REF} -0.1V$	5.4	5.9	6.4	V
Burst Mode COMP pin Threshold voltage			0.95		V
	Hysteresis		50		mV
<b>INV pin</b>					
OVP Trip Level		2.62	2.675	2.73	V
	OVP Hysteresis		0.175		V
Enable Threshold Voltage		0.4	0.45	0.5	V
	Enable Hysteresis		0.1		V
<b>Current Sensing (CS Pin)</b>					
Current Sense Input Threshold Voltage		0.75	0.8	0.85	V
Input bias current	$V_{CS}=0V\sim 1V$	0		1.0	$\mu A$
LEB time			250		ns
<b>Zero Current Detector (ZCD Pin)</b>					
Upper Clamp Voltage	$I_{DET}=100\mu A$		6.0		V
Lower Clamp Voltage	$I_{DET}=100\mu A$		-0.7		V
Input Voltage Threshold		0.05	0.1	0.15	V
	Hysteresis		0.1		V
Input bias current	$V_{ZCD}=1V\sim 4V$ , OUT=OFF	0.0	1.0		$\mu A$
Maximum Delay from ZCD to Output			250		ns

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Maximum ON-Time, Ton-max (Ramp Pin)</b>					
Maximum On Time Voltage	$R_{RAMP}=40.5K$	2.784	2.900V	3.016	V
Maximum On Time Programming	$R_{RAMP} =40.5K$	19	24	29	$\mu s$
Maximum On Time	$R_{RAMP} \geq 100K$		40		$\mu s$
<b>Minimum OFF-Time</b>					
Minimum OFF-Time			1		$\mu s$
Minimum OFF-Time Programming			0.10		Ton-max
<b>Gate Drive Output (OUT Pin)</b>					
Output Low Level	$V_{CC}=12V, I_{SINK}=20mA$			0.5	V
Output High Level	$V_{CC}=12V, I_{SOURCE}=20mA$	9		12	V
Output High Clamp Level	$V_{CC}=18V$		13		V
Rising Time	$V_{CC} =12V, CL=1000pF$		75	150	ns
Falling Time	$V_{CC} =12V, CL=1000pF$		25	100	ns
<b>Starter</b>					
Start Timer Period		50	150	300	$\mu s$
<b>OTP (Over Temp. Protection)</b>					
OTP Trip level			140		$^{\circ}C$
OTP Hysteresis			30		$^{\circ}C$

## Typical Performance Characteristics

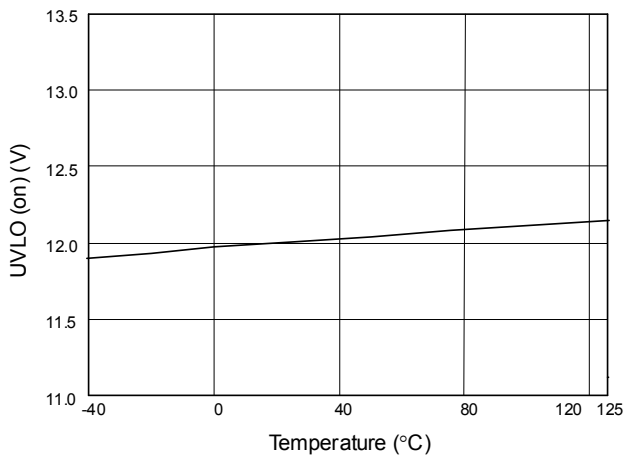


Fig. 1 UVLO (on) vs. Temperature

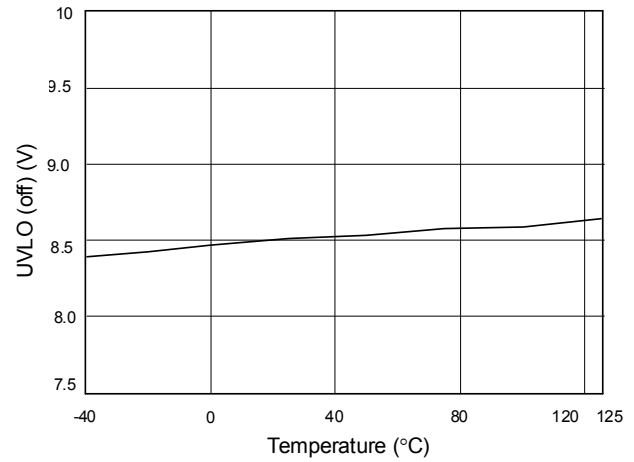


Fig. 2 UVLO (off) vs. Temperature

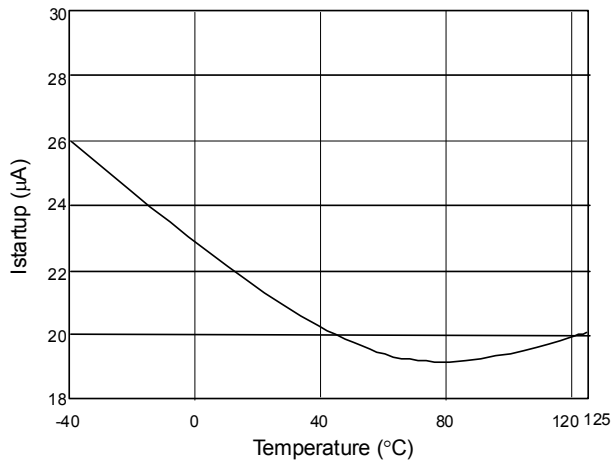


Fig. 3 Startup Current vs. Temperature

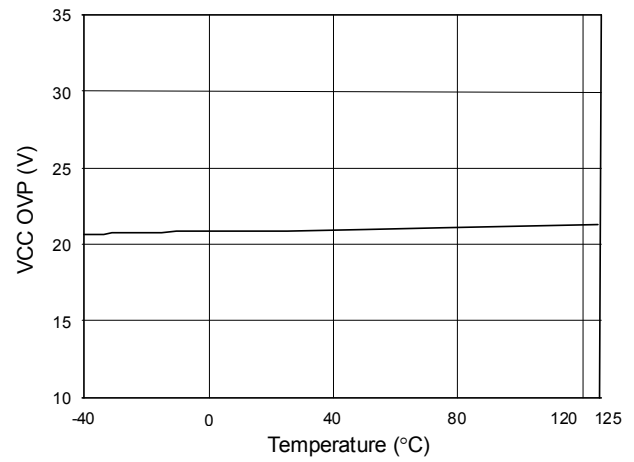


Fig. 4 VCC OVP vs. Temperature

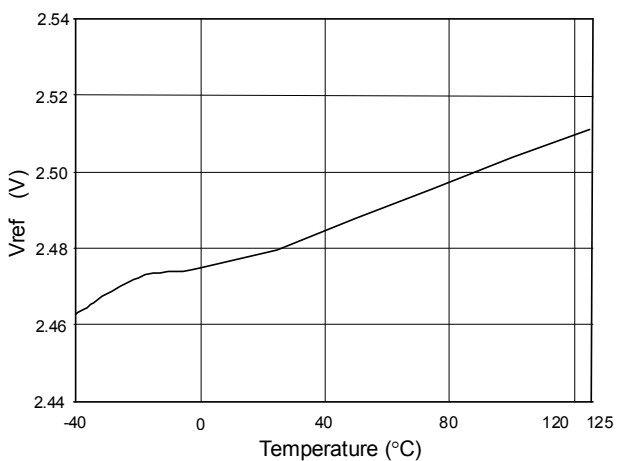


Fig. 5 Vref vs. Temperature

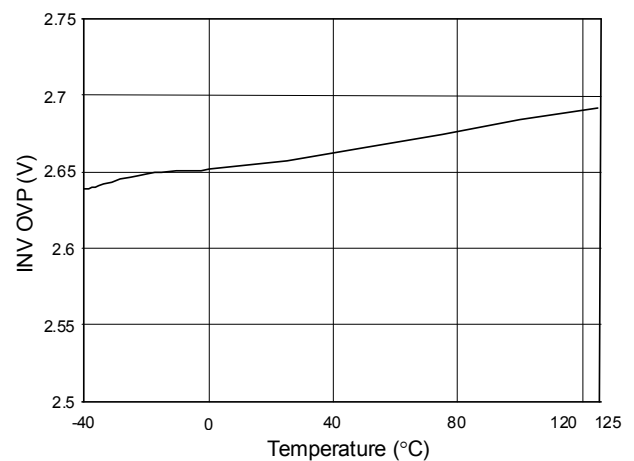


Fig. 6 INV OVP vs. Temperature



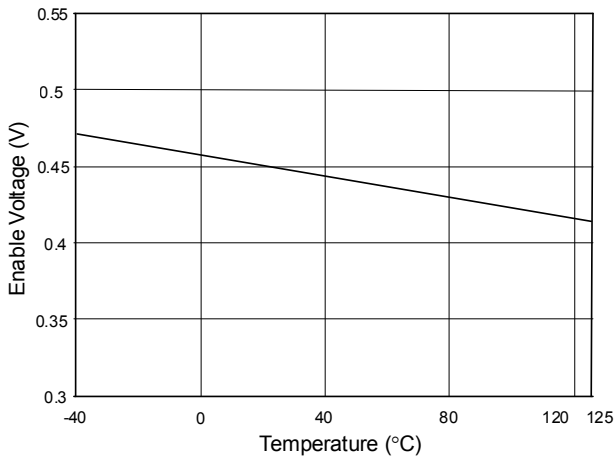


Fig. 7 Enable Voltage vs. Temperature

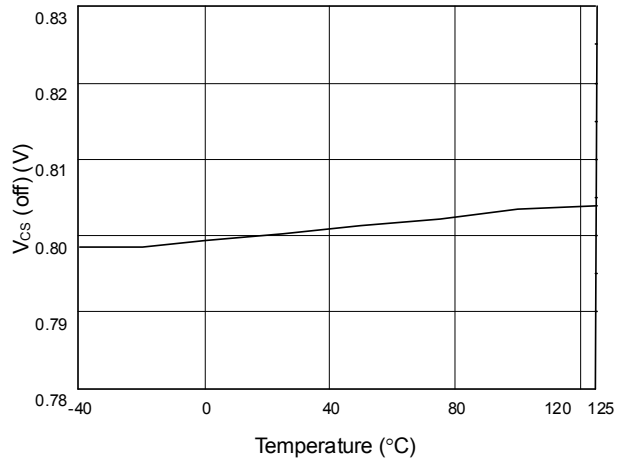


Fig. 8 V<sub>CS</sub> (off) vs. Temperature

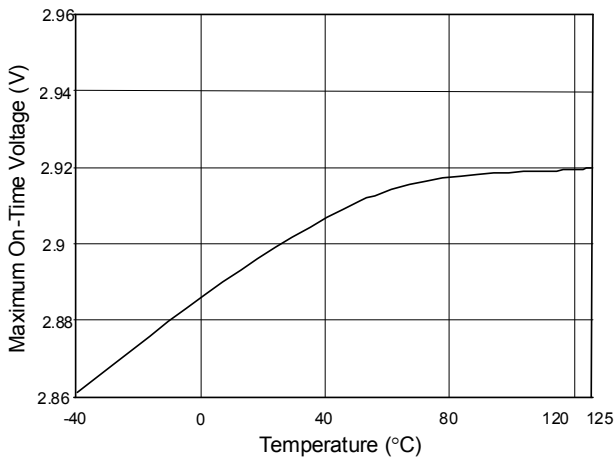


Fig. 9 Maximum On-Time Voltage vs. Temperature

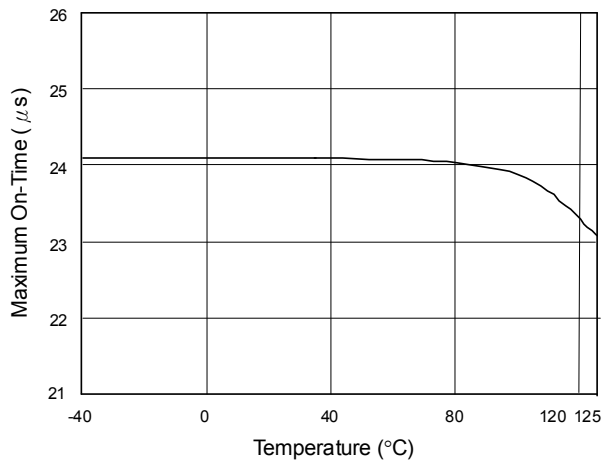


Fig. 10 Maximum On-Time vs. Temperature

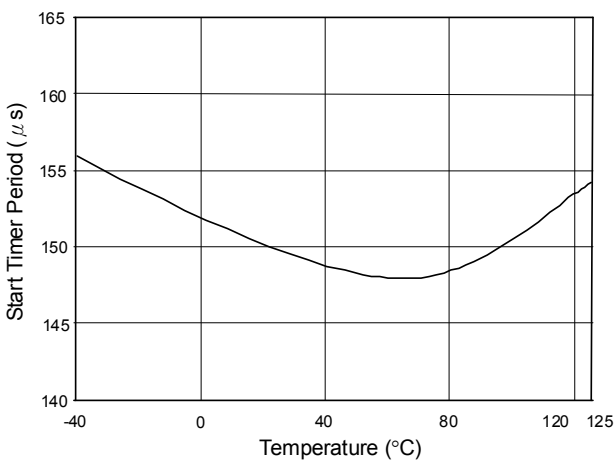


Fig. 11 Start Timer Period vs. Temperature

## Application Information

### Operation Overview

The LD7591 is an excellent voltage mode PFC controller. It meets the IEC61000-3-2 requirement and is intended for the use in those pre-regulator that demand low power harmonics distortion. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

### Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7591 PFC controllers and further to drive the power MOSFET. As shown in Fig. 12, a hysteresis is built in to prevent the shutdown from the voltage dip during start up. The turn-on and turn-off threshold level are set at 12.0V and 8.5V, respectively.

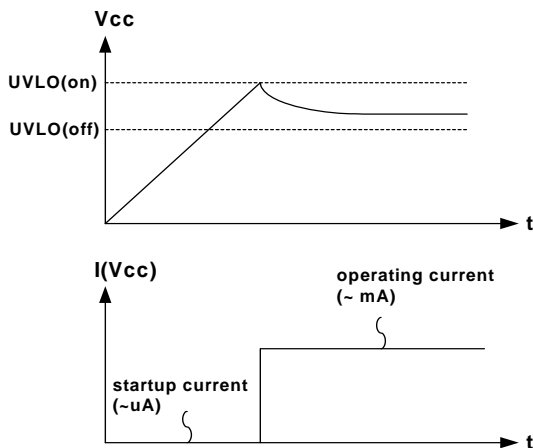


Fig. 12

### Startup Current and Startup Circuit

The typical startup circuit to generate the LD7591 Vcc is shown in Fig. 13. During the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse produced from LD7591 to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the

Vcc voltage is high enough to turn on the LD7591 and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the PFC choke. Lower startup current requirement on the PFC controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7591 is only 30μA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

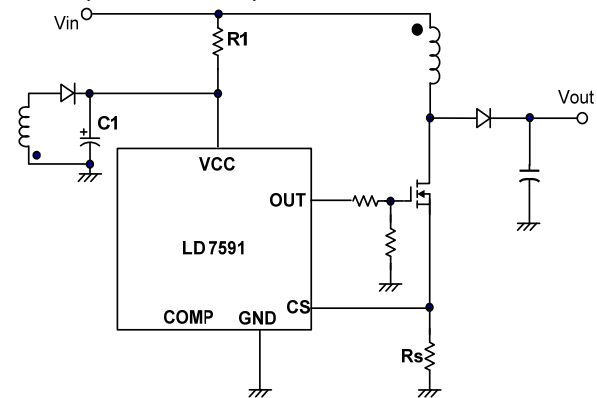


Fig. 13

### Output Voltage Setting

The LD7591 monitors the output voltage signal at INV pin through a resistor divider pair Ra and Rb. A transconductance amplifier is used instead of the conventional voltage amplifier. The transconductance amplifier (voltage controlled current source) aids the implementation of OVP and disables function. The output current of the amplifier changes according to the voltage difference of the inverting and non-inverting input of the amplifier. The output voltage of the amplifier is compared with the internal ramp signal to generate the turn-off signal. The output voltage is determined by the following relationship.

$$V_{OUT} = 2.5V(1 + \frac{R_a}{R_b})$$

Where  $R_a$  and  $R_b$  are top and bottom feedback resistor values (as shown in the Fig. 14).

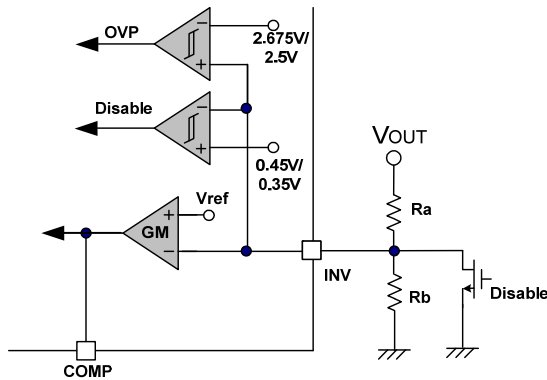


Fig. 14

### OVP and Disable on INV pin

To prevent the over voltage on the output capacitor from the fault condition, LD7591 is implemented with an OVP function on INV pin. Whenever the INV voltage is higher than the OVP threshold voltage 2.675V, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the INV pin down to 2.5V. The OVP function in LD7591 is an auto-recovery type protection. The Fig. 15 shows its operation. On the other hand, if the OVP condition is removed, the Vcc level will get back to normal level and the output will automatically return to the normal operation.

The disable comparator disables the operation of the LD7591 when the voltage of the inverting input is lower than 0.35V and there is 100mV hysteresis. An external small signal MOSFET can be used to disable the IC, referring to Fig. 14. The IC operating current decreases below 65 $\mu$ A to reduce power consumption if the IC is disabled.

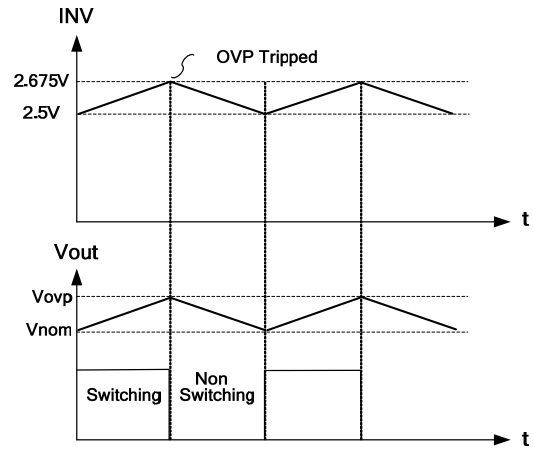


Fig. 15

### Zero Current Detection (ZCD)

Fig. 16 shows typical ZCD-block. The Zero Current Detection block will switch on the external MOSFET as the current through the boost inductor drops to zero in using an auxiliary winding coupled with the inductor. This feature allows transition-mode operation. If the voltage of the ZCD pin goes higher than 0.2V, the ZCD comparator waits until the voltage rises above 0.1V. If the voltage goes below 0.1V, the zero current detector will turn on the MOSFET. The ZCD pin is protected internally by two clamps, 6.0V-high clamp and -0.7V-low clamp. The 150 $\mu$ s timer generates a MOSFET turn on signal if the driver output has been low for more than 150 $\mu$ s from the falling edge of the driver output.

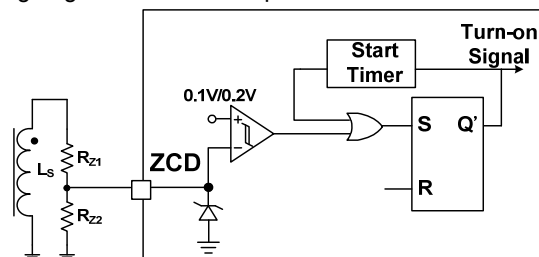


Fig. 16

Fig. 17 shows typical ZCD-related waveforms. Rz1 will produce some delay because of the capacitance carried by ZCD pin, it therefore delay the turn-on time accordingly. The switch will be turned on when the inductor current reaches zero; because of the structure of the ZCD delay, it will be turned on after some delay time. During this delay time, the stored charge of the COSS (MOSFET output capacitor) will be discharged through the path indicated in Fig. 18. This charge is transferred into a small filter capacitor C<sub>IN1</sub>, which is connected to the bridge diode. Therefore, there is no current flowing from the input side. That is, the input current I<sub>IN</sub> is zero during this period. In order to reduce the negative current flowing to the internal diode, a larger resistance of R<sub>Z1</sub> over 47kΩ is recommended.

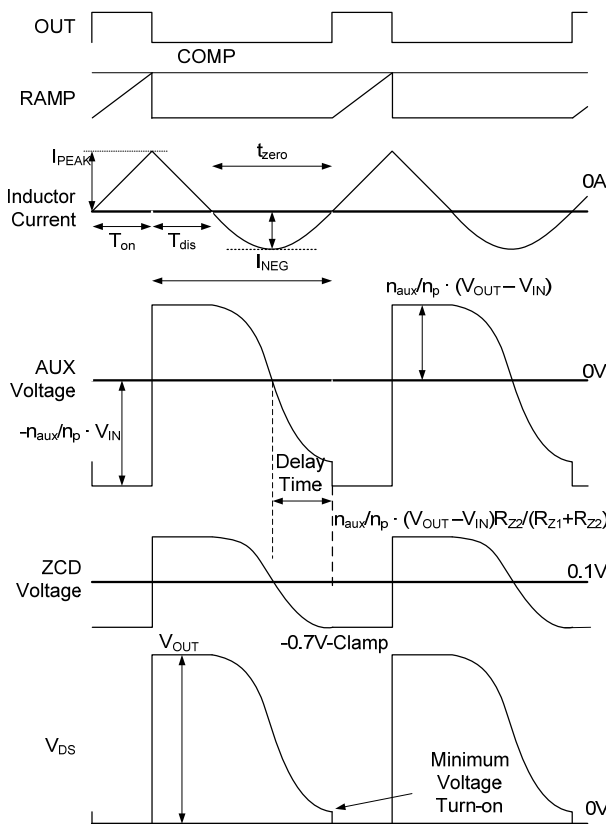


Fig. 17

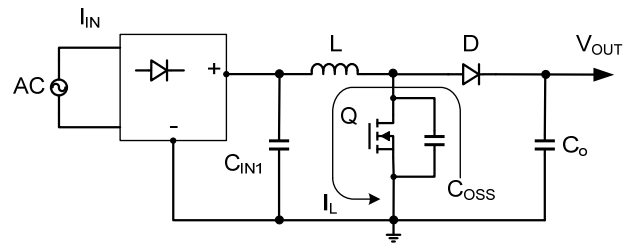


Fig. 18

## Ramp Generator Block

The output of the gm error amplifier and the output of the ramp generator block are compared to determine the MOSFET on time, as shown in Fig. 19. The slope of the ramp is determined by an external resistor connected to the RAMP pin. The voltage of the RAMP pin is 2.9V and the slope is proportional to the current flowing out of the RAMP pin. The internal ramp signal has a 1V offset; therefore, the drive output will be shut down if the voltage of the COMP pin is lower than 0.95V. The programmed on-time will be at its maximum when the COMP pin is open. The COMP pin open voltage is about 5.4~6.6V. According to the slope of the internal ramp, the maximum on-time can be programmed. The necessary maximum on-time will be achieved depending on the boost inductor, lowest AC line voltage, and maximum output power. The resistor value should be designed properly. The maximum on-time can be obtained from below

$$T_{ON-Time(MAX)} = \frac{R_{RAMP}}{1.58 \cdot 10^9}$$

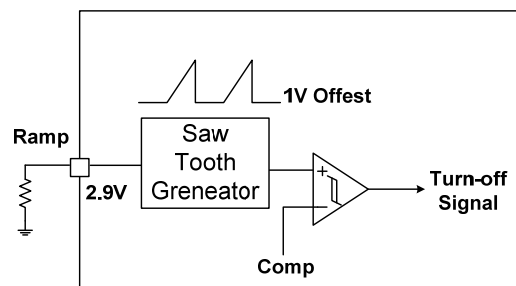


Fig. 19

## Output Drive Stage

An output stage of a CMOS buffer, with typical 800mA/-1200mA driving capability, is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

## Current Sensing and Leading-edge Blanking

The typical voltage mode of PFC controller feedbacks the voltage signals to close the control loop and achieve regulation. The LD7591 detects the primary MOSFET current from the CS pin, which is for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.8V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.8V}{R_S}$$

A 250ns leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. The R-C filter may be eliminated in some low power applications, such as the pulse width of the turn-on spikes is below 250ns and the negative spike on the CS pin is below -0.3V.

However, the pulse width of the turn-on spike is determined according to the output power, circuit design

and PCB layout. It is strongly recommended to adopt a smaller R-C filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

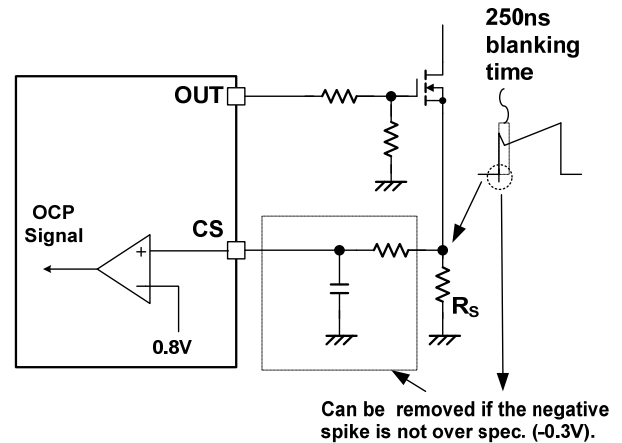


Fig. 20

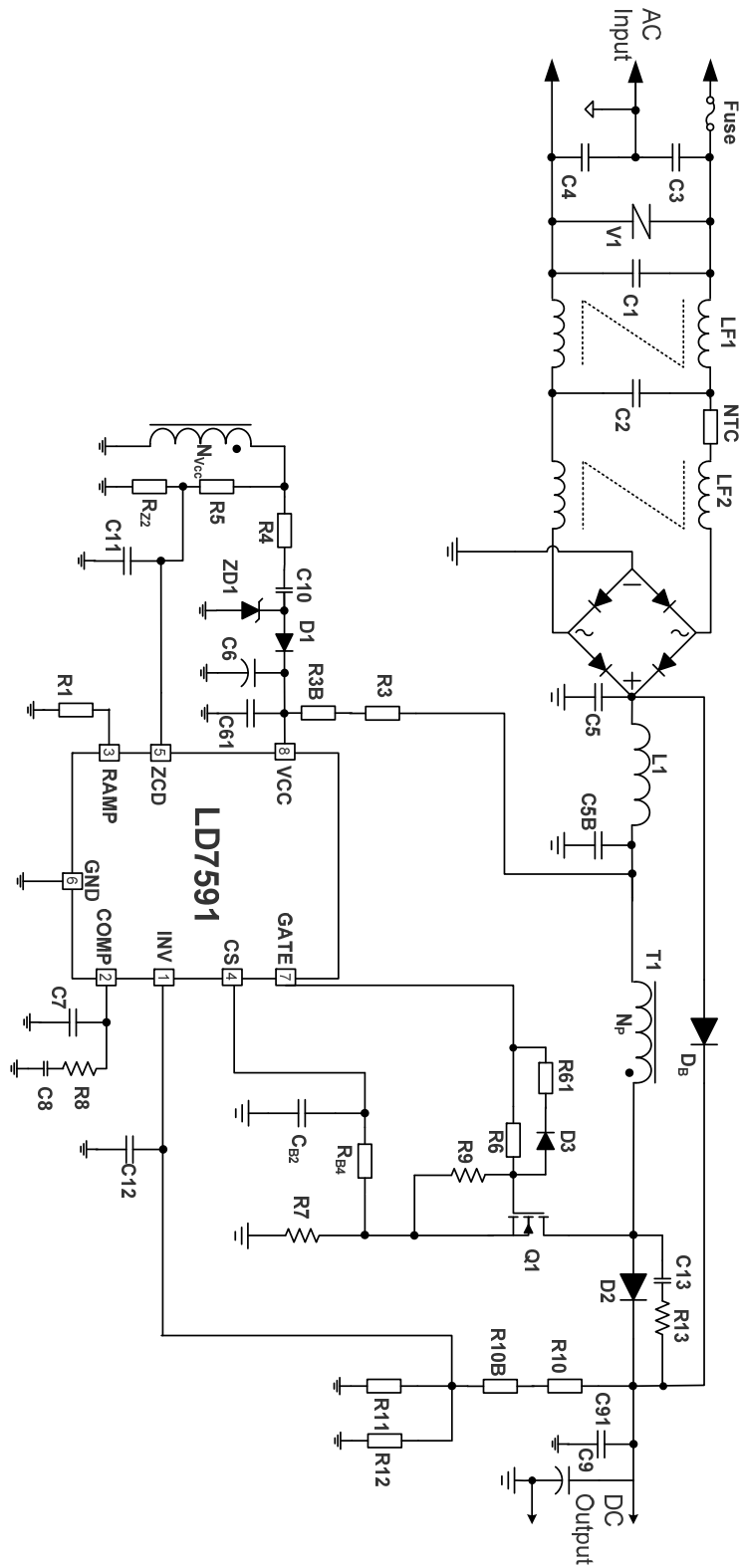
## Fault Protection

There are several critical protections integrated in the LD7591 to prevent the power supply or adapter from being damaged. Those damages usually come from open or short condition on the pins of LD7591.

Under the conditions listed below, the gate output will turn off immediately to protect the power circuit ---

1. Ramp pin short to ground
2. Ramp pin floating
3. CS pin floating

## Reference Application Circuit --- 400V/100W (90~264V<sub>AC</sub>)

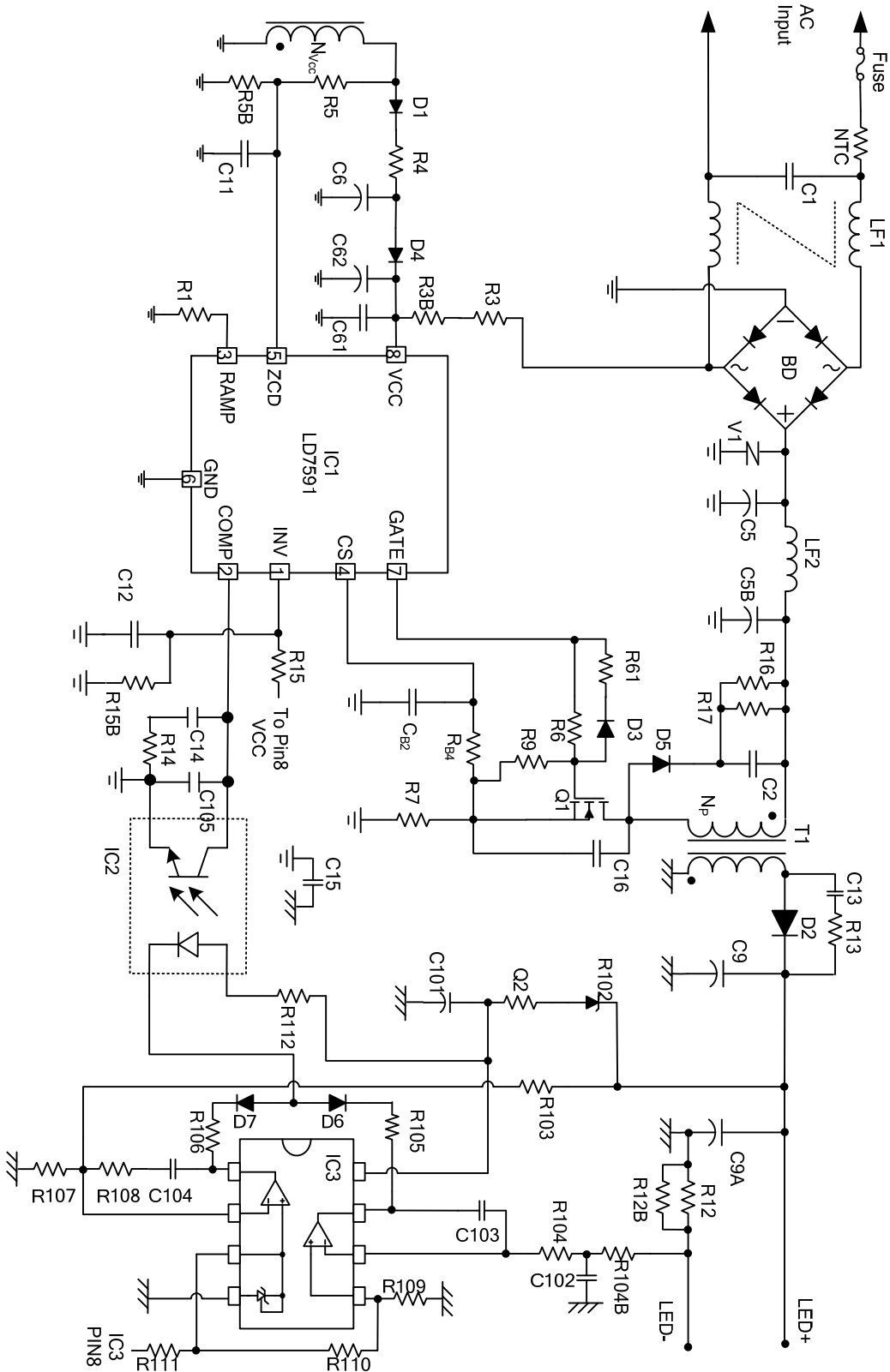


## BOM

P/N	Component Value	Note
Fuse	250V,T2A	
NTC	3A,5Ω	
R1	24 kΩ, 0805	
R2	620 kΩ, 0805	
R3	330 kΩ, 1206	
R3B	330 kΩ, 1206	
R4	270 Ω, 1206	
R5	110 kΩ, 0805	
R6	24 Ω, 0805	
R61	24 Ω, 0805	
R7	0.18 Ω	1/2W
R8	10 kΩ, 0805	
R9	22 kΩ, 1206	
R10	2 MΩ, 1206	
R10B	2 MΩ, 1206	
R11	27 kΩ, 0805	
R12	360 kΩ, 0805	
R13	1 MΩ, 1206	
RZ2	11 kΩ, 0805	
RZ3	0 Ω, 0805	
RB4	200 Ω, 0805	
RZ3	0 Ω, 0805	
RB4	200 Ω, 0805	

P/N	Component Value	Note
C1	0.1μF,X-cap	
C2	0.22μF,X-cap	
C3	2200pF,Y1-cap	
C4	2200pF,Y1-cap	
CY1	NC	
C5	0.47μF,400V	MPF
C5B	0.47μF,400V	MPF
C6	33μF, 50V	Electrolytic Capacitor
C61	100nF, 25V ,0805	
C7	100nF, 50V, 0805	
C8	220nF, 25V, 0805	
C9	100μF, 450V	Electrolytic Capacitor
C91	1000pF, 1kV, 1206	
C10	10nF, 100V, 1206	
C11	NC	
C12	100pF/ 16V, 0805	
C13	330pF/ 1kV/1206	
C14	100pF/ 1kV/1206	
CB2	100pF/16V, 0805	
D1	LL4148	SOD-80
D2	ER206	600V/ 2A, DO-15
D3	LL4148	SOD-80
DB	UF206G	600V/2A, DO-15
ZD1	GLZ18C, 18V Zener	SOD-80
BD	SBU4J or GBU4J	600V/4A
L1	Leadtrend's Design	220uH
LF1	Leadtrend's Design	
LF2	Leadtrend's Design	
Q1	FQP13N50C	500V, 13A, TO-220
IC1	LD7591	SOP-8
V1	NC	Varistor
T1	400uH	EI30, 44/6

## Reference Application Circuit --- LED -42V/350mA (90~264V<sub>AC</sub>)





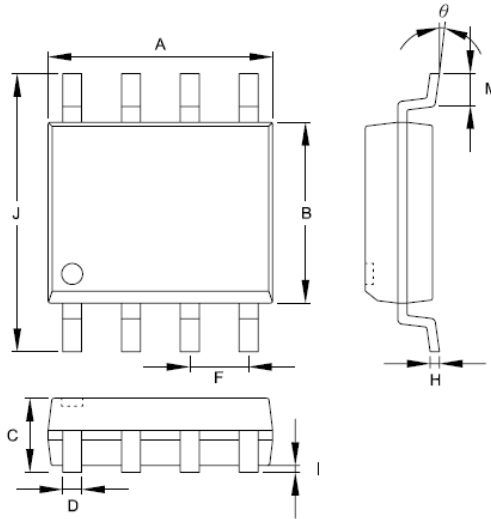
## BOM

P/N	Component Value	Note
Fuse	2A/250V	
NTC	0Ω, 1206	
V1	Varistor	471
R1	27kΩ, 0805	
R2	300kΩ, 0805	
R3	110kΩ, 1206	
R3B	110kΩ, 1206	
R4	39Ω, 1206	
R5	100kΩ, 0805	
R5B	10kΩ, 0805	
R6	51Ω, 0805	
R61	0Ω, 0805	
R7	0.75Ω	1/2W
R9	20kΩ, 0805	
R12	0.68Ω,	2W
R12B	NC,1206	
R13	100Ω, 1206	
R14	1kΩ, 0805	
R15	7.5MEGΩ, 0805	
R15B	620kΩ, 0805	
R16	100kΩ, 1206	
R17	100kΩ, 1206	
RB4	200Ω, 0805	
R101	NC, 0805	
R102	8.2V Zener	
R103	91k	
R104	0Ω, 0805	
R104B	10kΩ, 0805	
R105	20kΩ, 0805	
R106	75kΩ, 0805	
R107	5.6kΩ, 0805	
R108	39kΩ, 0805	
R109	10kΩ, 0805	
R110	100kΩ, 0805	
R111	15kΩ	
R112	4.7kΩ, 0805	
R113	NC, 0805	
R114	0Ω, 0805	
IC1	LD7591	SOP-8
IC2	PC817	
IC3		

P/N	Component Value	Note
C1	0.1μF / 275VAC	X-cap
C2	4.7nF/1kV,1206	
C5	0.047μF / 400V	MPF 塑膠電容
C5B	0.1μF / 400V	MPF 塑膠電容
C6	22uF/ 50V	Electrolytic Capacitor
C61	104pF/25V/0805	
C62	33uF/ 50V	
C9	330μF, 50V	Electrolytic Capacitor
C9A	330μF, 50V	Electrolytic Capacitor
C11	NC, 0805	
C12	10pF, 0805	
C13	470pF/500V, 1206	
C14	0.47μF/ 16V, 0805	
C15	2200pF,	Y 電容
C16	NC /1kV,1206	
C101	2.2uF/ 50V	
C102	4.7μF/10V/0805	
C103	0.1μF/ 25V, 0805	
C104	1μF/ 25V, 0805	
C105	473pF/25V/0805	
CB2	220pF/16V, 0805	
D1	BAV103	
D2	ER502	200V/ 5A,
D3	LL4148	SOD-80
D4	LL4148	SOD-80
D5	1N4007	1000V/1A
D6	LL4148	SOD-80
D7	LL4148	SOD-80
DZ1	NC	
DZ2	NC	
DZ3	P6KE200A	DO-15
BD	D1106	600V/1A
T1	EF20, 1150uH	106/32/13
LF1	UU9.8	
LF2	1000uH	
Q1	FQPF5N60C	600V, 4.5A, TO-220
Q2	330R, 0805	

## Package Information

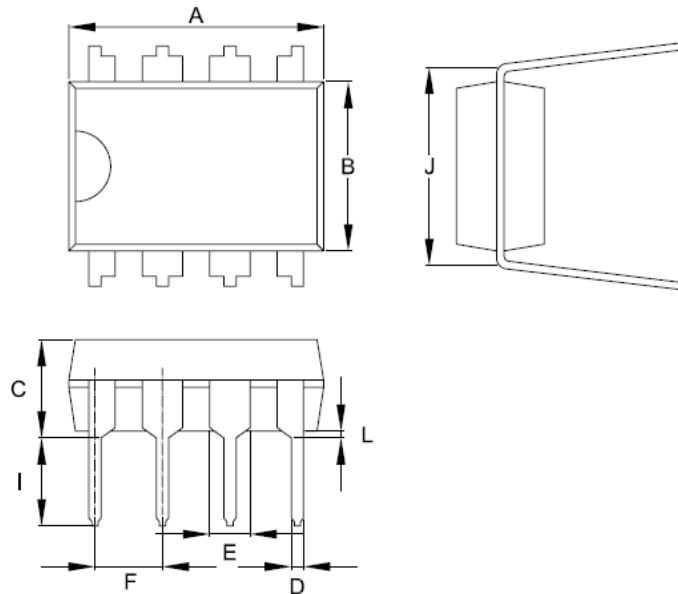
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

## Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	-----	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	-----	0.015	-----

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

**Revision History**

Rev.	Date	Change Notice
00	3/4/2010	Original Specification