LH2464

NMOS 256K (64K × 4) Dynamic RAM

FEATURES

- 65,536 × 4 bit organization
- Access times: 100/120/150 ns (MAX.)
- Cycle times: 200/220/260 ns (MIN.)
- Page mode, Read-Modify-Write operation
- Power supply: +5 V ± 10%
- Power consumption (MAX.):
  Operating: 523/457/413 mW (MAX.)
  Standby: 27.5 mW
- TTL compatible I/O
- Built-in gated $\overline{CAS}$ function
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh capability
- 256 refresh cycle (refreshing time 4 ms)
- Built-in high output substrate bias generator circuit
- Package:
  18-pin, 300-mil DIP

DESCRIPTION

The LH2464 is a 65,536 × 4 bit dynamic RAM fabricated using N-channel 2-layer polysilicon gate process technology. With multiplexed address inputs and a standard 18-pin DIP package, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH2464 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

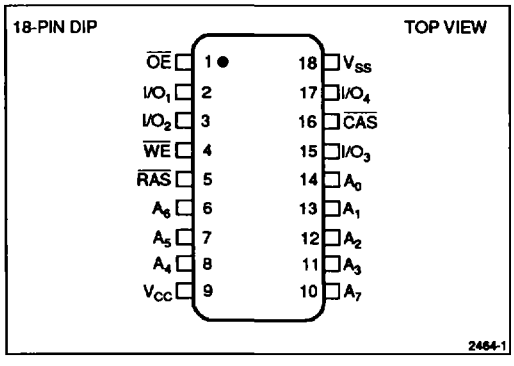

Figure 1. Pin Connections for DIP Package

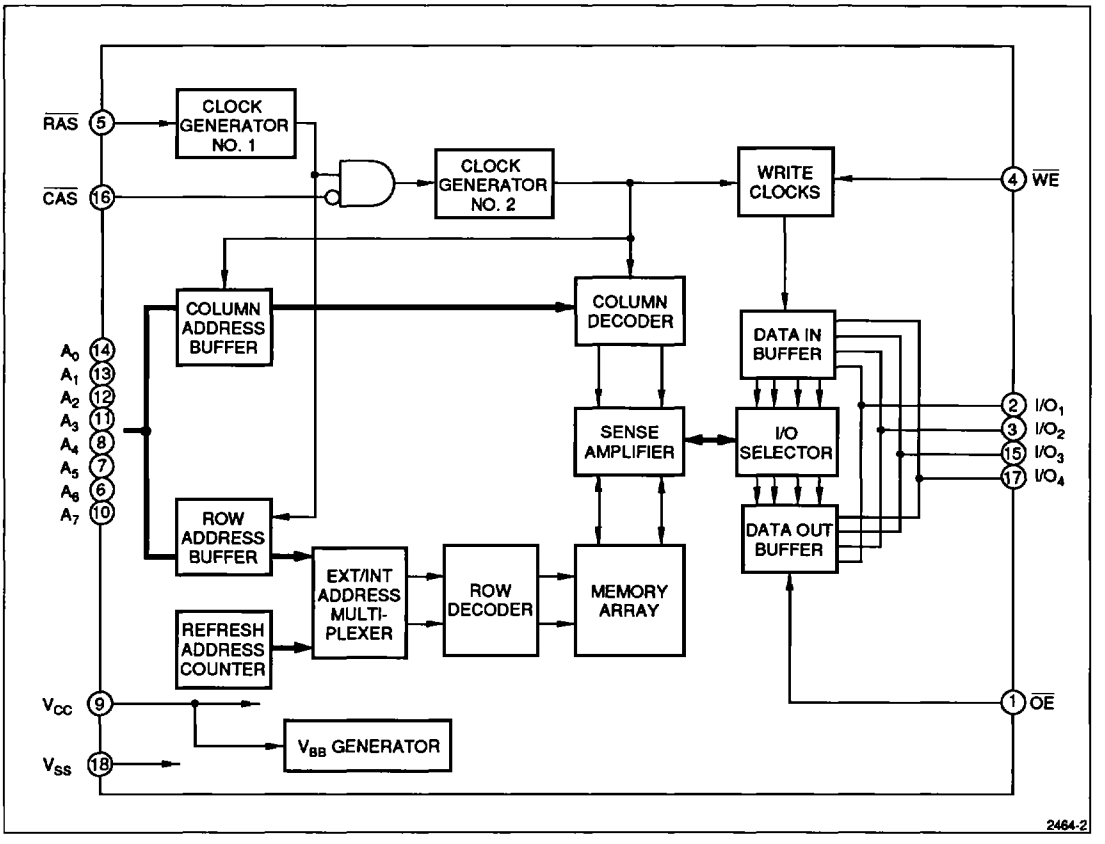

Figure 2. LH2464 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_7	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable

SIGNAL	PIN NAME
$\overline{OE}$	Output enable
I/O_1 - I/O_4	Data input/output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to +7.0	V	1
Output short-circuit current	I_O	50	mA	
Power consumption	P_D	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8		

NOTE:
1. Referenced to V_{SS}

CAPACITANCE (V_{CC} = 5 V ± 10%, T_A = 0 to 70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	A_0 - A_7	C_{IN1}			5	pF
	$\overline{OE}$, $\overline{WE}$	C_{IN2}			7	
	$\overline{RAS}$, $\overline{CAS}$	C_{IN2}			10	
Input/Output capacitance	I/O_1 - I/O_4	C_{IO}			8	pF

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

	PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
*	Average supply current in normal operation	LH2464-10	I_{CC1}	—	95	mA	1, 2
		LH2464-12		—	83		
		LH2464-15		—	75		
*	Average supply current in the standby mode		I_{CC2}	—	5.0	mA	1
	Average supply current in $\overline{RAS}$ only refresh time	LH2464-10	I_{CC3}	—	85	mA	1, 2
		LH2464-12		—	63		
		LH2464-15		—	65		
	Average supply current in page mode	LH2464-10	I_{CC4}	—	70	mA	1
		LH2464-12		—	60		
		LH2464-15		—	50		
	$\overline{CAS}$ before $\overline{RAS}$ average supply current in refresh cycle	LH2464-10	I_{CC5}	—	85	mA	1, 2
		LH2464-12		—	70		
		LH2464-15		—	65		
	Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other pins	I_{L1}	-10	10	µA	
	Output leakage current	0 V ≤ V_{OUT} ≤ 6.5 V Output in high-impedance state	I_{LO}	-10	10	µA	
	Output "High" voltage	I_{OUT} = -2 mA	V_{OH}	2.4	—	V	
	Output "Low" voltage	I_{OUT} = 4.2 mA	V_{OL}	—	0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on the cycle time.

AC CHARACTERISTICS [1, 2, 3] (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH2464-10		LH2464-12		LH2464-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read/write cycle time	t_{RC}	200	—	220	—	260	—	ns	
Read write cycle time	t_{RWC}	280	—	305	—	360	—	ns	
Page mode cycle time	t_{PC}	100	—	120	—	145	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	5, 6
Output turn off delay time	t_{OFF}	0	30	0	30	0	40	ns	
Rise and fall time	t_T	3	35	3	35	3	35	ns	3
$\overline{RAS}$ precharge time	t_{RP}	90	—	90	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	—	60	—	75	—	ns	
Refresh counter test cycle time	t_{RTC}	385		445		520		ns	12
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	285		335		410		ns	12
$\overline{CAS}$ precharge time	t_{CP}	40	—	50	—	60	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ setup time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	10	—	10	—	30	—	ns	
$\overline{RAS}$/$\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	30	75	ns	7, 8
$\overline{CAS}$/$\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	30	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	45	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	75	—	80	—	120	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time from $\overline{RAS}$	t_{RRH}	10	—	10	—	20	—	ns	10
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	9
Write command hold time	t_{WCH}	35	—	40	—	45	—	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	85	—	100	—	120	—	ns	
Write command pulse width	t_{WP}	35	—	40	—	45	—	ns	
Write command $\overline{RAS}$ lead time	t_{RWL}	35	—	40	—	45	—	ns	
Write command $\overline{CAS}$ lead time	t_{CWL}	35	—	40	—	45	—	ns	
$\overline{RAS}$ write command delay time	t_{RWD}	140	—	160	—	200	—	ns	
$\overline{CAS}$ write command delay time	t_{CWD}	90	—	100	—	125	—	ns	
Data input setup time	t_{DS}	0	—	0	—	0	—	ns	
Data input hold time from $\overline{CAS}$	t_{DHC}	35	—	40	—	45	—	ns	
Data input hold time from $\overline{RAS}$	t_{DHR}	85	—	100	—	120	—	ns	
Refresh interval	t_{REF}	—	4	—	4	—	4	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{OE}$ command hold time	t_{OEH}	25	—	25	—	40	—	ns	11
$\overline{OE}$ access time	t_{OEA}	—	25	—	30	—	40	ns	
$\overline{OE}$ to data delay	t_{OED}	30	—	30	—	40	—	ns	
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	30	0	30	0	40	ns	
Data input hold time from $\overline{WE}$	t_{DHW}	35	—	40	—	45	—	ns	

NOTES:

1. For proper operation, at least 500 µs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
2. AC characteristic assume t_T = 5 ns. (t_T refers to the transition time between V_{IH} and V_{IL}.)
3. Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
4. Only when $t_{RCD} \leq t_{RCD}$ (MAX.). If $t_{RCD} > t_{RCD}$ (MAX.), t_{RAC} will increase by (t_{RCD} - t_{RCD} (MAX.)).
5. When $t_{RCD} \geq t_{RCD}$ (MAX.).
6. Load condition for 2TTL + 100 pF.
7. t_{RCD} (MAX.) is the max. point fo. t_{RCD} where t_{RAC} (MAX.) is ensured, and doesn't represent a limit of operation. If t_{RCD} (MAX.) ≤ t_{RCD}, the access time will come under the control of t_{CAC}.
8. t_{RCD} (MIN.) = t_{RAH} (MIN.) + 2t_T + t_{ASC} (MIN.).
9. When $t_{WCS} \geq t_{WCS}$ (MIN.), it comes into early write cycle.
10. The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.
11. Only when $t_{WCS} < t_{WCS}$ (MIN.), it must be satisfied.
12. Only when in $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle.

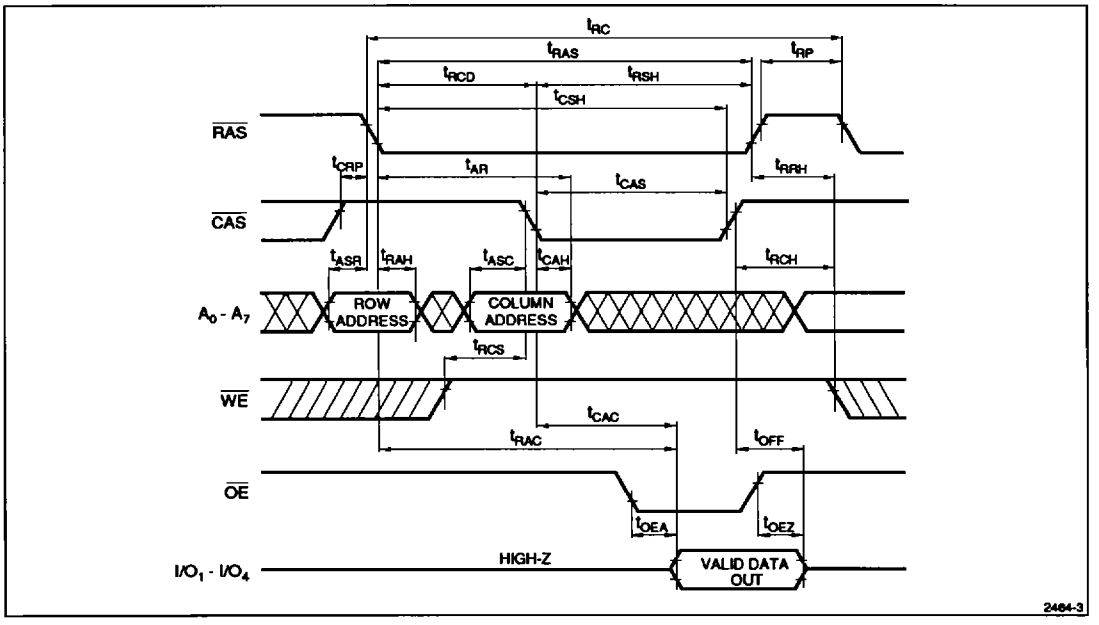

Figure 3. Read Cycle

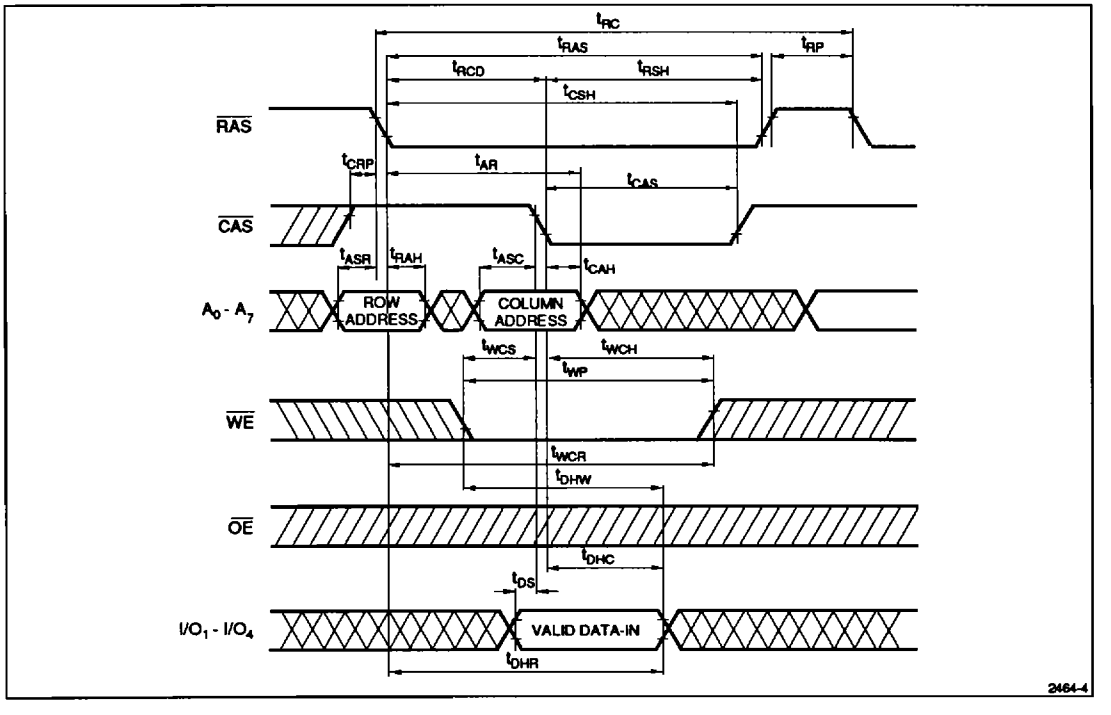

Figure 4. Write Cycle (Early Write)

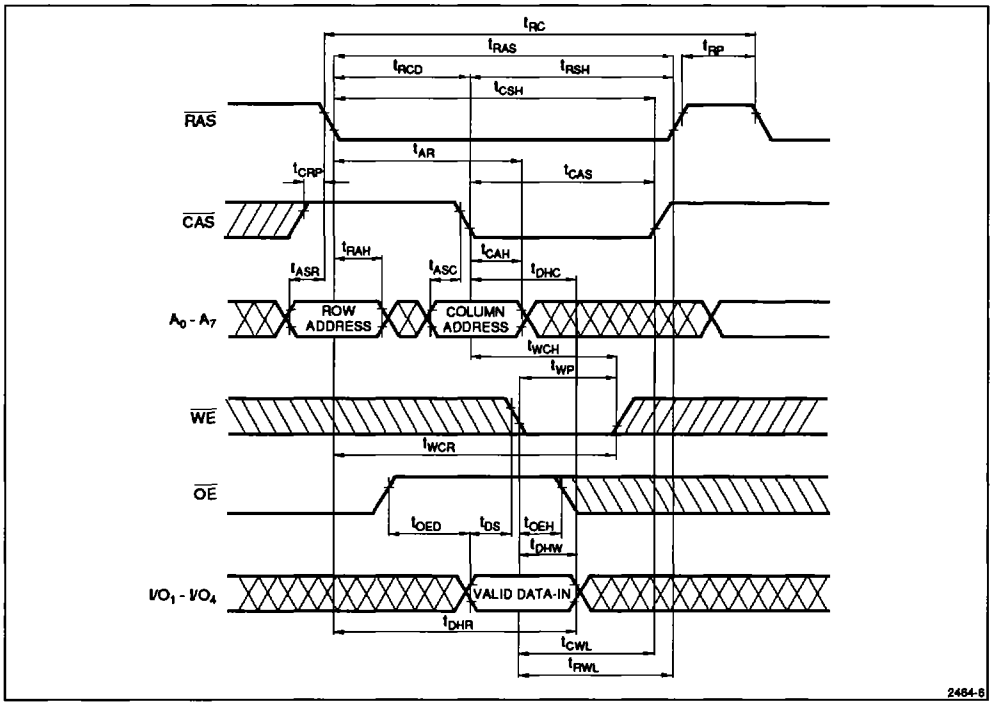

Figure 5. Write Cycle ($\overline{OE}$ Controlled Write)

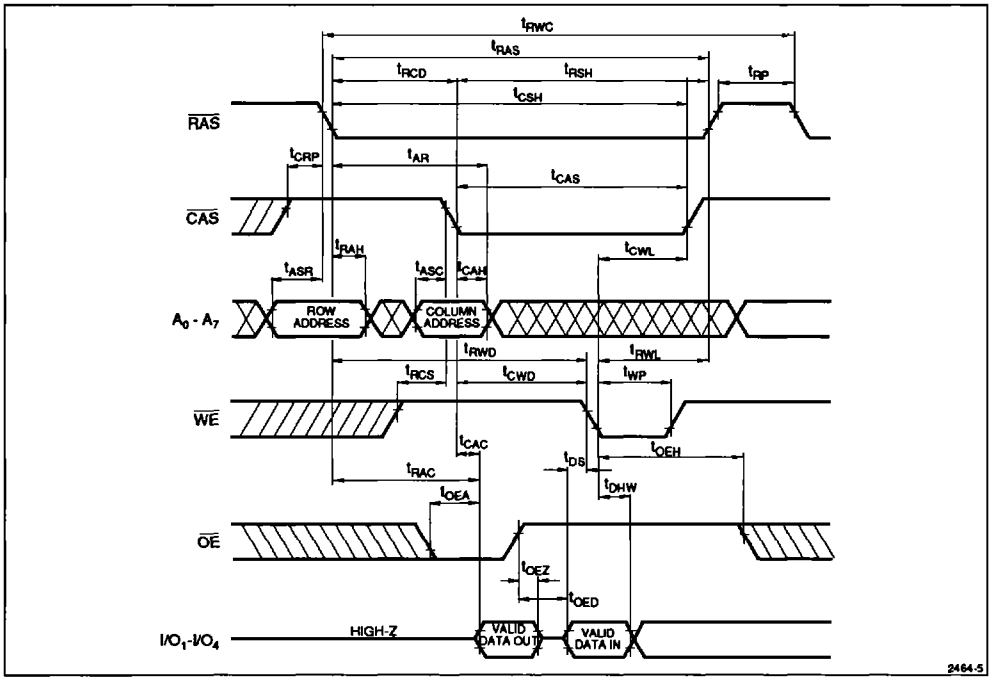

Figure 6. Read-Write/Read-Modify-Write Cycle

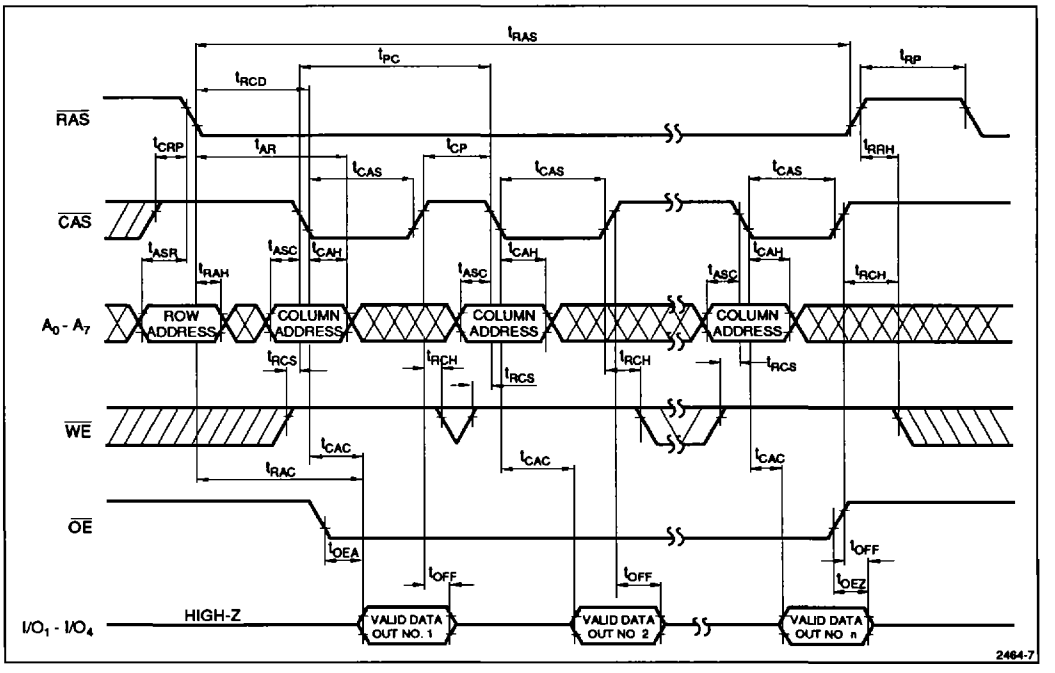

Figure 7. Page Mode Read Cycle

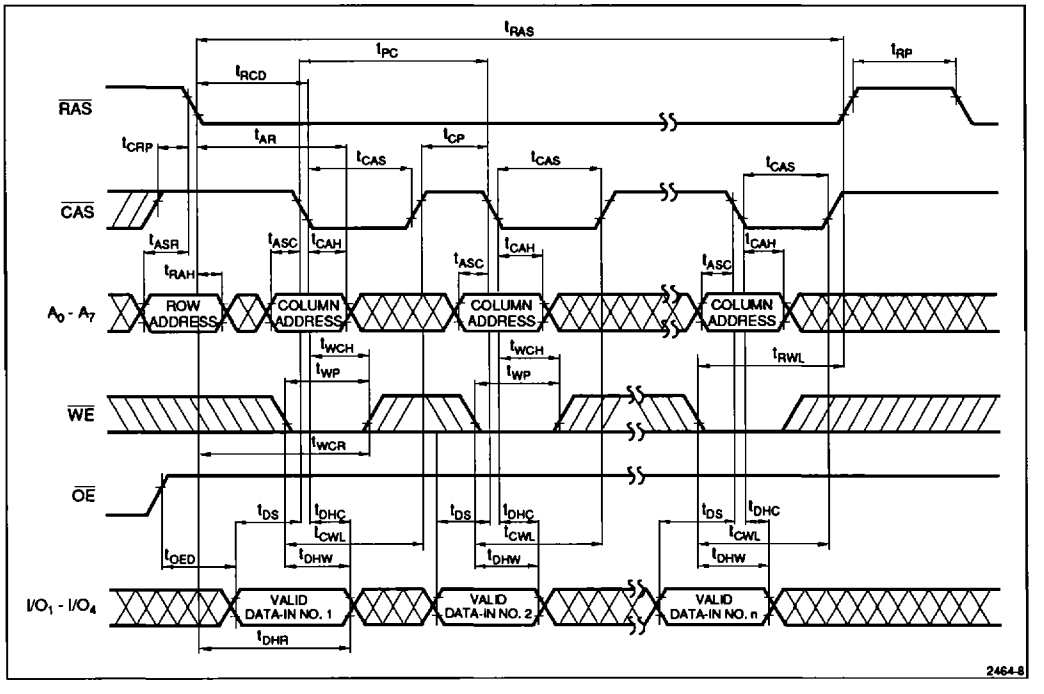

Figure 8. Page Mode Write Cycle

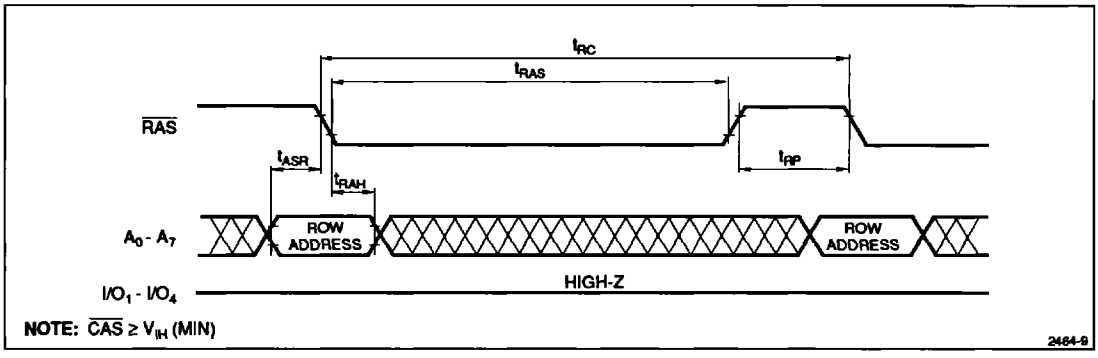

Figure 9. $\overline{RAS}$ Only Refresh Cycle

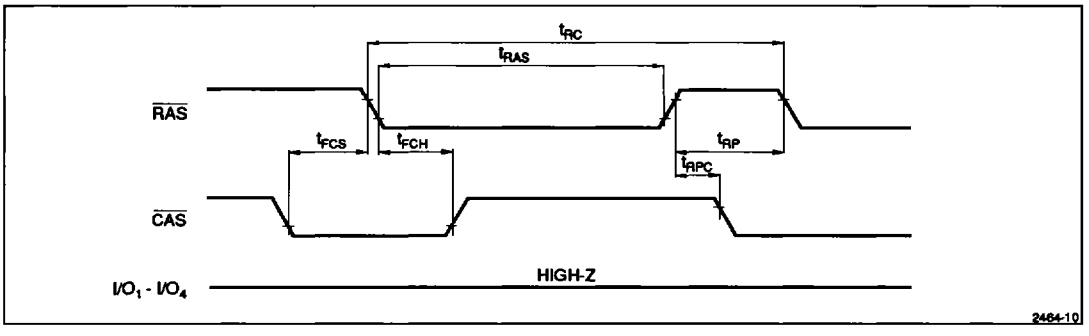

Figure 10. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

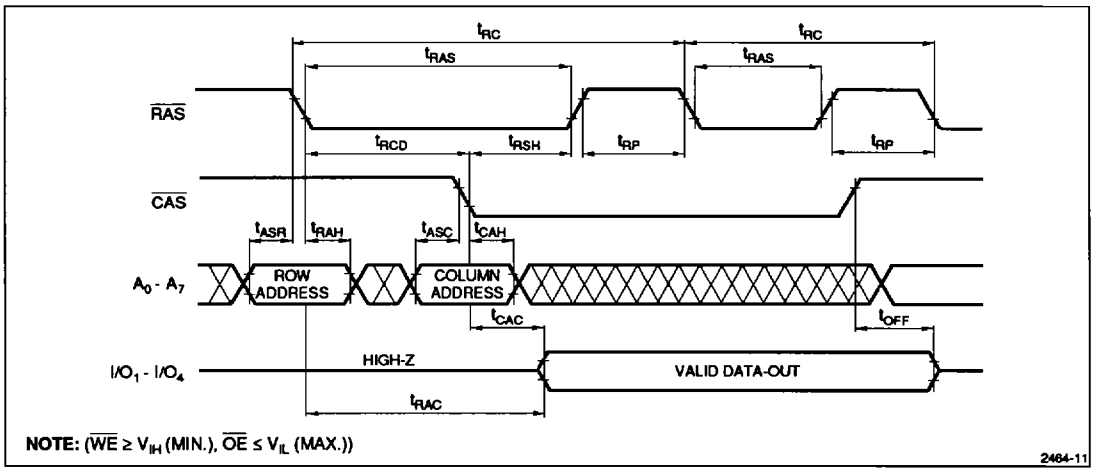

Figure 11. Hidden Refresh Cycle

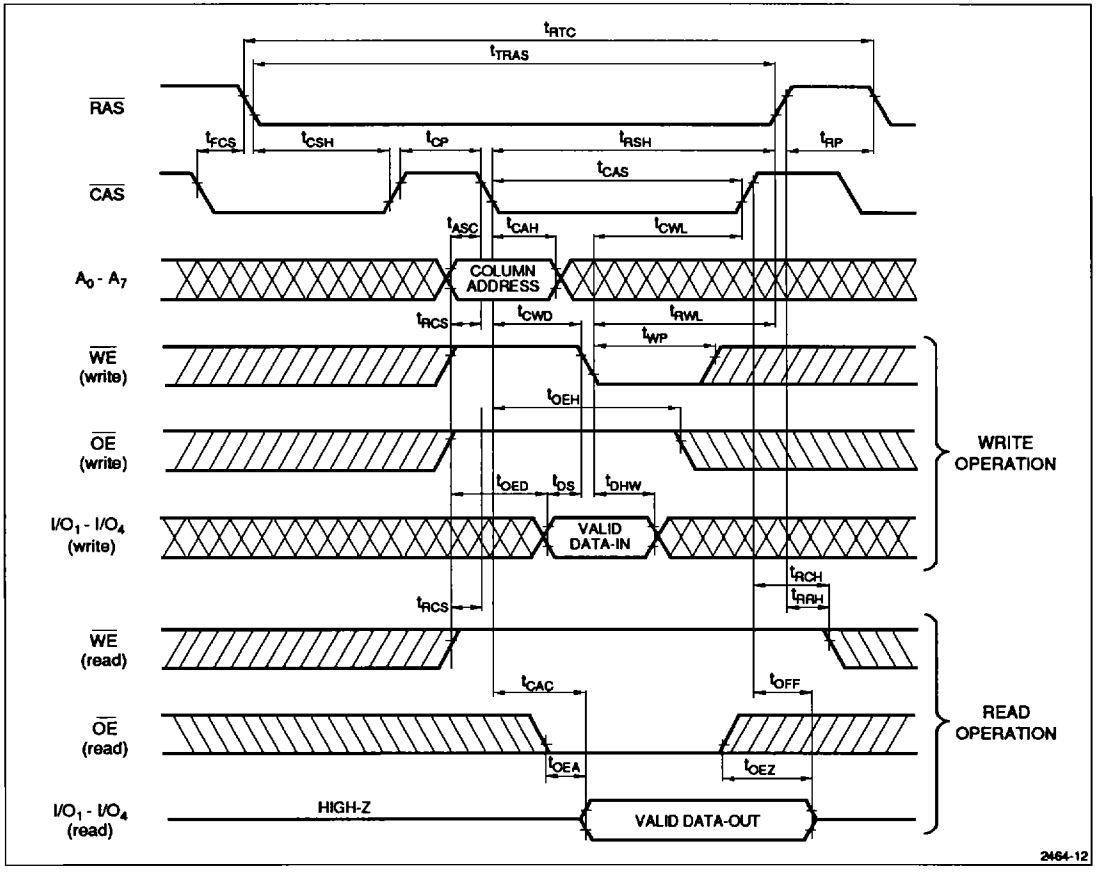

Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle is used to verify the operation of the internal refresh counter. The verification can be done by following the steps as described below.

1. Write "0" into 256 row addresses on a particular column address, which are selected by the internal refresh counter, by the write operation of the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle mode with any given column address.

2. Read and verify "0" of the 256 row addresses on the same column in regular read mode by externally supplying address signals.

Then, write "1" into the above 256 row addresses in regular write mode.

3. Read and verify "1" of the 256 row addresses in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle mode.

Refer to timing chart (12) of the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle.

ORDERING INFORMATION