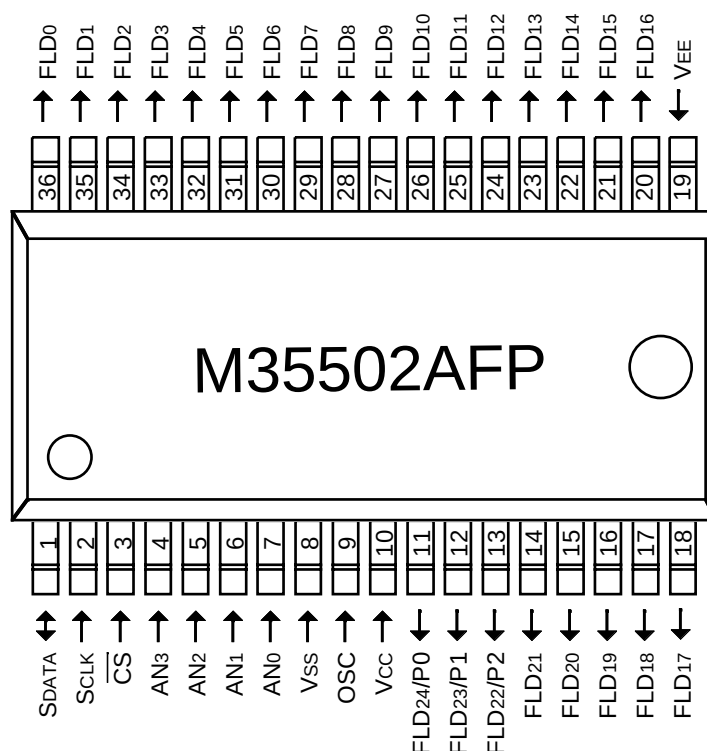


DESCRIPTION/FEATURES

- High-breakdown-voltage output port 25
 - Segment output 8 to 20
 - Digit output 5 to 16
(Ports P0 to P2 are also used as normal output ports)
 - Output breakdown $V_{CC} - 45\text{ V}$
 - Output current -18 mA (at DIG selecting),
 -7 mA (at SEG selecting)
 - Pull-down resistor built-in
 - Dimmer switch 4 levels
- A-D converter 8-bit X 4 channels
 - Absolute accuracy $\pm 3\text{ LSB}$
- Serial I/O 3 (CS controller, external clock)
 - Noise filter built-in
(in serial input pin and clock pin, 2 MHz sampling)
 - FLD display data input
 - A-D conversion data output
 - Command input
- Package 36P2R-G
- Oscillation circuit CR oscillation circuit (external capacitor)
 - Oscillation frequency 2 MHz
- Power source voltage 4.0 to 5.5 V

PIN CONFIGURATION (TOP VIEW)



Package type: 36P2R-G

Fig.1 Pin configuration of M35502AFP

FUNCTIONAL BLOCK

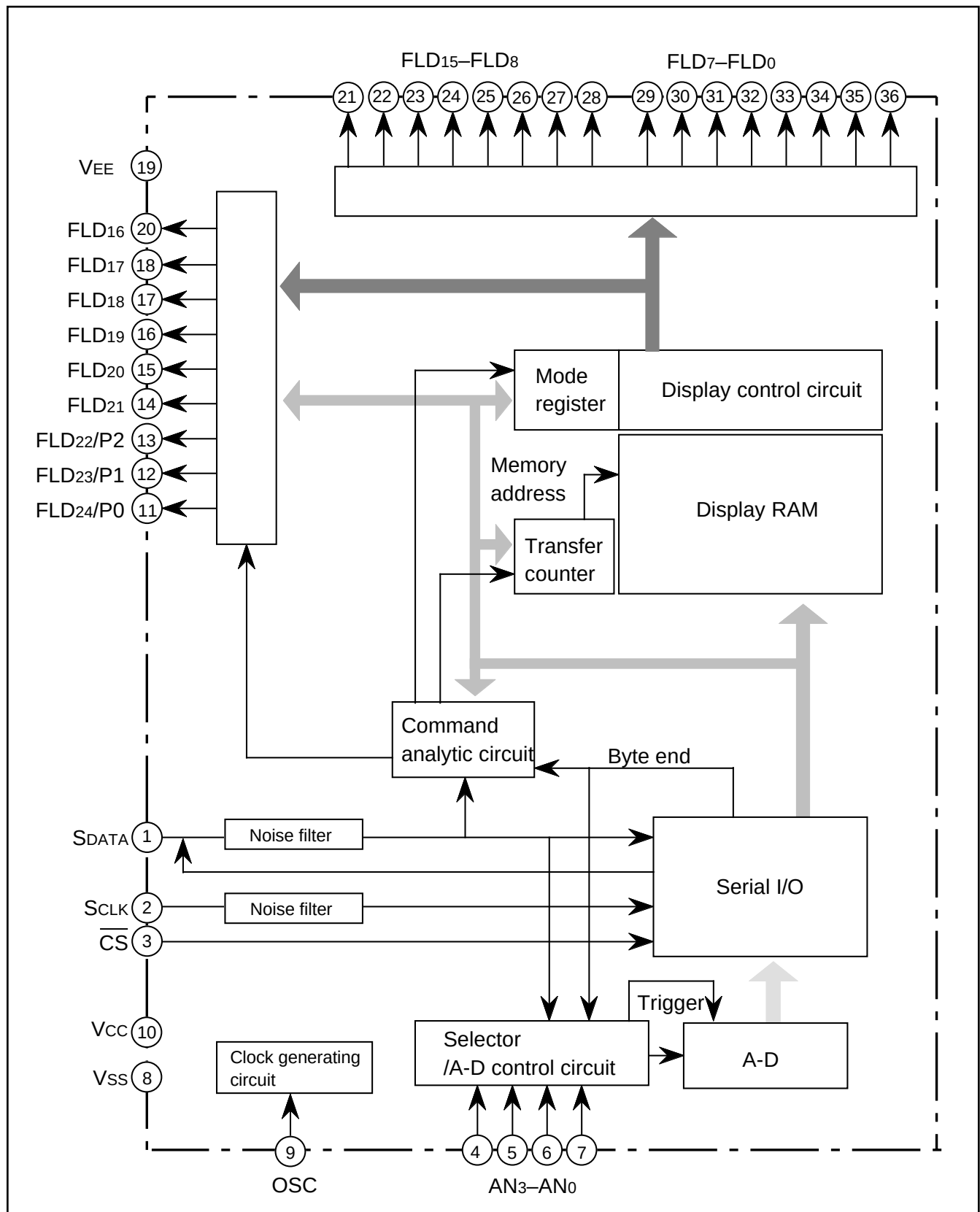


Fig.2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Input	Output	Function
VCC, VSS	Power source			• Apply voltage of 5 V to Vcc, and 0 V to Vss.
VEE	Pull-down power source			• Applies voltage supplied to pull-down resistors.
OSC	Clock input	Input		• Connect an external capacitor to this pin.
CS	Chip select	CMOS input		• Serial transfer is possible by inputting "L" signal. • Pull-up resistor is built in.
SCLK	Serial clock	CMOS input Noise filter		• Clock for serial transfer is input. • Read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
SDATA	Serial input/output	CMOS input Noise filter	N-channel open-drain	• Serial data is input/output. • In input mode, read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
FLD24/P0 – FLD22/P2	Digit/Port		P-channel open-drain	• Pin for ordinary output or digit output. • At reset this port is set to VEE level through a pull-down resistor.
FLD21– FLD0	Segment/Digit		P-channel open-drain	• Pin for digit output or segment output. • At reset this port is set to VEE level through a pull-down resistor.

PORT BLOCK

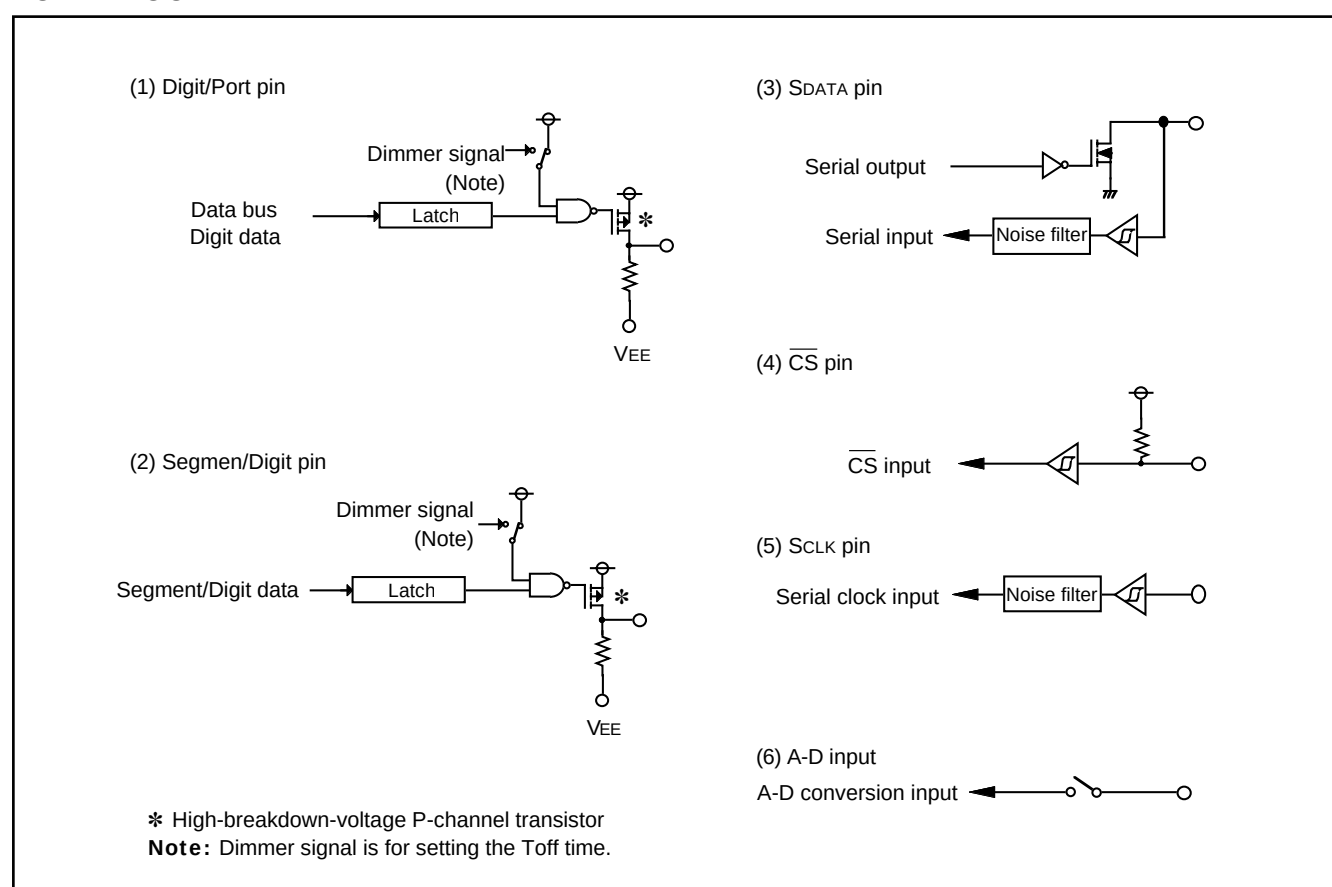


Fig.3 Port block diagram

COMMAND STYLE

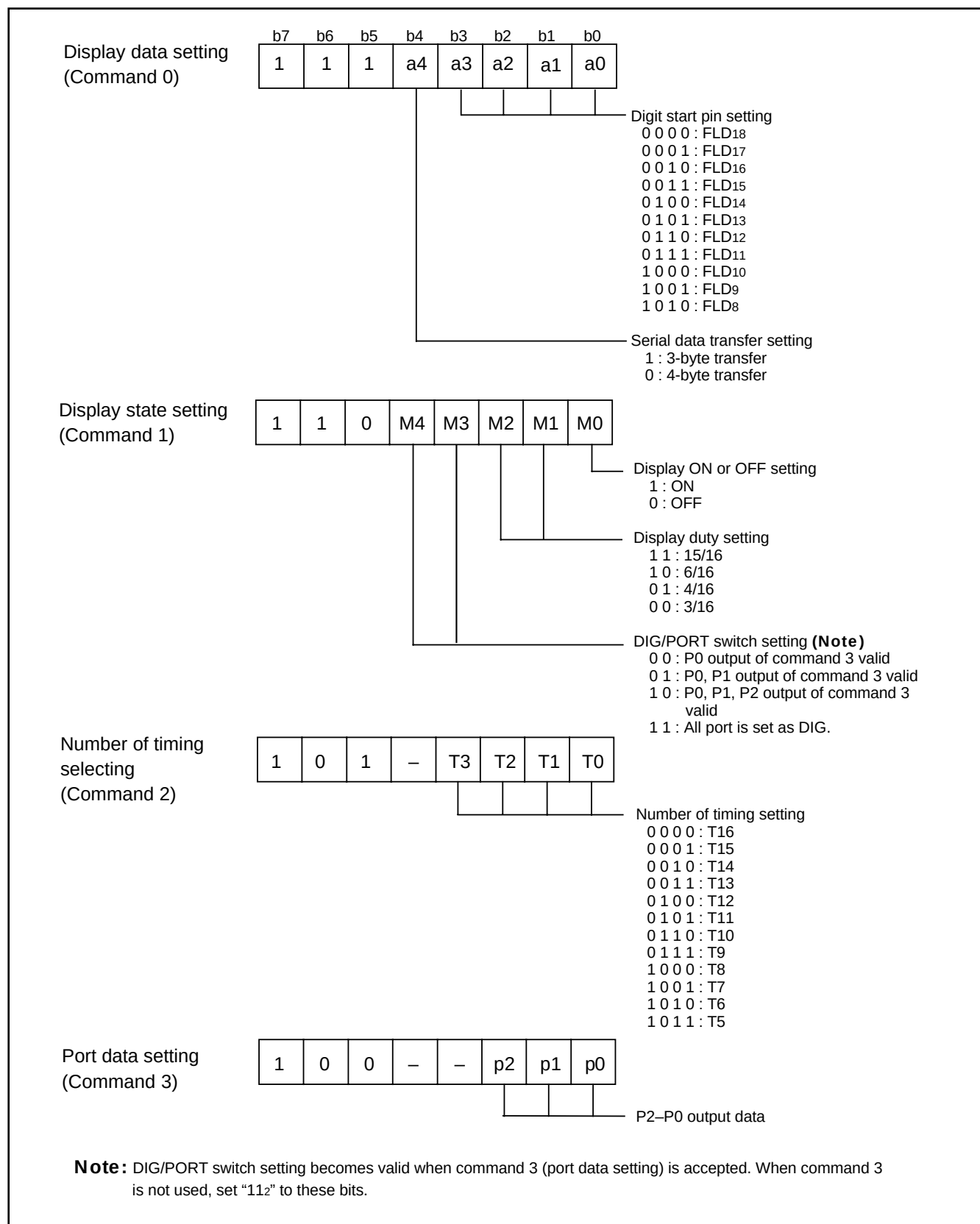


Fig.4 Command style

SERIAL I/O PROTOCOL

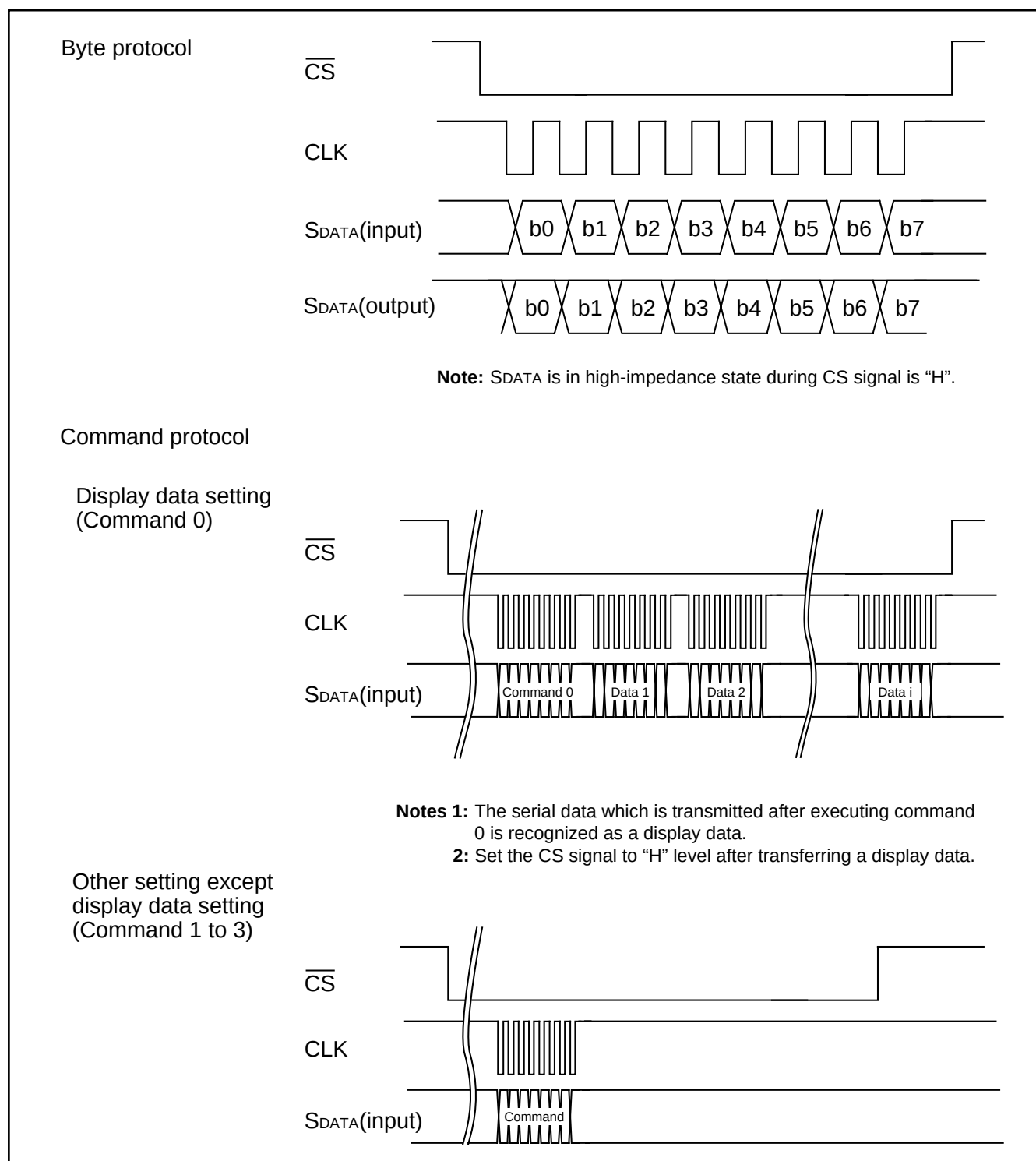
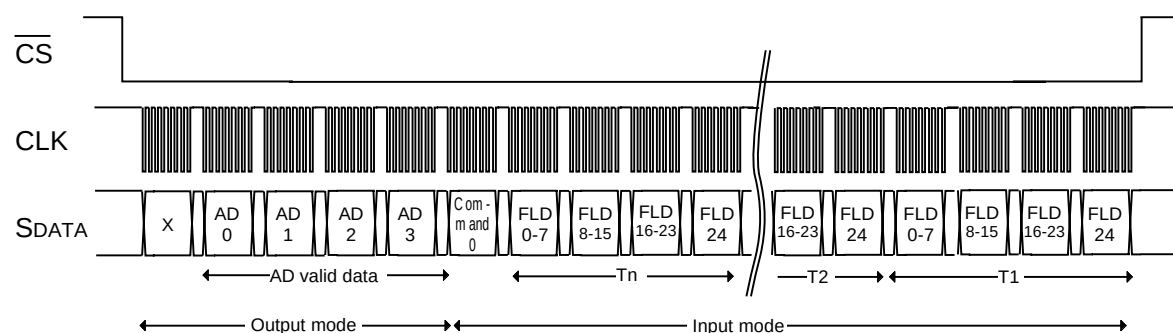


Fig.5 Serial I/O protocol

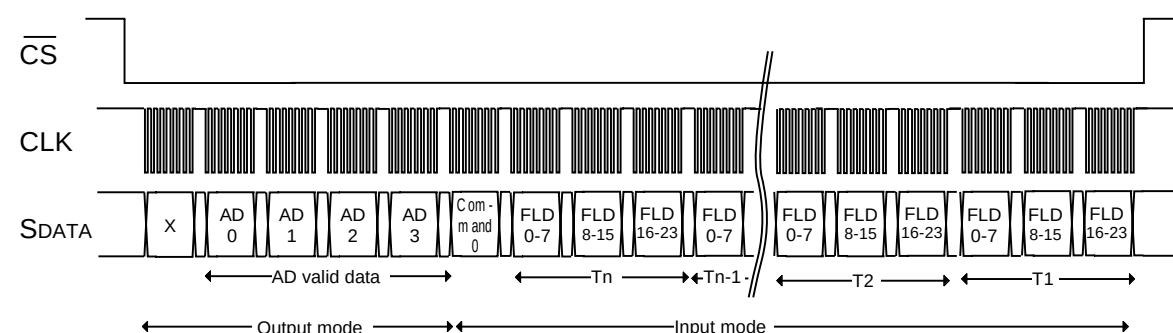
SERIAL COMMUNICATION FORMAT (DISPLAY DATA, A-D OUTPUT)

When using 25 high-breakdown-voltage ports (segment + grid) (4-byte transfer)



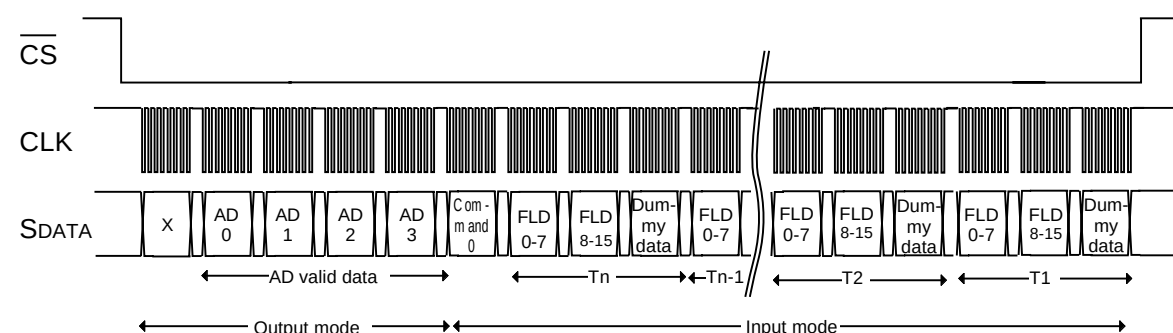
The SDATA pin becomes output mode from after the $\overline{CS}$ pin falling until the 5th byte of serial data.
The SDATA becomes command input mode from the 6th byte of serial data.

When using 24 high-breakdown-voltage ports (segment + grid) (3-byte transfer)



The SDATA pin becomes output mode from after the $\overline{CS}$ pin falling until the 5th byte of serial data.
The SDATA becomes command input mode from the 6th byte of serial data.

When using 16 high-breakdown-voltage ports (segment + grid) or less (3-byte transfer)



Transfer dummy data to the third byte of each timing.
The SDATA pin becomes output mode from after the $\overline{CS}$ pin falling until the 5th byte of serial data.
The SDATA becomes command input mode from the 6th byte of serial data.

Fig.6 Serial communication format

FLD DISPLAY TIMING

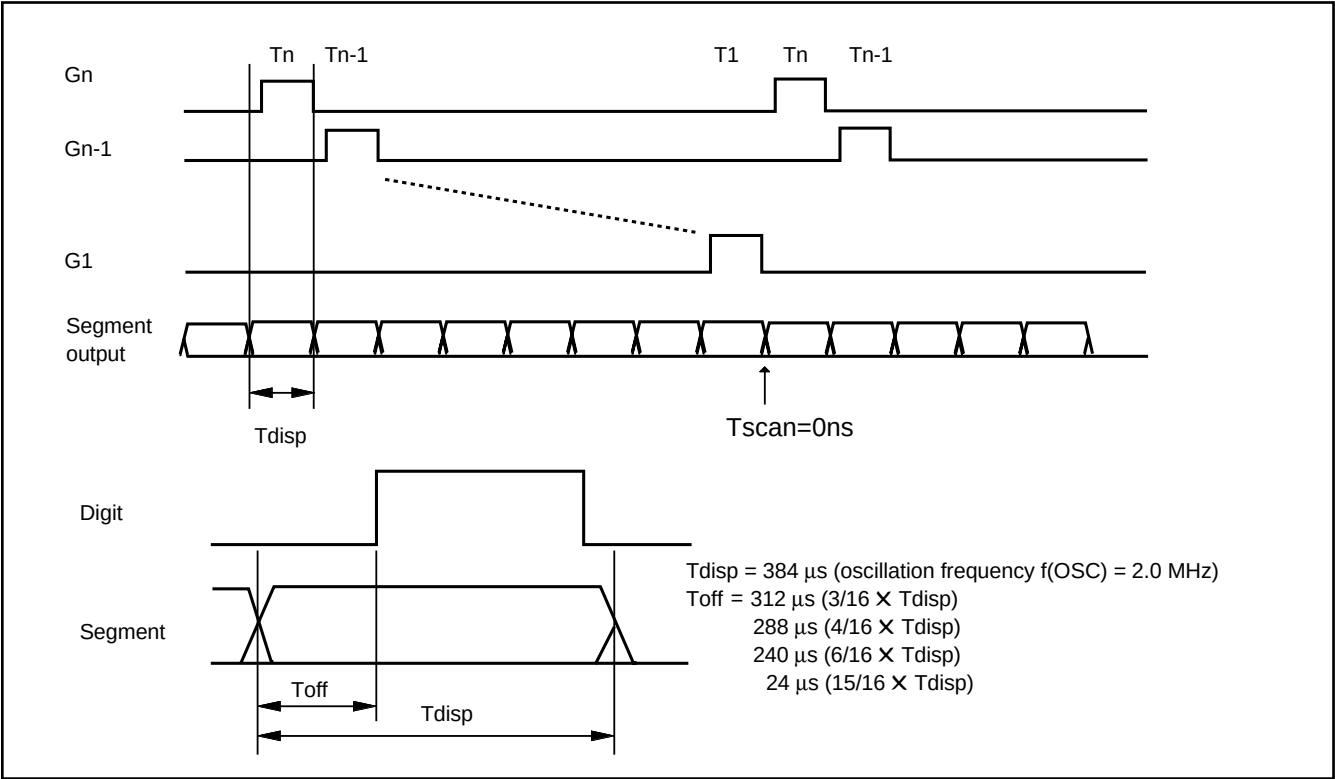


Fig.7 FLD display timing diagram

SEGMENT/DIGIT SETTING EXAMPLE

	PORT	FLD	Grid: 5 Segment: 8	Grid: 7 Segment: 8	Grid: 10 Segment: 8	Grid: 7 Segment: 18
1		FLD0	SEG1	SEG1	SEG1	SEG1
2		FLD1	SEG2	SEG2	SEG2	SEG2
3		FLD2	SEG3	SEG3	SEG3	SEG3
4		FLD3	SEG4	SEG4	SEG4	SEG4
5		FLD4	SEG5	SEG5	SEG5	SEG5
6		FLD5	SEG6	SEG6	SEG6	SEG6
7		FLD6	SEG7	SEG7	SEG7	SEG7
8		FLD7	SEG8	SEG8	SEG8	SEG8
9		FLD8	GRID5	GRID7	GRID10	SEG9
10		FLD9	GRID4	GRID6	GRID9	SEG10
11		FLD10	GRID3	GRID5	GRID8	SEG11
12		FLD11	GRID2	GRID4	GRID7	SEG12
13		FLD12	GRID1	GRID3	GRID6	SEG13
14		FLD13		GRID2	GRID5	SEG14
15		FLD14		GRID1	GRID4	SEG15
16		FLD15			GRID3	SEG16
17		FLD16			GRID2	SEG17
18		FLD17			GRID1	SEG18
19		FLD18				GRID7
20		FLD19				GRID6
21		FLD20				GRID5
22		FLD21				GRID4
23	P2	FLD22				GRID3
24	P1	FLD23				GRID2
25	P0	FLD24				GRID1

Fig.8 Segment/Digit setting example

BIT ALLOCATION FOR DISPLAY RAM

ADDRESS	b7	b6	b5	b4	b3	b2	b1	b0		b7	b6	b5	b4	b3	b2	b1	b0	
00 ₁₆								FLD 24	T1	20 ₁₆							FLD 24	T9
01 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		21 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16
02 ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8		22 ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8
03 ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0		23 ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0
04 ₁₆								FLD 24	T2	24 ₁₆							FLD 24	T10
05 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		25 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16
06 ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8		26 ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8
07 ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0		27 ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0
08 ₁₆								FLD 24	T3	28 ₁₆							FLD 24	T11
09 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		29 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16
0A ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8		2A ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8
0B ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0		2B ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0
0C ₁₆								FLD 24	T4	2C ₁₆							FLD 24	T12
0D ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		2D ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16
0E ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8		2E ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8
0F ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0		2F ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0
10 ₁₆								FLD 24	T5	30 ₁₆							FLD 24	T13
11 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		31 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16
12 ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8		32 ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8
13 ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0		33 ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0
14 ₁₆								FLD 24	T6	34 ₁₆							FLD 24	T14
15 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		35 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16
16 ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8		36 ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8
17 ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0		37 ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0
18 ₁₆								FLD 24	T7	38 ₁₆							FLD 24	T15
19 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		39 ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16
1A ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8		3A ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8
1B ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0		3B ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0
1C ₁₆								FLD 24	T8	3C ₁₆							FLD 24	T16
1D ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16		3D ₁₆	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16
1E ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8		3E ₁₆	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8
1F ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0		3F ₁₆	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0

Fig.9 Bit allocation for display RAM

CLOCK GENERATING CIRCUIT

Oscillating circuit is built up by connecting a capacitor between pins OSC and Vss.

When supplying a clock externally, input it to the OSC pin.

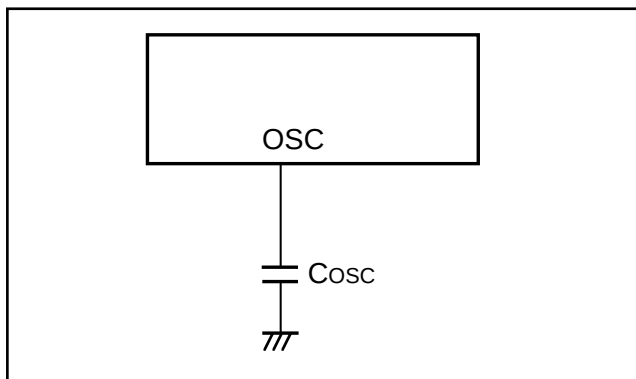


Fig.10 CR generating circuit

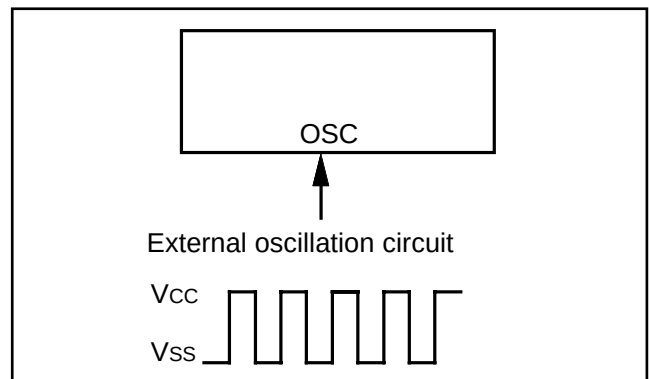


Fig.11 External clock input circuit

HANDLING OF UNUSED PINS

Handle unused pins as the follow.

Table 2 Handling of unused pins

Pin	Handling
Segment	Open
Digit	Open
Analog input	Connect to Vcc or Vss through a resistor.

POWER-ON RESET

Reset can be performed automatically during power on (power-on reset) by the built-in power-on reset circuit.

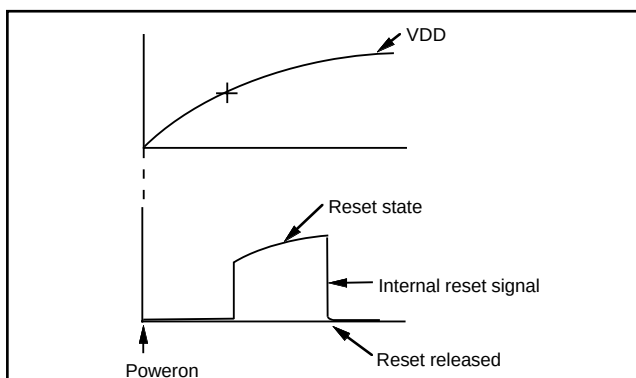


Fig.12 Power-on reset

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage	- All voltage are based on V_{SS}. - Output transistors are cut off.	−0.3 to 6.5	V
V _{EE}	Pull-down power source voltage		V _{CC} −45 to V _{CC} +0.3	V
V _I	Input voltage AN ₀ – AN ₃		−0.3 to V _{CC} +0.3	V
V _I	Input voltage CS, S _{DATA} , S _{CLK}		−0.3 to V _{CC} +0.3	V
V _O	Output voltage FLD ₀ – FLD ₂₄		V _{CC} −45 to V _{CC} +0.3	V
		- A waveform: 450 μs or more frequency and 30 μs or less pulse width. - Connect only capacitor load (C_L = 200pF).	V _{CC} −50 to V _{CC} +0.3	
V _O	Output voltage S _{DATA}	- All voltage are based on V_{SS}. - Output transistors are cut off.	−0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _a = 25 °C	600	mW
T _{opr}	Operating temperature		−20 to 85	°C
T _{stg}	Storage temperature		−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5 V, T_a = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Power source voltage	4.0	5.0	5.5	V
V _{SS}	Power source voltage		0		V
V _{EE}	Pull-down power source voltage	V _{CC} −38		V _{CC}	V
V _{IH}	“H” input voltage CS, S _{CLK} , S _{DATA}	0.75V _{CC}		V _{CC}	V
V _{IL}	“L” input voltage CS, S _{CLK} , S _{DATA}	0		0.25V _{CC}	V

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5 V, T_a = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣI _{OH} (peak)	“H” total peak output current FLD ₀ – FLD ₂₄ (Note 1)			−240	mA
ΣI _{OH} (avg)	“H” total average output current FLD ₀ – FLD ₂₄			−120	mA
I _{OH} (peak)	“H” peak output current FLD ₀ – FLD ₂₄ (at DIG selecting) (Note 2)			−40	mA
I _{OH} (peak)	“H” peak output current FLD ₀ – FLD ₂₄ (at SEG selecting) (Note 2)			−20	mA
I _{OL} (peak)	“L” peak output current S _{DATA}			10	mA
I _{OH} (avg)	“H” peak output current FLD ₀ – FLD ₂₄ (at DIG selecting) (Note 3)			−18	mA
I _{OH} (avg)	“H” average output current FLD ₀ – FLD ₂₄ (at SEG selecting) (Note 3)			−7	mA
I _{OL} (avg)	“L” average output current S _{DATA}			5.0	mA
f(OSC)	Clock input oscillation frequency (Note 4)	1.4	2.0	2.6	MHz
f(SCLK)	Serial I/O external clock frequency		250		kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the oscillation frequency has a 50 % duty cycle.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
VOH	“H” output voltage	DIG output	IOH = −18 mA	VCC−2.0			V
		SEG output	IOH = −7 mA	VCC−2.0			V
VOL	“L” output voltage	SDATA	IOL = 5 mA			2.0	V
VT+ — VT−	Hysteresis	SDATA, SCLK, CS	VCC = 5.0 V		0.5		V
IiH	“H” input current	SDATA, SCLK, CS	Vi = VCC			5.0	μA
IiL	“L” input current	SDATA, SCLK	Vi = VSS			−5.0	μA
		CS			−500		μA
		OSC			−4.0		μA
ILOAD	Output load current	FLD0 – FLD24	VEE = VCC−36 V VOL = VCC Output transistors “off”	250	500	750	μA
I _{LEAK}	Output leakage current	FLD0 – FLD24	VEE = VCC−38 V VOL = VCC−38 V Output transistors “off”			−10	μA

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VRAM	RAM hold voltage	When clock is stopped	2.0		5.5	V
ICC	Power source current	VCC = 5 V, f(XIN) = 2.0 MHz Output transistors “off” at A-D converter operating		1.5	2.5	mA

A-D CONVERTER CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)	VCC = 5.12 V			±3	LSB
Tconv	Conversion time				100	tc(OSC)
VIA	Analog input voltage		0		VCC	V
IiA	Analog port input current			0.5	5.0	μA
RLADDER	Ladder resistor			35		kΩ

TIMING REQUIREMENTS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _c (OSC)	Reset input "L" pulse width	384			ns
t _{wH} (OSC)	Clock input "H" pulse width	120			ns
t _{wL} (OSC)	Clock input "L" pulse width	120			ns
t _c (SCLK)	Serial clock input cycle time (Note)	5			CLKs
t _{wH} (SCLK)	Serial clock input "H" pulse width (Note)	2			CLKs
t _{wL} (SCLK)	Serial clock input "L" pulse width (Note)	3			CLKs
t _{su} (SDATA-SCLK)	Serial input setup time (Note)	2			CLKs
t _h (SCLK-SDATA)	Serial input hold time (Note)	3			CLKs
t _{su} (CS)	Serial input setup time	50 t _c (OSC)			ns
t _h (CS)	Serial input hold time	50 t _c (OSC)			ns
t _{re} (SCLK)	Serial clock interval time	50 t _c (OSC)			ns

Note: The unit means a number of noise filter sampling clock (t_c(OSC)).

SWITCHING CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _d (SCLK-SOUT)	Serial I/O output delay time (Note 1)				3	CLKs
t _v (SCLK-SOUT)	Serial I/O output valid time		0			ns
t _r (Pch)	High-breakdown-voltage P-channel open-drain output rising time	CL = 100pF VEE = V _{CC} –36 V		1.8		μs
Cosc	External capacitor size (Note 2)			18	80	pF

Note 1: The unit means a number of noise filter sampling clock (t_c(OSC)).

2: An external capacitor size varies with a mounted condition.

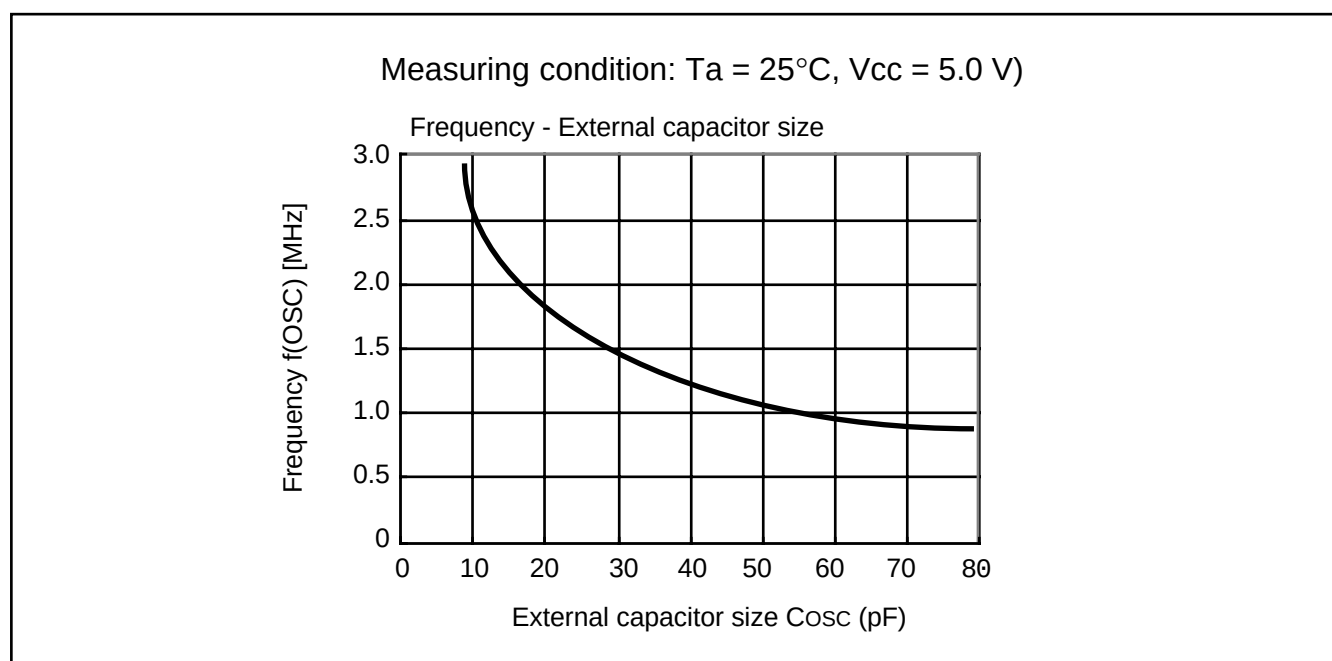


Fig. 13 Standard characteristic example of f(OSC)–Cosc

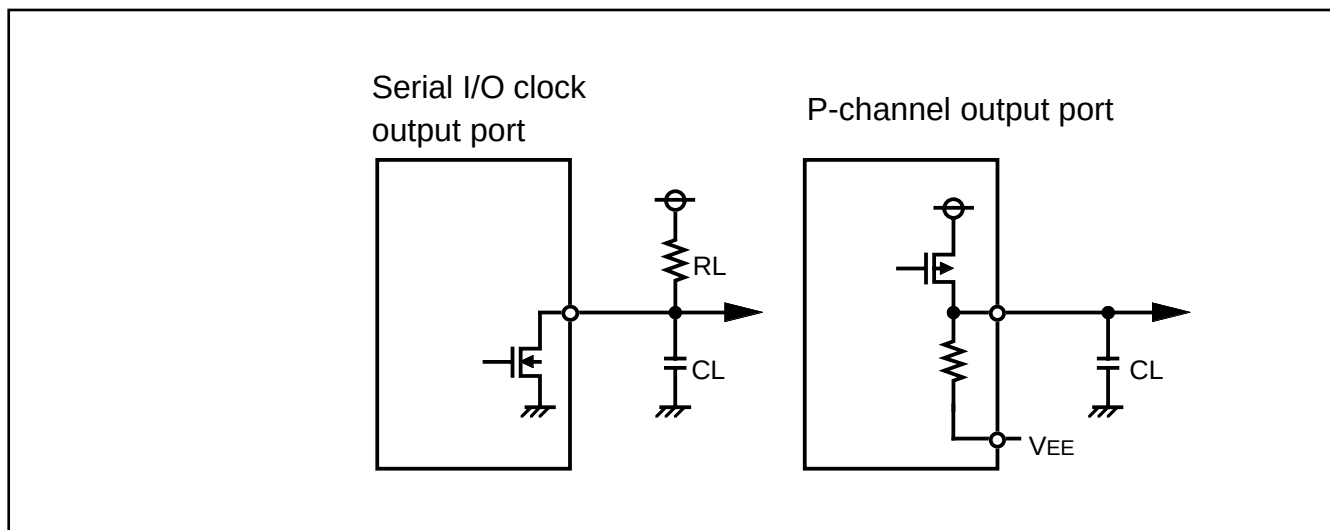


Fig.14 Output switching characteristics measurement circuit diagram

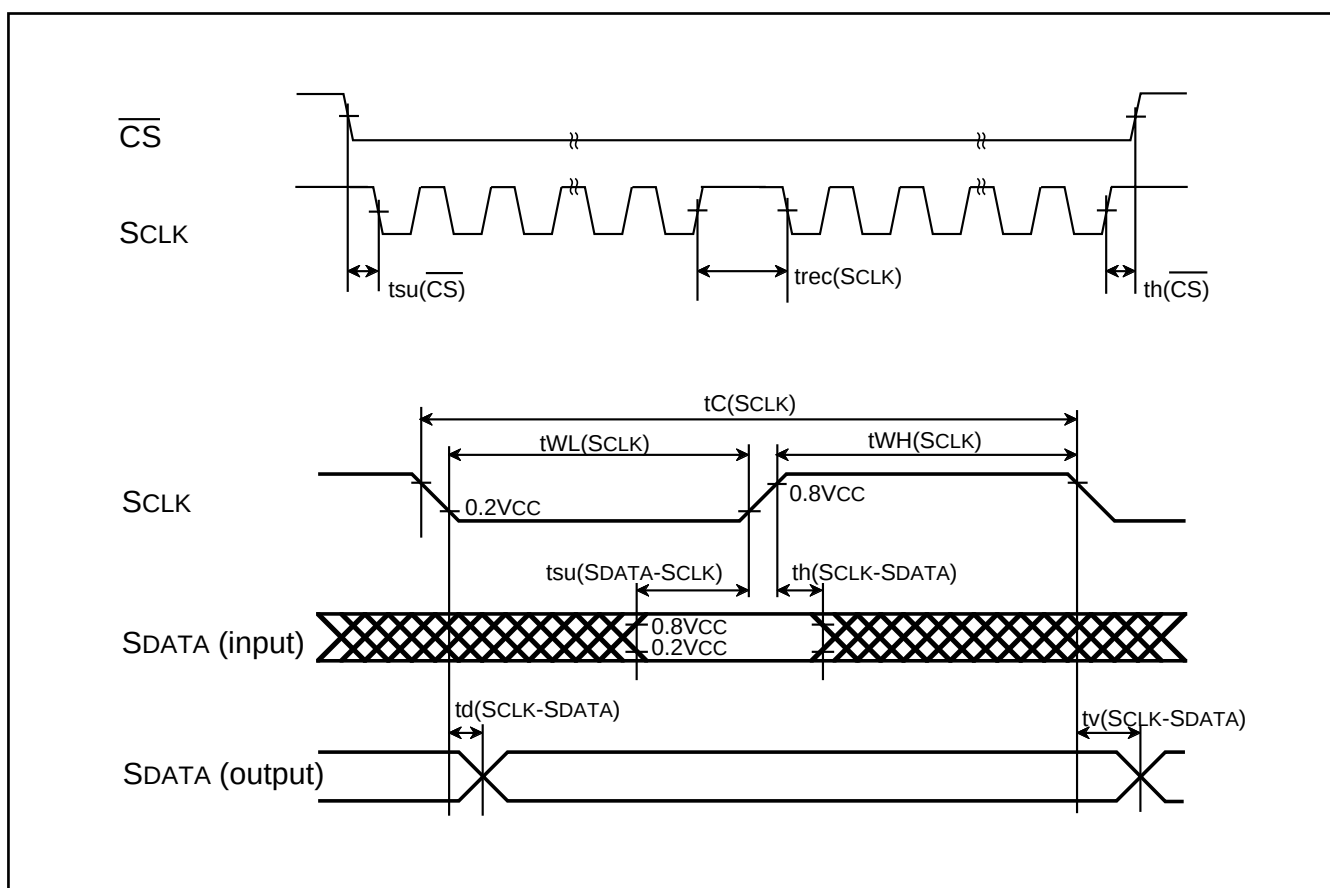
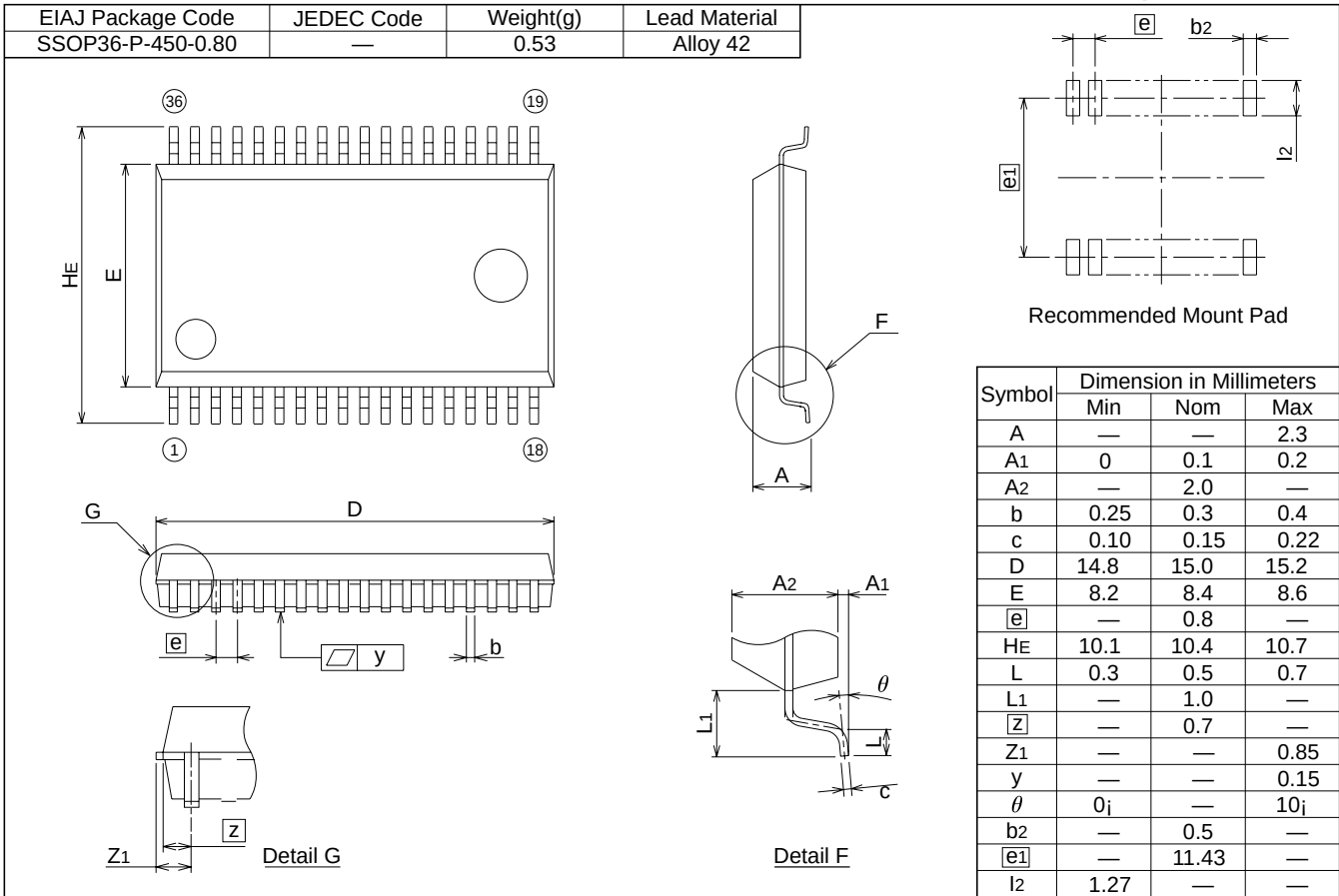


Fig.15 Timing diagram

PACKAGE OUTLINE

36P2R-G

Plastic 36pin 450mil SSOP



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