DESCRIPTION

The Mitsubishi M5M23256-XXXP is a 262144-bit mask-programmable high speed read-only memory.

The M5M23256-XXXP is fabricated by N-channel polysilicon gate technology and available in a 28-pin DIL package. It is compatible with the M5L27256K and Intel 27256 in read mode.

The XXX in type code is a three-digit decimal number assigned by Mitsubishi to identify the customer's specification to which the ROM has been programmed.

FEATURES

- 32768 word x 8-bit organization
- Access time .... 250ns (max)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power supply current (I_{CC}) Active . . 80mA (max)
  Standby . 30mA (max)
- Single 5V power supply
- 3-state output buffer
- Input and output TTL-compatible
- Standard 28-pin DIL package
- Compatible with Intel 27256

FUNCTION

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level.)

Low level inputs to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{14}$) make the data contents of the designated address location available at the data output ($D_0 \sim D_7$).
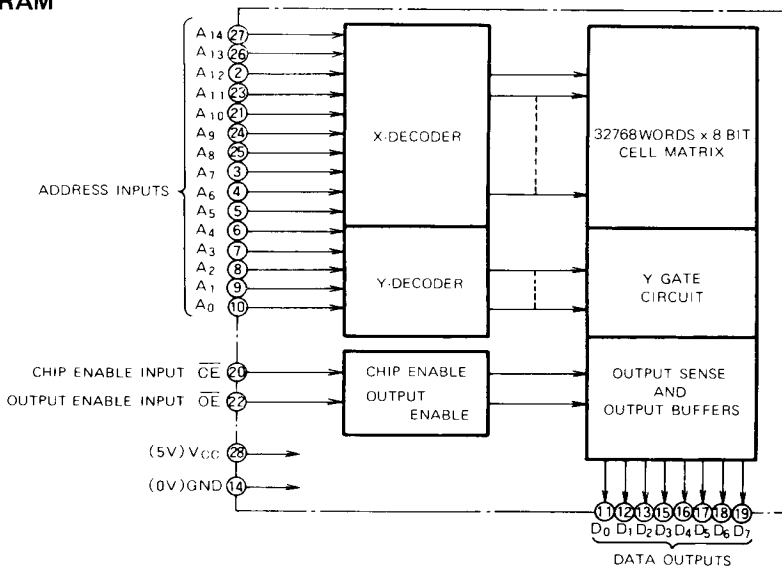
PIN CONFIGURATION (TOP VIEW)

NC. NO CONNECTION

Outline 28P4
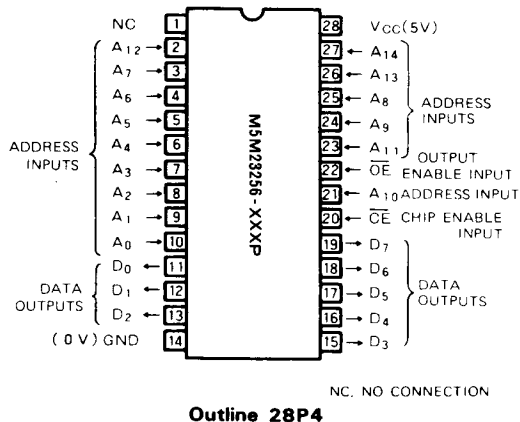
When the $\overline{CE}$ or $\overline{OE}$ signal is high, data output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

BLOCK DIAGRAM

262144-BIT(32768-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS*

Temperature under bias .... $-10°C \sim +80°C$

Storage temperature .... $-65°C \sim +150°C$

All input or output voltage** .... $-0.6V \sim +7V$

COMMENT

* Stresses above those listed may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these
or at any other conditions above those indicated in the operational sec-
tions of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods
affects device reliability.

** With respect to Ground.

D.C. ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$V_{IN} = 5.5V$	-10		10	μA
I_{LO}	Output leakage current	$V_{OUT} = 5.5V$	-10		10	μA
I_{CC1}	V_{CC} current standby	$\overline{CE} = V_{IH}$		15	30	mA
I_{CC2}	V_{CC} current active	$\overline{CE} = \overline{OE} = V_{IL}$		40	80	mA
V_{IL}	Input low voltage		-0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V

A.C. ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$			250	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$			250	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{CE} = V_{IL}$	10		100	ns
t_{DF}	Output enable high to output float	$\overline{CE} = V_{IL}$	0		90	ns
t_{OH}	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

A.C. WAVEFORMS
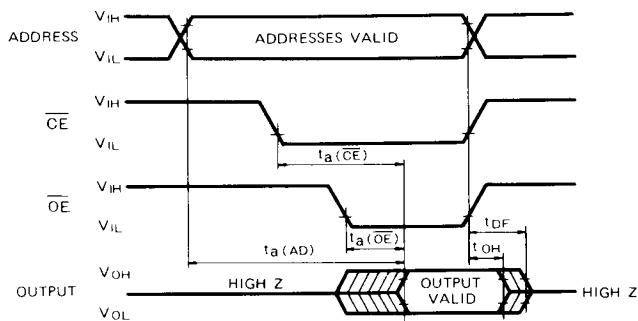
Test Conditions for A.C. Characteristics

- Input voltage: $V_{IL} = 0.45V$, $V_{IH} = 2.4V$

Input rise and fall times: $\leq 20ns$

Reference voltage at timing measurement. Inputs 1V and 2V

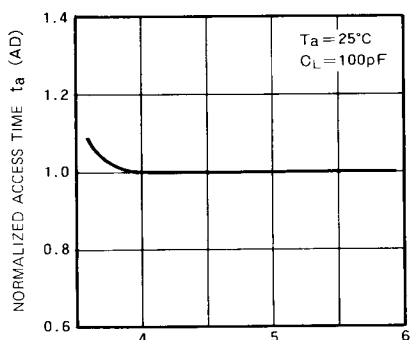Outputs 0.8V and 2V

Output load: 1 TTL gate, $C_L = 100pF$

MITSUBISHI ELECTRIC

262144-BIT(32768-WORD BY 8-BIT)MASK-PROGRAMMABLE ROM

CAPACITANCE (Ta 25°C, f = 1MHz)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance	$V_{IN}=0V$		4	6	pF
C_{OUT}	Output capacitance	$V_{OUT}=0V$		8	12	pF

TYPICAL PERFORMANCE DATA

NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE

NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE
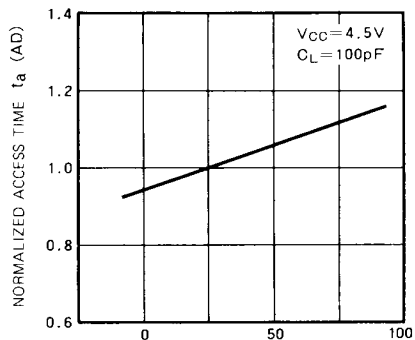
SUPPLY CURRENT VS. SUPPLY VOLTAGE
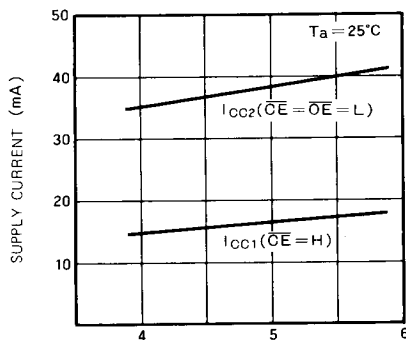
SUPPLY CURRENT VS. AMBIENT TEMPERATURE