

Video Signal Driver for DVD Players

Monolithic IC MM1568

July 10, 2002

Outline

This IC is a video signal driver IC that supports 6-ch progressive video developed for DVD players. It includes a low-pass filter that attenuates the noise element during DA conversion, and a 3-channel 6dB amp with 75Ω driver (component circuit: 2-channel).

In addition, external ESD protection diodes can be reduced by a sag correction pin for reducing output coupling capacitance, and enhancement of the ESD protection elements for output pins.

Features

1. Includes a SAG correction pin
2. Enabled to drive a 3-channel 6dB amp with 75Ω driver
3. Includes a 4th-order low-pass filter
 Frequency response: 6.75MHz ±1dB / 27MHz - 27dB min.
 13.5MHz ±1dB / 54MHz - 24dB min.
4. Includes a 6dB amp
5. Includes a power save function
6. S/N=80dB typ.(Y/C mix:74dB typ.)
7. ESD strength (aerial discharge) of ±15kV (IEC standard)
8. The component circuitry can support RGB signals with the control pin.

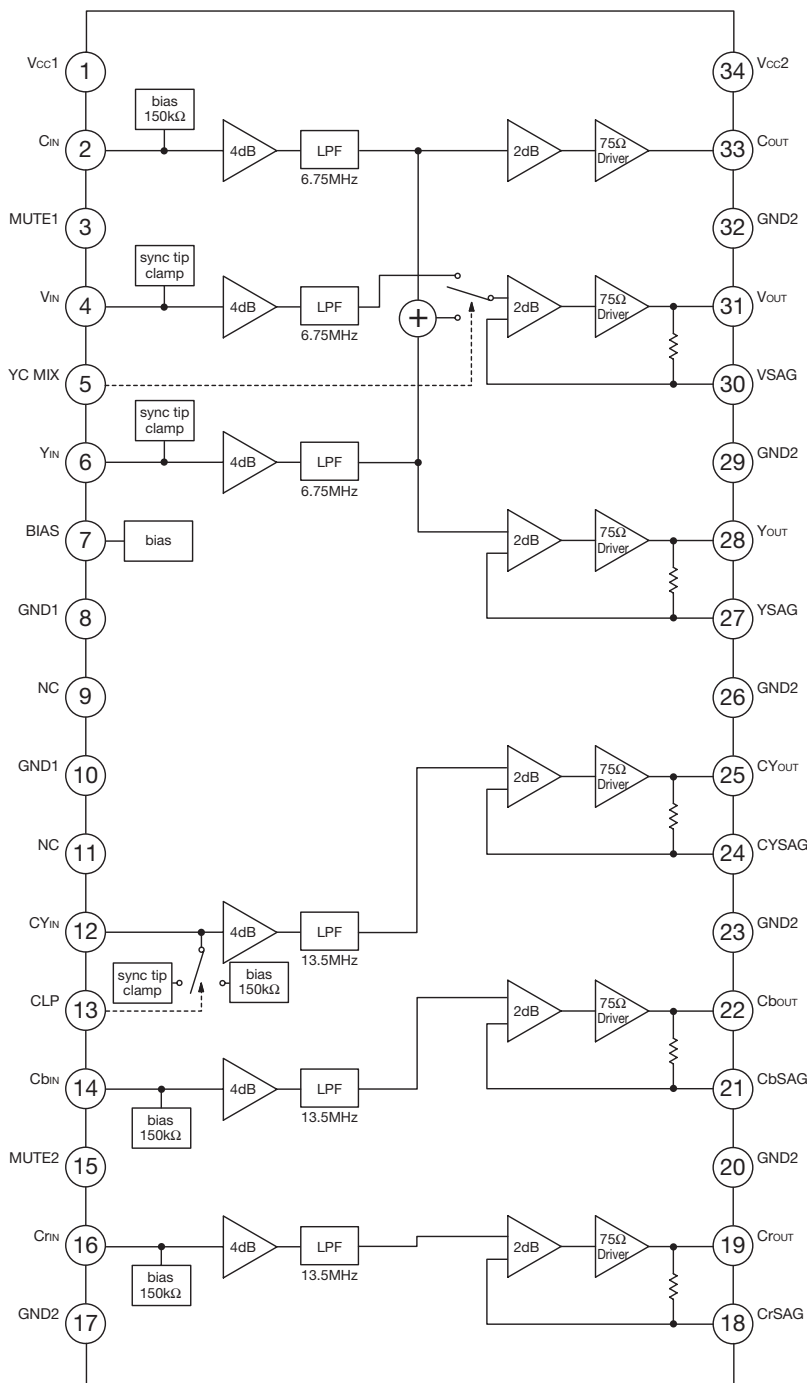
Package

SSOP-34A

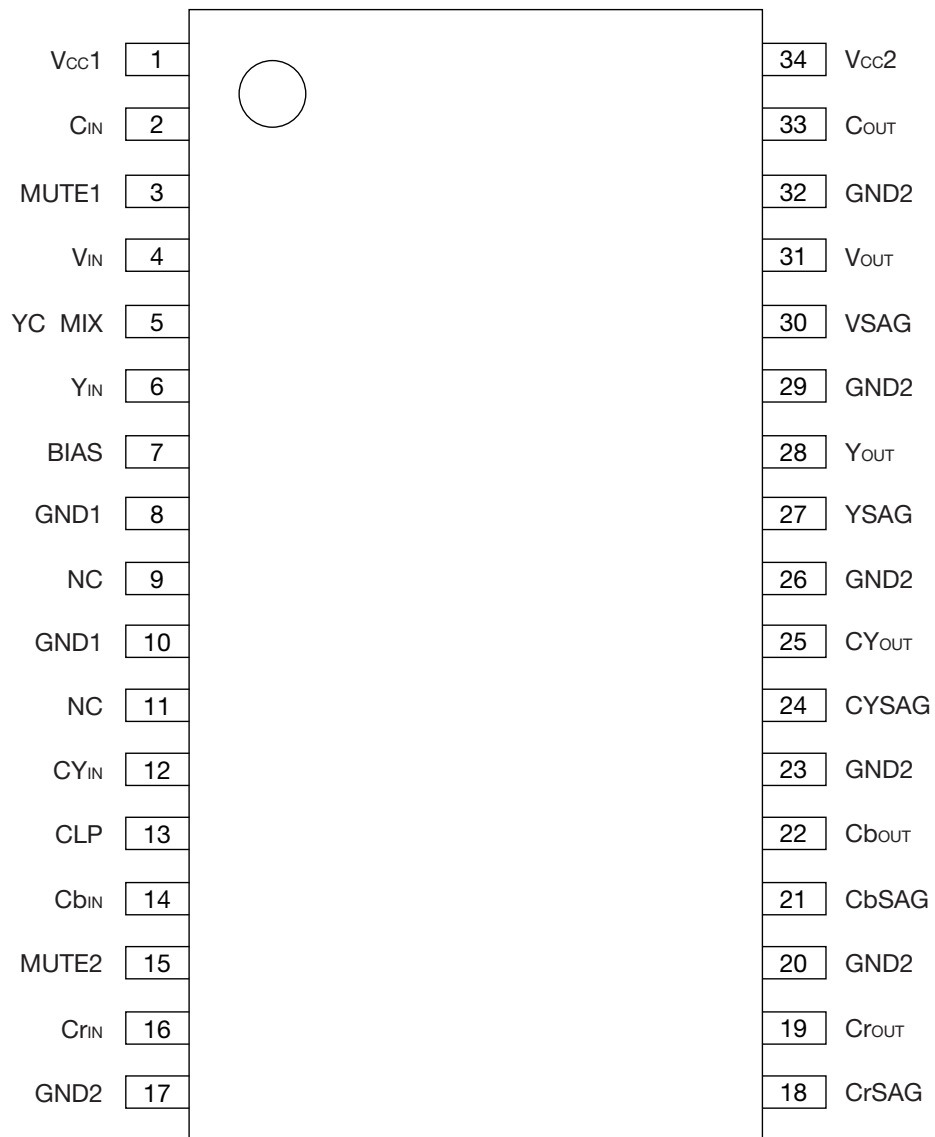
Applications

1. DVD players that support progressive video
2. Digital STB
3. Other digital video equipment

Block diagram



Pin Assignment



SSOP-34A

1	V _{CC1}	18	CrSAG
2	C _{IN}	19	C _{rOUT}
3	MUTE1	20	GND2
4	V _{IN}	21	C _{bSAG}
5	YC MIX	22	C _{bOUT}
6	Y _{IN}	23	GND2
7	BIAS	24	C _{YSAG}
8	GND1	25	C _{YOUT}
9	NC	26	GND2
10	GND1	27	Y _{SAG}
11	NC	28	Y _{OUT}
12	C _{YIN}	29	GND2
13	CLP	30	V _{SAG}
14	C _{bIN}	31	V _{OUT}
15	MUTE2	32	GND2
16	C _{rIN}	33	C _{OUT}
17	GND2	34	V _{CC2}

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
1 34	V _{CC1} V _{CC2}	V _{CC}	
2	C _{IN}	Croma input	
3 15	MUTE1 MUTE2	Mute Select Using of Mute and POWER-SAVING	
4 6	V _{IN} Y _{IN}	Video input (Composite or Y) Input clamp: Sync tip	
5	YC MIX	YC MIX select	

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
7	BIAS	Bias	
8	GND1	GND	
10	GND1		
17	GND2		
20	GND2		
23	GND2		
26	GND2		
29	GND2		
32	GND2		
9	NC	NC	
11	NC	NC	
12	CY _{IN}	Luminance input The input can select Sync tip clamp or Bias.	
13	CLP	Input clamp select	
14	C _{BI} _N	Component input	
16	C _{TI} _N		

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram	
18 21 24 27 30	C _R OUT C _B OUT C _Y OUT Y _{OUT} V _{OUT}	Signal output		
19 22 25 28 31	C _r SAG C _b SAG C _Y SAG Y _{SAG} V _{SAG}	SAG correction		
33	C _O UT	Croma output		

Absolute Maximam Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Storage temperature	T _{STG}	-65 ~ +150	°C
Operating temperature	T _{OPR}	-40 ~ +85	°C
Supply Voltage	V _{CC} max.	7	V
Power dissipation *1	P _d	1.4	W

note *1 Board mounting power dissipation. Board size 100mmX100mmX1.6mm

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Operating temperature	T _{OPR}	-40 ~ +85	°C
Operating Voltage	V _{CCOP}	4.5 ~ 5.5	V

Electrical Characteristics (Unless otherwise specified, Ta=25°C, Vcc=5V)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Consumption current	Icc1	No signal	74	97	126	mA
	Icc2	No signal Mute1:ON	36	51	66	mA
	Icc3	No signal Mute2:ON	39	55	71	mA
	Icc4	No signal Mute1 and Mute2:ON	1	3	5	mA
Croma input	V _{CIN}		1.9	2.4	2.9	V
Composite video input	V _{VIN}		1.15	1.4	1.65	V
Luminance input	V _{YIN, CYIN}		1.15	1.4	1.65	V
Component input	V _{CbIN, CrIN}		1.9	2.4	2.9	V
Croma outoutput	V _{COOUT}			2.4		V
Composite video output	V _{VOOUT}			1.1		V
Luminance output	V _{YOUT, CYOUT}			1.1		V
Component output	V _{CbOUT, CrOUT}			2.4		V
Control terminal Input current	H	I _{IHm} *2			350	μA
	L	I _{ILm} *2			35	μA
Control terminal input voltage	H	V _{thHm} *2	2.1			V
	L	V _{thLm} *2			0.7	V
Input impedance	Z _{CIN, CbIN, CrIN}		100	150	200	kΩ
Voltage gain	G _{1,2,3,5,6} *3	SIN wave:1V f=100kHz	5.7	6.0	6.3	dB
	G _{2,1,4,7,8} *3	SIN wave:1V f=100kHz	5.7	6.0	6.3	dB
Frequency characteristic	f _{1~5} *3	SIN wave:1V 6.75MHz/100kHz	-1.0	0	1.0	dB
	f _{2~5} *3	SIN wave:1V 27MHz/100kHz		-40	-27	dB
	f ₃ *3	SIN wave:1V 13.5MHz/100kHz	0	1.0	2.0	dB
	f _{4,7,8} *3	SIN wave:0.7V 13.5MHz/100kHz	0	1.0	2.0	dB
	f _{5,6~8} *3	SIN wave:1V 54MHz/100kHz		-40	-24	dB
Differential gain	DG _{1~3} *3	Staircase signal 1V		0.6	1.0	%
Differential phase	DP _{1~3} *3	Staircase signal 1V		0.6	1.0	°
Output dynamic range	DR _n *3	SIN wave:100kHz THD=1.0%	2.6	3.0		V
Crosstalk	CT _n *3	f=4.43MHz, 1V		-60	-55	dB
S/N	SN _{1,4~5} *3	BW:100k ~ 6MHz		-80		dB
	SN _{2,1~3} *3	BW:100k ~ 6MHz at MIX OUT		-74		dB
	SN _{3,6~8} *3			-80		dB
Group delay	t _{1GD1~5} *3	at 100kHz		50		ns
	t _{2GD6~8} *3	at 100kHz (Component)		30		ns
Group delay deviation	Δt _{1GDn} *3	to 3.58MHz		4		ns
	Δt _{2GDn} *3	to 4.43MHz		7		ns
	Δt _{3GD1~5} *3	to 6MHz		12		ns
	Δt _{4GD6~8} *3	to 6MHz (Component)		4		ns
	Δt _{5GD6~8} *3	to 12MHz (Component)		12		ns

note *2 The subscript number "m" is the terminal of right table.

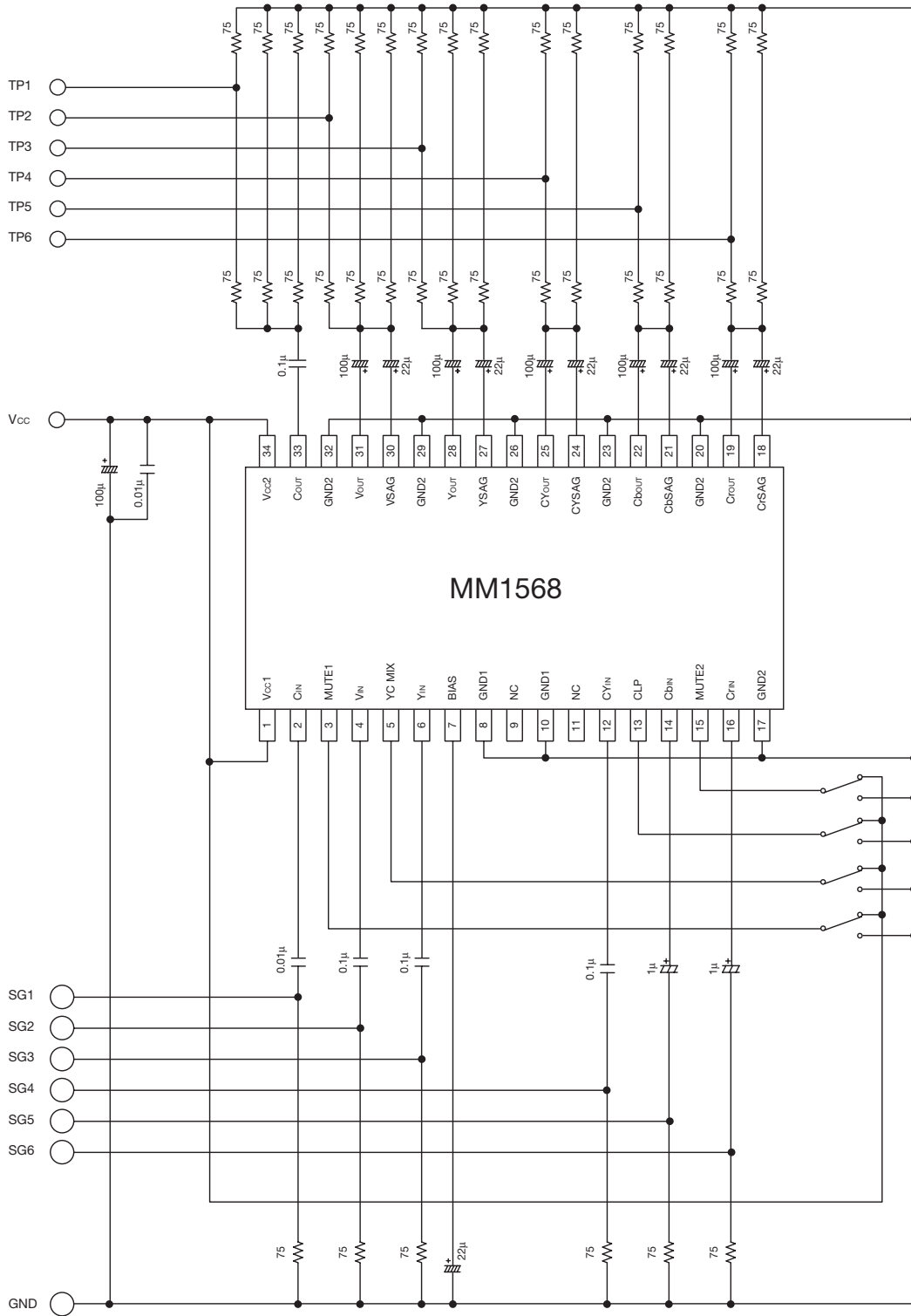
m	Terminal
1	MUTE1
2	MUTE2
3	YC MIX
4	CLP

note *3 The subscript number "n" is the combination of under table.

n	Input	Output
1	C _{IN}	V _{OUT}
2	V _{IN}	
3	Y _{IN}	
4	C _{IN}	C _{OUT}

n	Input	Output
5	Y _{IN}	Y _{OUT}
6	CY _{IN}	CY _{OUT}
7	Cb _{IN}	Cb _{OUT}
8	Cr _{IN}	Cr _{OUT}

Test Circuit

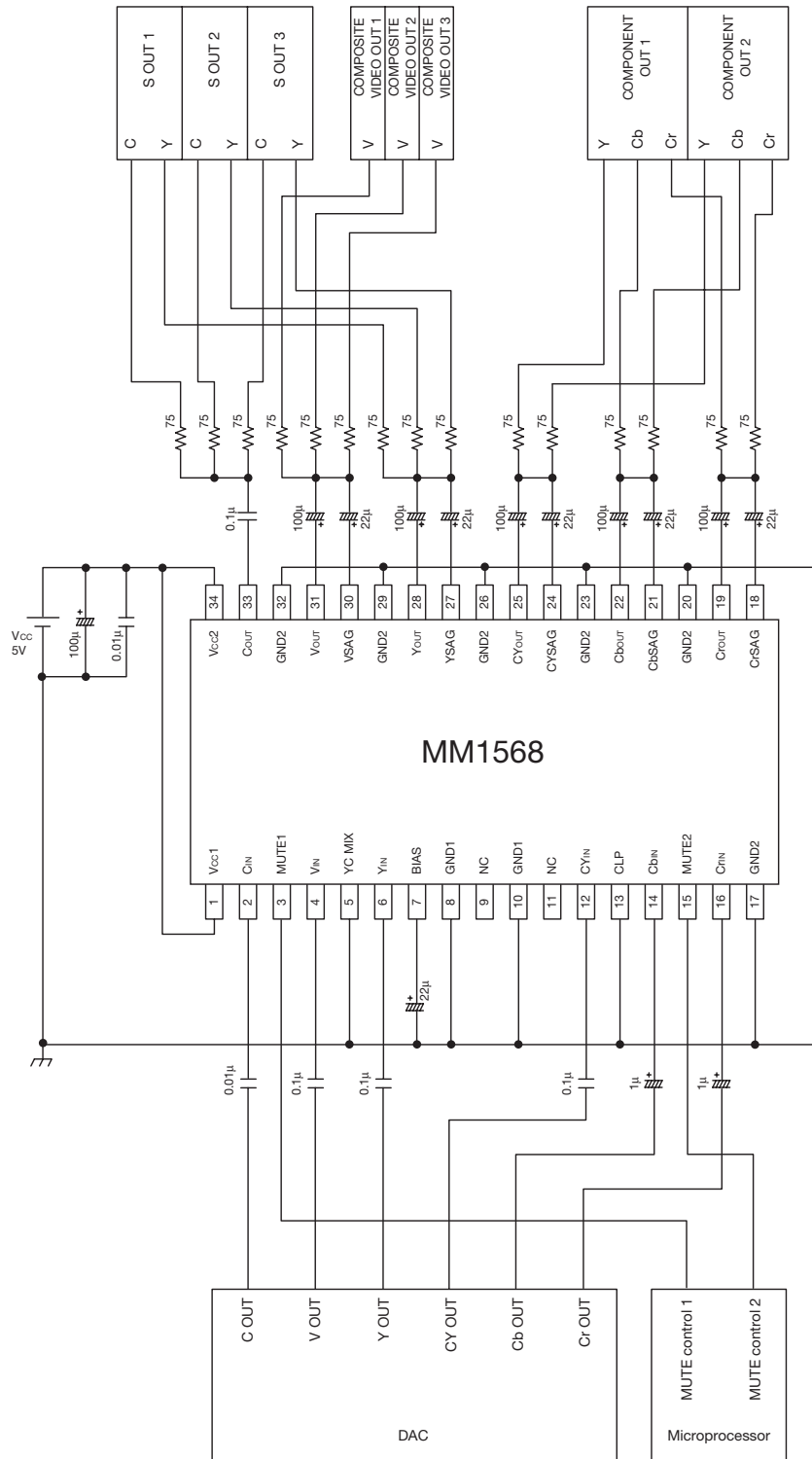


Switch Control Table

Input Select	Output Terminal	Control Terminal			
		MUTE1	YC MIX	MUTE2	CLP
MUTE	C _{OUT}	Low	*	*	*
C _{IN}		High	*	*	*
MUTE	V _{OUT}	Low	*	*	*
Y _{IN} +C _{IN}		High	Low	*	*
V _{IN}			High	*	*
MUTE	Y _{OUT}	Low	*	*	*
Y _{IN}		High	*	*	*
MUTE	CY _{OUT}	*	*	Low	*
CY _{IN} (Clamp)		*	*	High	Low
CY _{IN} (Bias)		*	*		High
MUTE	Cb _{OUT}	*	*	Low	*
Cb _{IN}		*	*	High	*
MUTE	Cr _{OUT}	*	*	Low	*
Cr _{IN}		*	*	High	*

* : Don't care

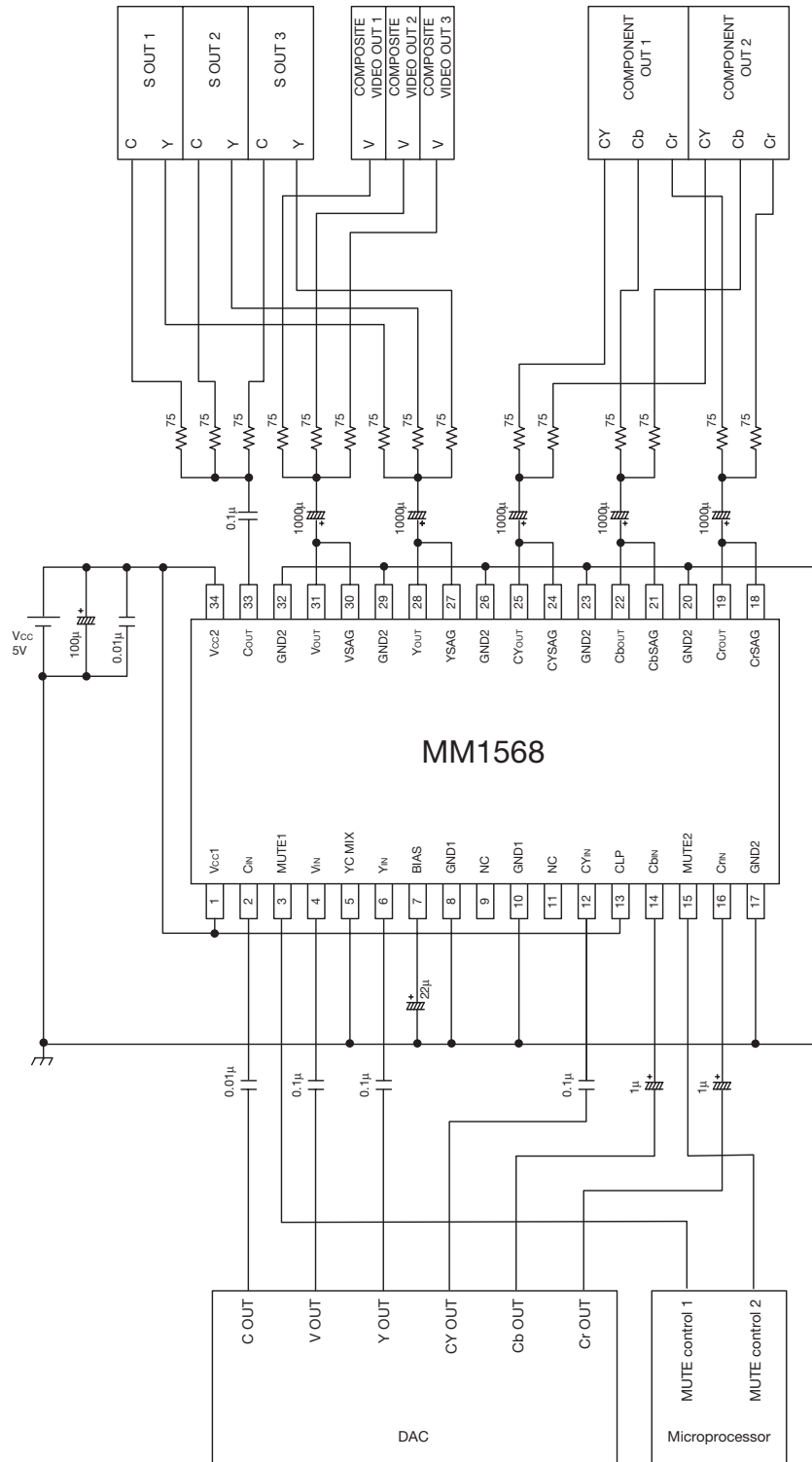
Application Circuit 1



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (34PIN).

Application Circuit 2

■ At unused the SAG correction function



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (34PIN).