

DESCRIPTION

The MP2396 is a 500kHz non-synchronous step-down switch mode converter with a built in internal power high side MOSFET. It offers a very compact solution to achieve 2A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include OCP and thermal shut down.

The MP2396 requires a minimum number of readily available standard external components and is available in a space saving SOIC8 package.

FEATURES

- Wide 4.5V to 18V Operating Input Range
- 2A Output Current
- 90mΩ Internal Power MOSFET
- Fixed 500kHz switching frequency
- Sync from 300kHz to 2MHz External Clock
- Internal Compensation
- Power Good Output
- Integrated Bootstrap Diode
- Over-Current Latch-off
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in SOIC8 package.

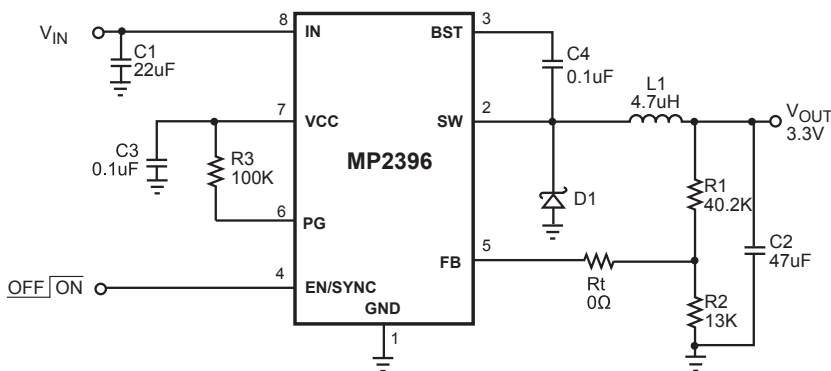
APPLICATIONS

- Notebook Systems and I/O Power
- Networking Systems
- Digital Set Top Boxes
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

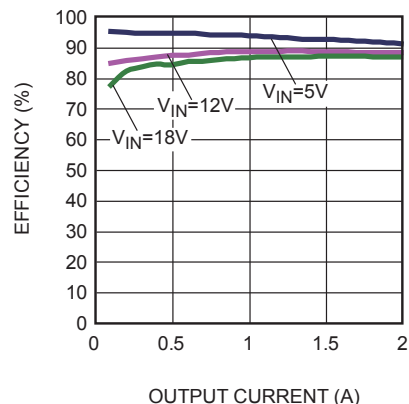
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TYPICAL APPLICATION



Efficiency vs. Output Current
 $V_{OUT}=3.3V$

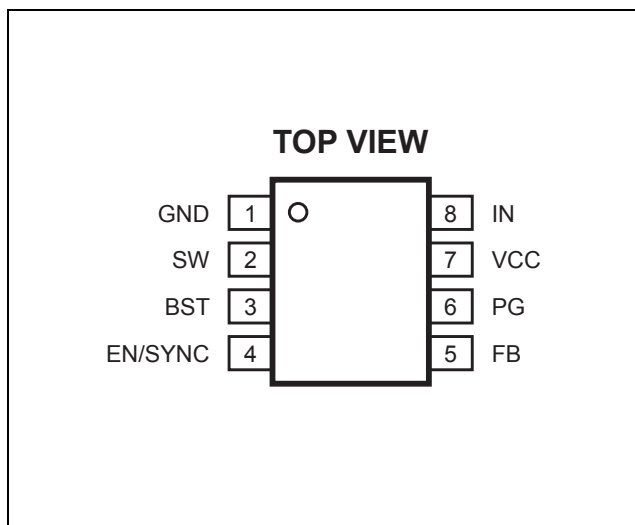


ORDERING INFORMATION

Part Number*	Package	Top Marketing	Temperature
MP2396ES	SOIC8	MP2396ES	–20°C to +85°C

For Tape & Reel, add suffix –Z (e.g. MP2396ES–Z); For RoHS compliant packaging, add suffix –LF; (e.g. MP2396ES–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Voltage V_{IN}	20V
V_{SW}	–0.3V (–5V for <10ns) to 21V
V_{BS}	$V_{SW} + 6V$
All Other Pins	–0.3V to +6V
Operating Temperature	–20°C to +85°C
Continuous Power Dissipation ($T_A = +25^\circ\text{C}$) ⁽²⁾	1.4W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	–65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Supply Voltage V_{IN}	4.5V to 18V
Output Voltage V_{OUT}	0.8V to 15V

Operating Temperature

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
SOIC8	90	45 ... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The device is not guaranteed to function outside of its operating conditions.
- The maximum allowable power dissipation is a function of the maximum junction temperature $T_J(\text{MAX})$, the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $T_A = +25^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	$V_{EN} = 0V$			10	μA
Supply Current (Quiescent)	I_{IN}	$V_{EN} = 2V$, $V_{FB} = 1V$		650		μA
Switch On Resistance	$R_{DS_{ON}}$			90		m Ω
Switch Leakage	SW_{LKG}	$V_{EN} = 0V$, $V_{SW} = 0V$		0.1	10	μA
Current Limit ⁽⁵⁾	I_{LIMIT}			3		A
Oscillator Frequency	F_{SW}	$V_{FB} = 700mV$	350	500	650	KHz
Fold-back Frequency	F_{FB}	$V_{FB} = 300mV$		140		KHz
Maximum Duty Cycle	D_{MAX}	$V_{FB} = 700mV$	85	90		%
Sync Frequency Range	F_{SYNC}		0.3		2	MHz
Feedback Voltage	V_{FB}		794	810	826	mV
Feedback Current	I_{FB}	$V_{FB} = 800mV$		10	50	nA
EN Rising Threshold	V_{EN_RISING}		1.05	1.3	1.55	V
EN Threshold Hysteresis	V_{EN_HYS}			0.35		V
EN Input Current	I_{EN}	$V_{EN} = 2V$		2		μA
		$V_{EN} = 0V$		0.1		
EN Turn Off Delay	EN_{Td-Off}			5		μsec
Soft-Start Period			1	3.5	5	ms
Power Good High Threshold	$V_{TH_{PG}}$			0.9		V_{FB}
Power Good Low Threshold	$V_{TL_{PG}}$			0.7		V_{FB}
Power Good Delay	PG_{Td}			15		μs
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	$V_{PG} = 3.3V$			25	nA
V_{IN} Under Voltage Lockout Threshold Rising	$INUV_{Vth}$		3.75	4.0	4.25	V
V_{IN} Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			880		mV
VCC Regulator	V_{CC}			5.1		V
VCC Load Regulation		$I_{CC} = 1mA$		3		%
Thermal Shutdown	T_{SD}			150		$^{\circ}C$

Note:

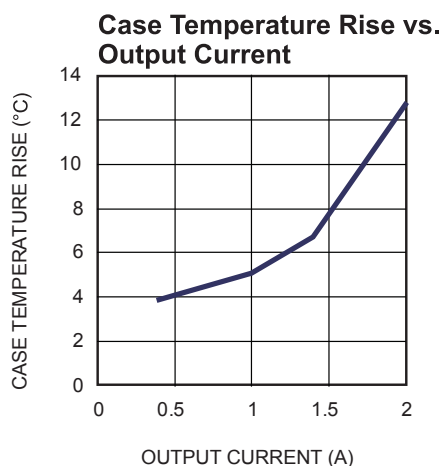
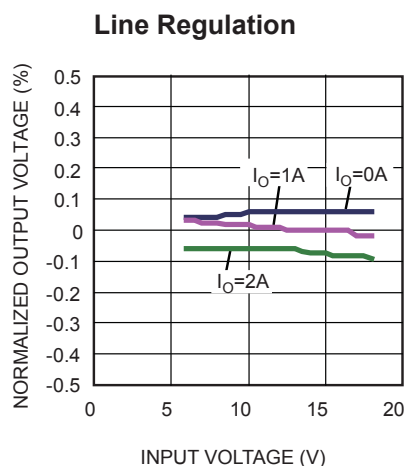
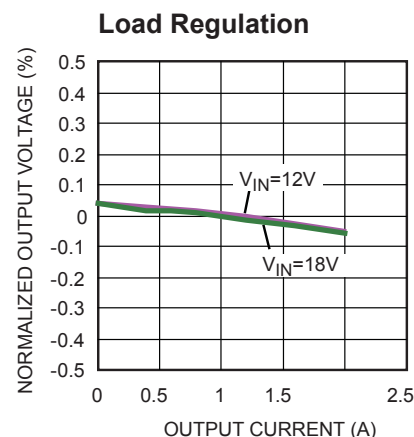
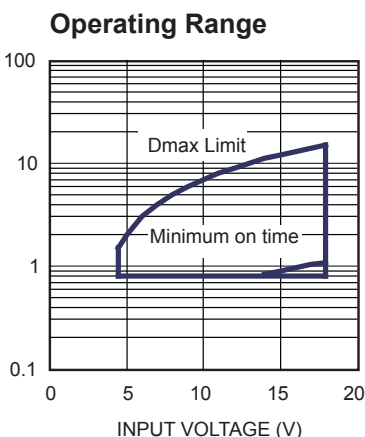
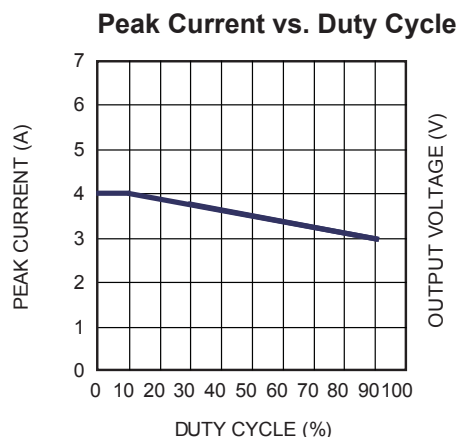
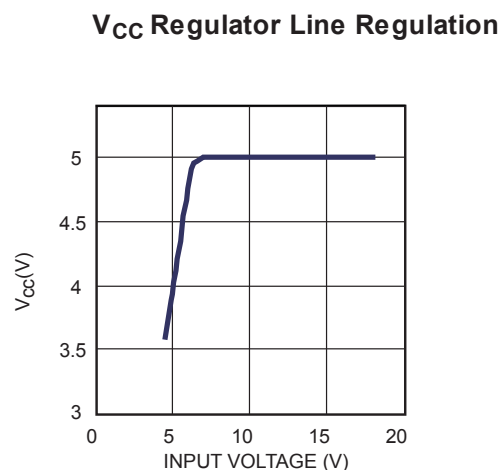
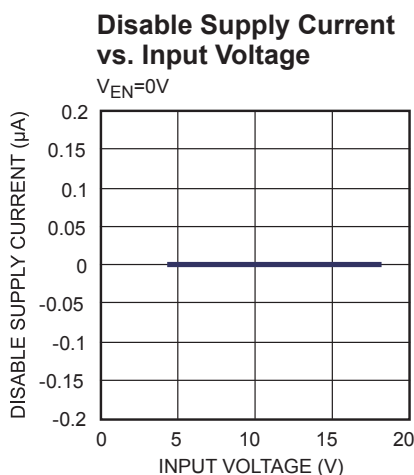
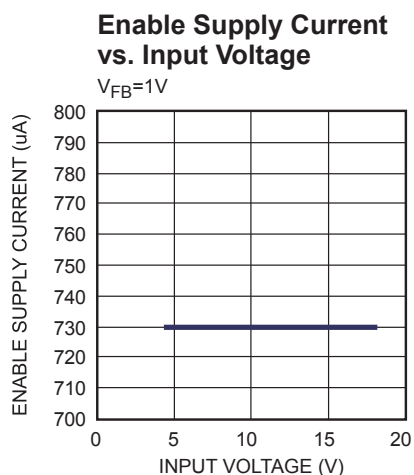
5) Guaranteed by design.

PIN FUNCTIONS

Pin #	Name	Description
1	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
2	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
3	BST	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
4	EN/SYNC	EN=1 to enable the chip. External clock can be applied to EN pin for changing switching frequency. For automatic start-up, connect EN pin to VIN by proper EN resistor divider as Figure 2 shows.
5	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 500mV.
6	PG	Power Good Output, the output of this pin is open drain. Power good threshold is 90% low to high and 70% high to low of regulation value.
7	VCC	Bias Supply. Decouple with 0.1uF~0.22uF cap. And the capacitance should be no more than 0.22uF.
8	IN	Supply Voltage. The MP2396 operates from a +4.5V to +18V input rail. C1 is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.

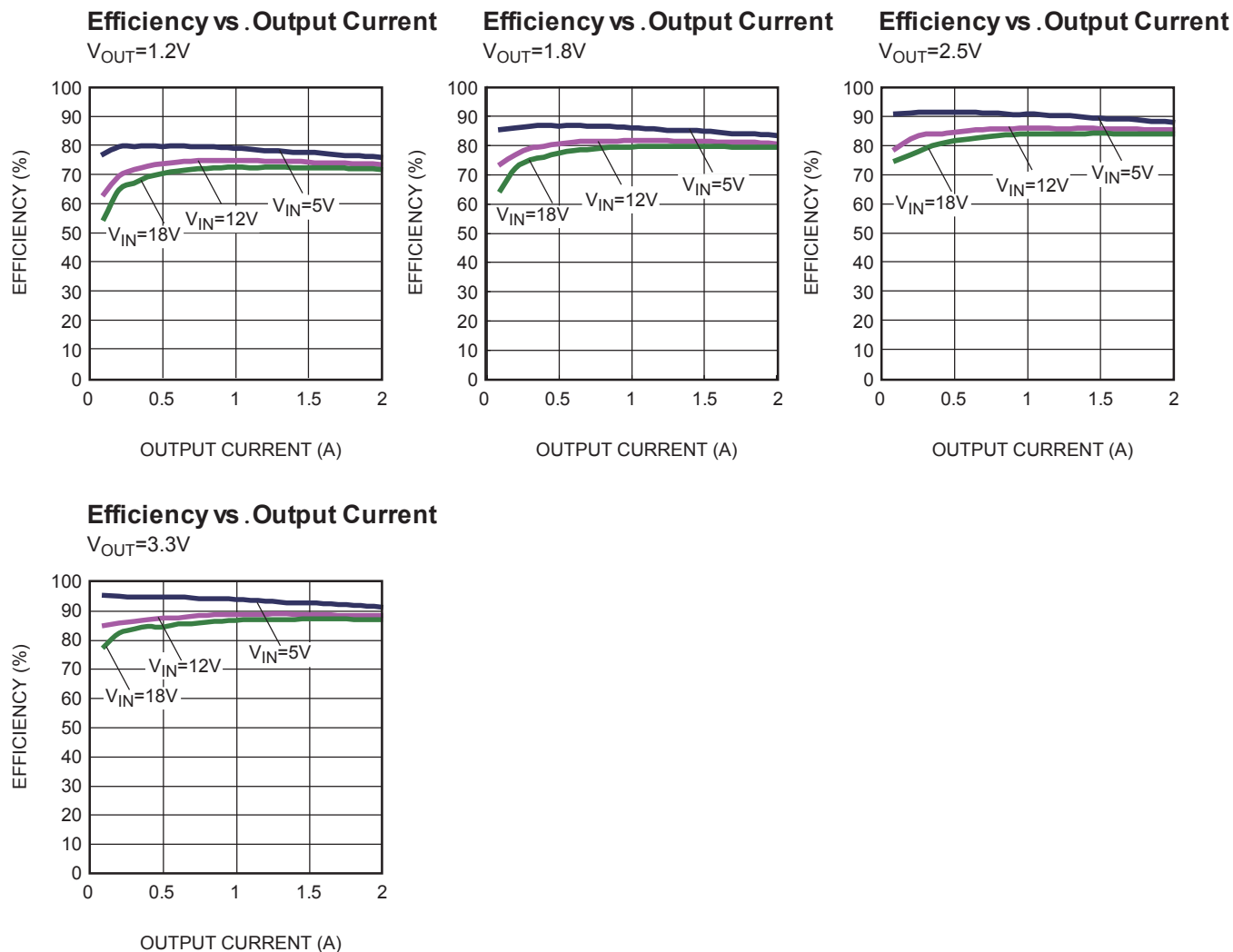
TYPICAL PERFORMANCE CURVES

$V_{IN}=12V$, $V_{OUT}=3.3V$, $L=4.7\mu H$, $T_A = +25^\circ C$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES *(continued)*

$V_{IN}=12V$, $V_{OUT}=3.3V$, $L=4.7\mu H$, $T_A = +25^\circ C$, unless otherwise noted.

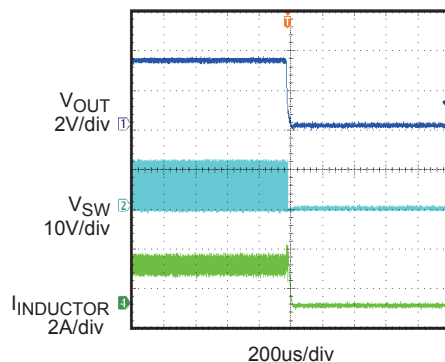


TYPICAL PERFORMANCE CURVES *(continued)*

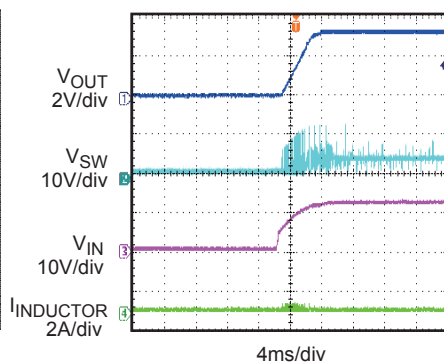
$V_{IN}=12V$, $V_{OUT}=3.3V$, $L=4.7\mu H$, $T_A = +25^\circ C$, unless otherwise noted.

Short Entry

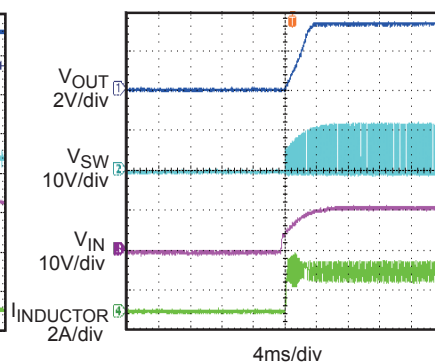
$I_0=2A$



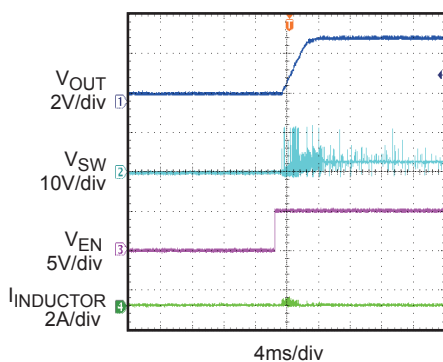
Power up without Load



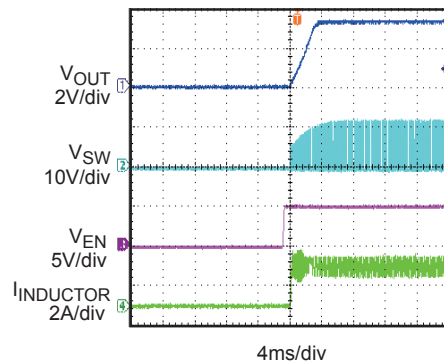
Power up with 2A Load



Enable Startup without Load

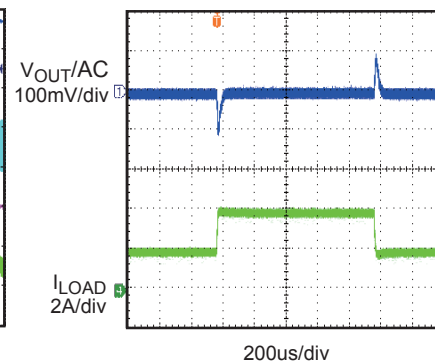


Enable Startup with 2A Load



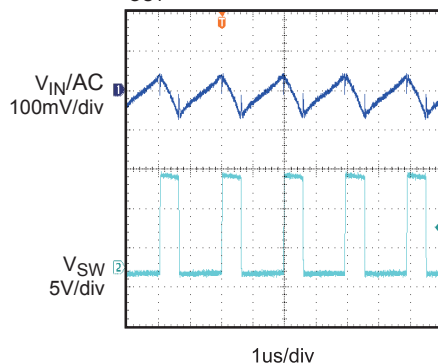
Load Transient Response

$I_0=1A \sim 2A$



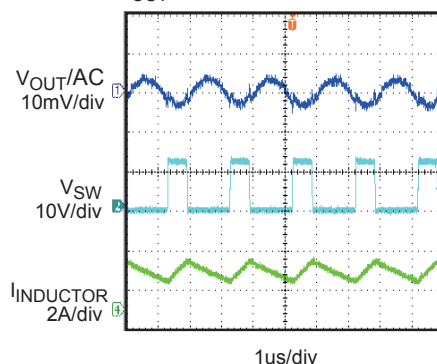
Input Ripple Voltage

$I_{OUT}=2A$



Output Ripple Voltage

$I_{OUT}=2A$



BLOCK DIAGRAM

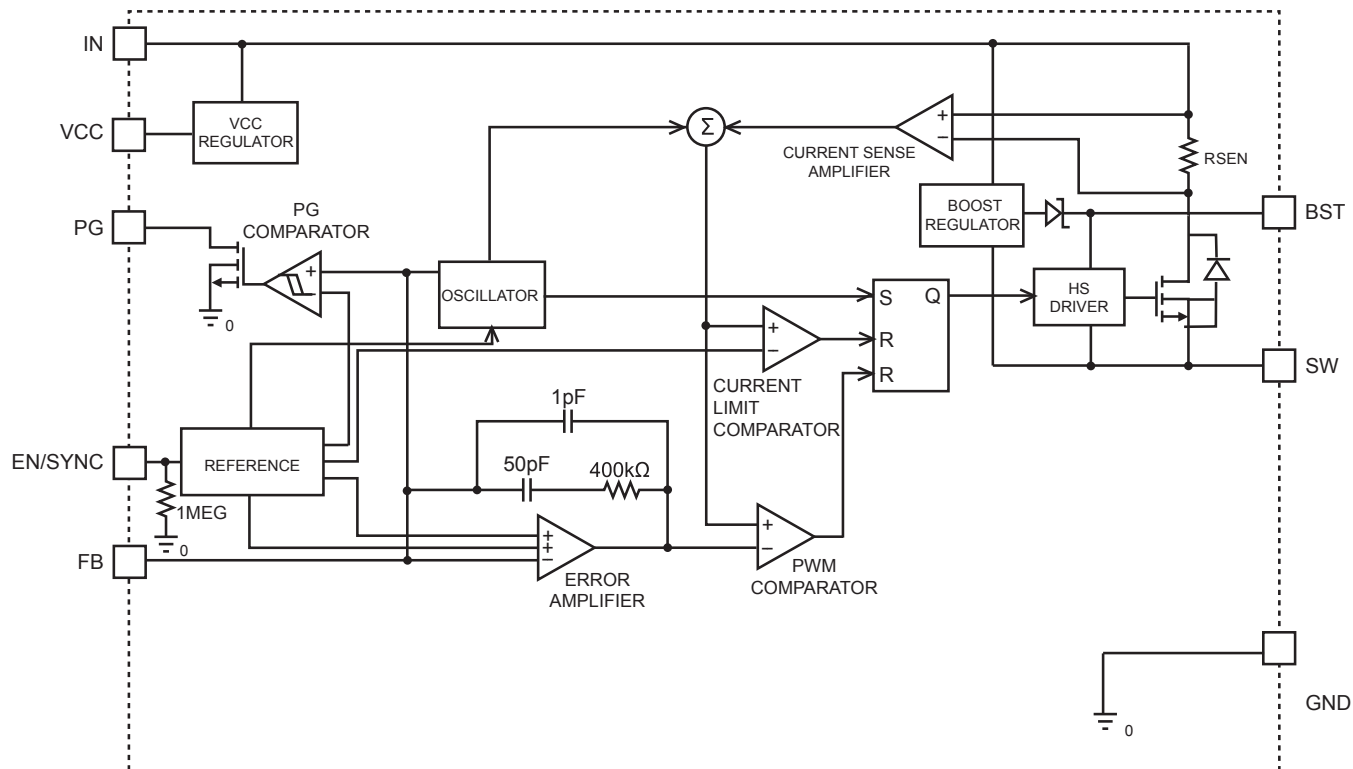


Figure 1—Functional Block Diagram

OPERATION

The MP2396 is a high frequency non-synchronous step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 2A continuous output current over a wide input supply range with excellent load and line regulation.

The MP2396 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off

Power Good Indicator

When the FB is below $0.70V_{FB}$, the PG pin will be internally pulled low. When the FB is above $0.9V_{FB}$, the PG becomes an open-drain output.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases, a 0.1uF ceramic capacitor for decoupling purpose is required.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.810V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Enable/Sync Control

EN/Sync is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator, drive it low to turn it off. There is an internal 1MEG resistor from EN/Sync to GND thus EN/Sync can be floated to shut down the chip.

1) Enabled by external logic H/L signal

The chip starts up once the enable signal goes higher than EN/SYNC input high voltage (2V), and is shut down when the signal is lower than EN/SYNC input low voltage (0.4V). To disable the chip, EN must be pulled low for at least 5μs. The input is compatible with both CMOS and TTL.

2) Enabled by Vin through voltage divider.

Connect EN with VIN through a resistive voltage divider for automatic startup as the figure 2 shows.

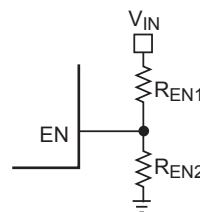


Figure 2—Enable Divider Circuit

Choose the value of the pull-up resistor R_{EN1} and pull-down resistor R_{EN2} to reset the automatic start-up voltage:

$$V_{IN_START} = V_{EN_RISING} \cdot \frac{(R_{EN1} + R_{EN2} \parallel 1M\Omega)}{R_{EN2} \parallel 1M\Omega}$$

$$V_{IN_STOP} = V_{EN_FALLING} \cdot \frac{(R_{EN1} + R_{EN2} \parallel 1M\Omega)}{R_{EN2} \parallel 1M\Omega}$$

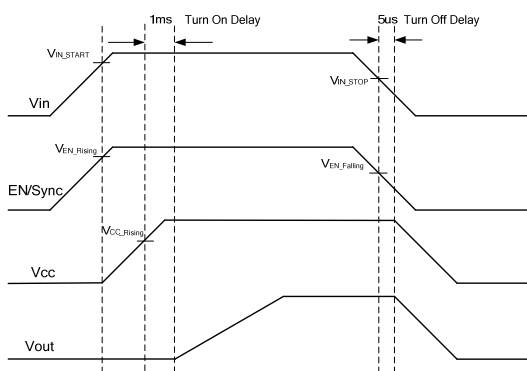


Figure 3—Startup Sequence Using EN Divider

3) Synchronized by External Sync Clock Signal

The chip can be synchronized to external clock range from 300kHz up to 2MHz through this pin 2ms right after output voltage is set, with the internal clock rising edge synchronized to the external clock rising edge.

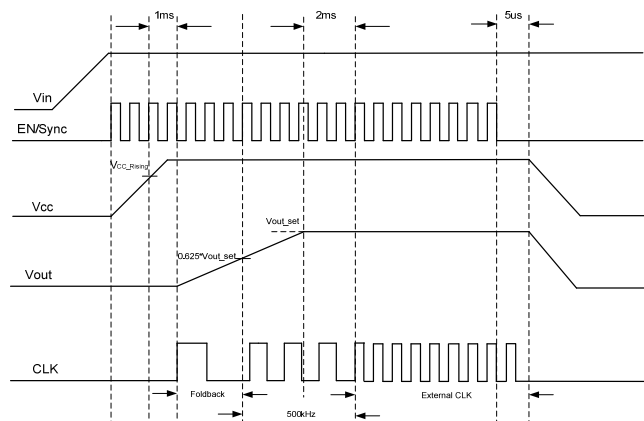


Figure 4—Startup Sequence Using External Sync Clock Signal

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP2396 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is a consistent 3.2V.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 1.2V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally fixed to 4ms.

Over-Current-Protection and Latch Off

The MP2396 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the MP2396 is latched off until En or IN is recycled. This protection mode is especially useful when the output is dead-short to ground.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its

lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M3, C4, L1 and C2 (Figure 5). If (VIN-VSW) is more than 5V, U2 will regulate M3 to maintain a 5V BST voltage across C4.

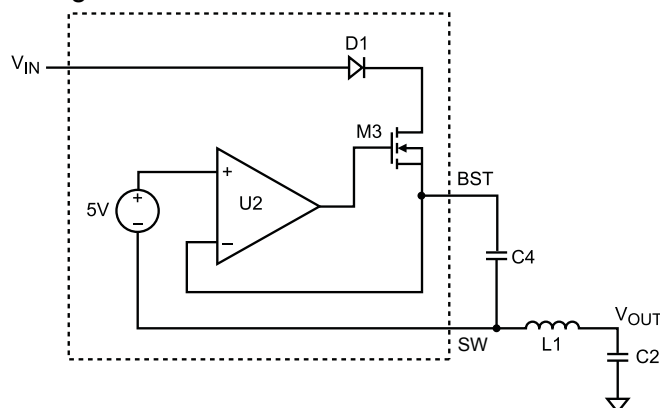


Figure 5—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 to be around 40.2kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{FB}} - 1}$$

The T-type network is highly recommended when Vo is low, as Figure 6 shows.

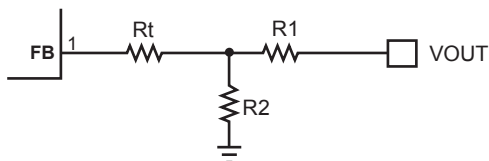


Figure 6— T-type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V _{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)
1.05	4.99(1%)	16.5(1%)	24.9(1%)
1.2	4.99(1%)	10.2(1%)	24.9(1%)
1.5	4.99(1%)	5.76(1%)	24.9(1%)
1.8	4.99(1%)	4.02(1%)	24.9(1%)
2.5	40.2 (1%)	19.1(1%)	0
3.3	40.2(1%)	13(1%)	0
5	40.2(1%)	7.68(1%)	0

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor ripple current to be approximately 30% if the maximum load current, 2A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Output Rectifier Diode

The output rectifier diode supplies the current to the indicator when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage and whose current rating is greater than the maximum load current. Table 2 lists example Schottky diodes and manufacturers.

Table 2—Diode Selection Guide

Part No.	Voltage/Current Raging	Manufacture
B330A	30V, 3A	Diodes Inc.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22μF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at V_{IN} = 2V_{OUT}, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

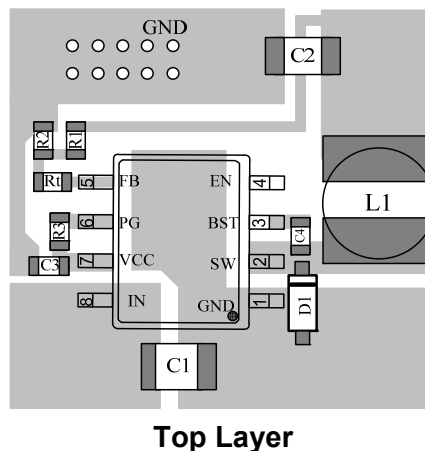
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2396 can be optimized for a wide range of capacitance and ESR values.

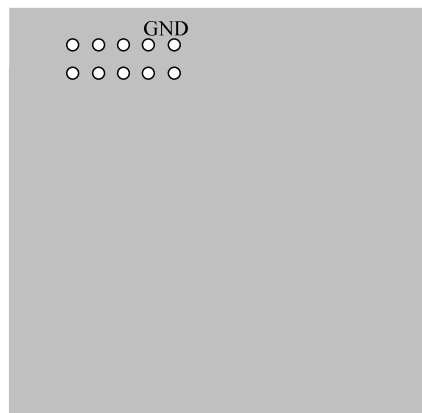
PCB Layout

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure 7 for references.

- 1) Keep the power loop of input capacitor, HS switch, LS switch as small as possible.
- 2) Keep the connection of input capacitor and IN pin as short and wide as possible.
- 3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 4) Route SW away from sensitive analog areas such as FB.
- 5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.
- 6) Adding RC snubber circuit from IN pin to SW pin can reduce SW spikes.



Top Layer



Bottom Layer

Figure 7—PCB Layout

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode is:

- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In this case, an external BST diode is recommended from the VCC pin to BST pin, as shown in Figure 8

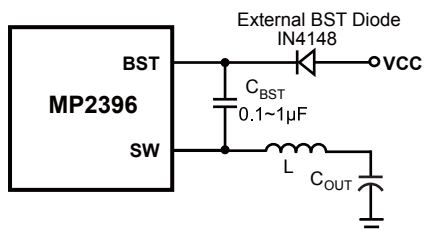
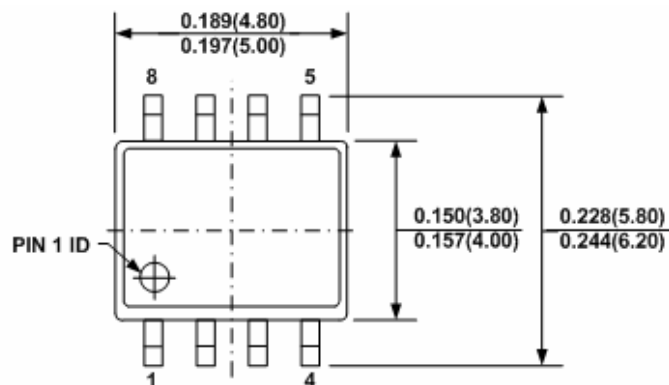


Figure 8—Add Optional External Bootstrap Diode to Enhance Efficiency

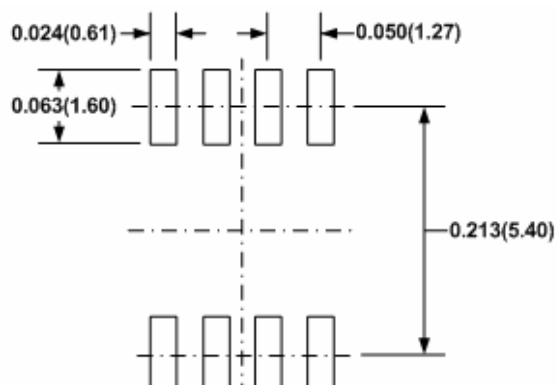
The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF

PACKAGE INFORMATION

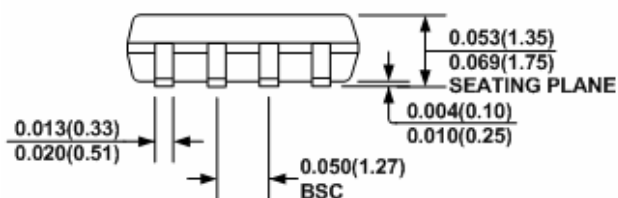
SOIC8



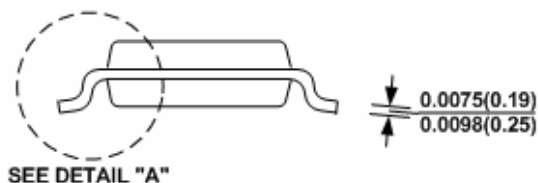
TOP VIEW



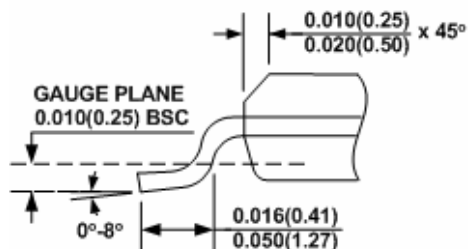
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.