



March 2015

MTD3055VL

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N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

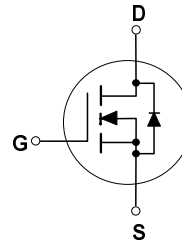
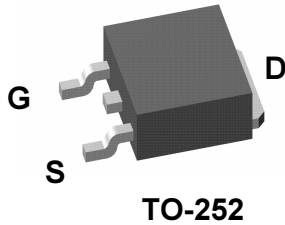
This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 12 A, 60 V. $R_{DS(ON)} = 0.18 \Omega @ V_{GS} = 5 V$
- Critical DC electrical parameters specified at elevated temperature.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(th)} < 2 V$.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.



Absolute Maximum Ratings $T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated Value	Units
V_{DSS}	Drain-Source Voltage	60	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Maximum Drain Current -Continuous (Note 1)	12	A
	$T_C = 100^\circ\text{C}$ (Note 1)	8	
P_D	Maximum Drain Current -Pulsed	42	W
	Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1)	48	
	$T_A = 25^\circ\text{C}$ (Note 1a)	3.9	
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to- Case (Note 1)	3.13	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to- Ambient (Note 1a)	71.4	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MTD3055VL	MTD3055VL	13"	16mm	2500

* Die and manufacturing source subject to change without prior notification.

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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DRAIN-SOURCE AVALANCHE RATINGS (Note 2)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25\text{ V}, I_D = 12\text{ A}$			72	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				12	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		54		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			10	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$			100	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -15\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.5	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-2.6		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 5\text{ V}, I_D = 6\text{ A}$			0.18	Ω
$V_{DS(on)}$	Drain-Source On-Voltage On-Resistance	$V_{GS} = 5\text{ V}, I_D = 12\text{ A}$			2.6	V
		$I_D = 6\text{ A}, T_J = 150^\circ\text{C}$			2.5	
g_{FS}	Forward Transconductance	$V_{DS} = 8\text{ V}, I_D = 6\text{ A}$	5.0			S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$			570	pF
C_{oss}	Output Capacitance				160	pF
C_{riss}	Reverse Transfer Capacitance				40	pF

Switching Characteristics (Note 2)

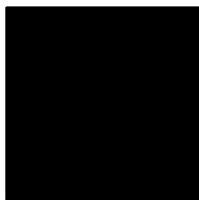
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 12\text{ A}, V_{GS} = 5\text{ V}, R_{GEN} = 9.1\ \Omega$			20	ns
t_r	Turn-On Rise Time				190	ns
$t_{d(off)}$	Turn-Off Delay Time				30	ns
t_f	Turn-Off Fall Time				90	ns
Q_g	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 12\text{ A}, V_{GS} = 5\text{ V}$			10	nC
Q_{gs}	Gate-Source Charge			2		nC
Q_{gd}	Gate-Drain Charge			6.1		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current (Note 2)				12	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current (Note 2)				42	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$ (Note 2)			1.3	V
t_{rr}	Drain-Source Reverse Recovery Time	$I_F = 12\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		51		nS

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

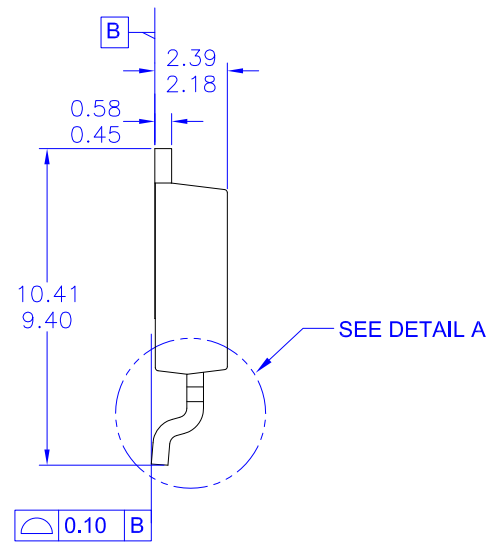
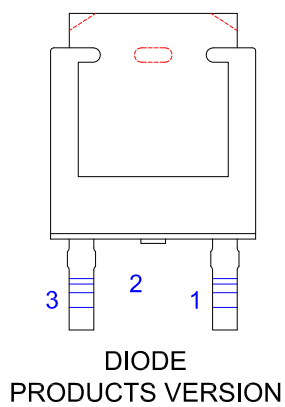
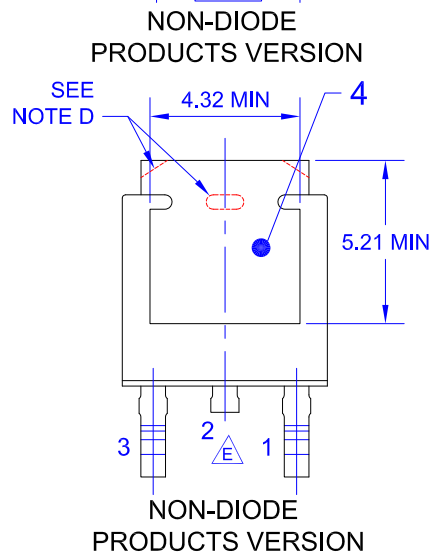
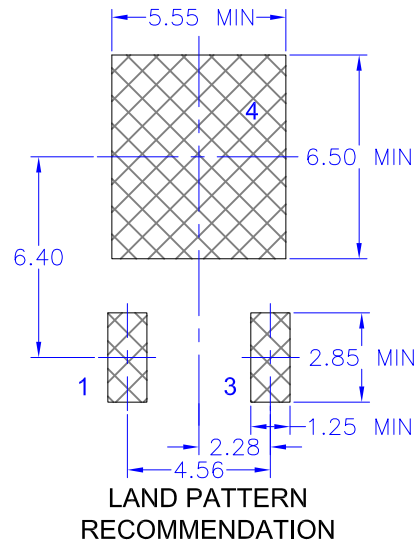
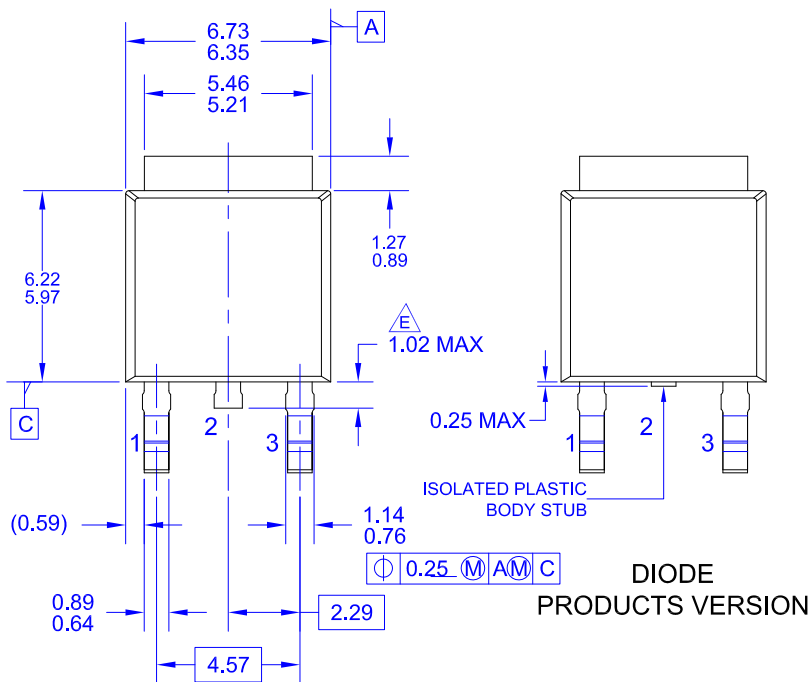


■ a) $R_{\theta JA} = 38^\circ\text{C/W}$ when mounted on a 1 in² pad of 2oz copper.

■ b) $R_{\theta JA} = 96^\circ\text{C/W}$ when mounted on a minimum pad.

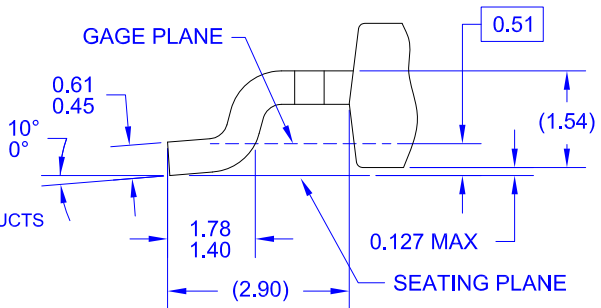
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11





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