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NTE887M
Integrated Circuit
Low Power, JFET OP Amplifier

Description:

The NTE887M is a JFET–input operational amplifier in an 8–Lead DIP type package designed as a low–power version of the NTE857M amplifier. This device features high input impedance, wide bandwidth, high slew rate, and low input offset and bias current.

Features:

- Very Low Power Consumption
- Typical Supply Current: 200μA
- Wide Common–Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common–Mode Input Voltage Range Includes V_{CC}+
- Output Short–Circuit Protection
- High Input Impedance: JFET–Input Stage
- Internal Frequency Compensation
- Latch–Up–Free Operation
- High Slew rate: 3.5V/μs Typ

Absolute Maximum Ratings: (T_A = 0° to +70°C unless otherwise specified)

Supply Voltage (Note 1), V_{CC}+ . . . . . +18V
Supply Voltage (Note 1), V_{CC}– . . . . . –18V
Differential Input Voltage (Note 2), V_{ID} . . . . . ±30V
Input Voltage (Note 1, Note 3), V_I . . . . . ±15V
Duration of Output Short Circuit (Note 4), t_s . . . . . Unlimited
Continuous Total Dissipation, P_D
$T_A \le +25°C$ 680mW
Derate Above +65°C . . . . . 8mW/°C
T_A = +70°C 640mW
Operating Ambient Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 1/16” (1.6mm) from case for 10sec), T_L . . . . . +260°C

Note 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC}+ and V_{CC}–.

Note 2. Differential voltages are at the non–inverting input pin with respect to the inverting input pin.

Note 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15V, whchever is less.

Note 4. The output may be shorted to GND or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

Electrical Characteristics: ($V_{CC}\pm$ = ±15V, Note 5 unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	V_O = 0, R_S = 50Ω	T_A = +25°C	–	3	15	mV
			T_A = 0° to +70°C	–	–	20	mV
Temperature Coefficient of Input Offset Voltage	α_{VIO}	V_O = 0, R_S = 50Ω, T_A = 0° to +70°C		–	10	–	µV/°C
Input Offset Current	I_{IO}	V_O = 0, Note 6	T_A = +25°C	–	5	200	pA
			T_A = 0° to +70°C	–	–	5	nA
Input Bias Current	I_{IB}	V_O = 0, Note 6	T_A = +25°C	–	30	400	pA
			T_A = 0° to +70°C	–	–	10	nA
Common–Mode Input Voltage Range	V_{ICR}	T_A = +25°C		±11	–12 +15	–	V
Maximim Peak Output Voltage Swing	V_{OM}	R_L = 10kΩ, T_A = +25°C		±10.0	±13.5	–	V
		$R_L \geq$ 10kΩ, T_A = 0° to +70°C		±10.0	–	–	V
Large–Signal Differential Voltage Amplification	A_{VD}	V_O = ±10V, $R_L \geq$ 10kΩ	T_A = +25°C	3	6	–	V/mV
			T_A = 0° to +70°C	3	–	–	V/mV
Unity–Gain Bandwidth	B_1	R_L = 10kΩ, T_A = +25°C		–	1	–	MHz
Input Resistance	r_i	T_A = +25°C		–	10^{12}	–	Ω
Common–Mode Rejection Ratio	CMRR	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50Ω, T_A = +25°C		70	86	–	dB
Supply Volatge Rejection Ratio ($\Delta V_{CC}\pm/\Delta V_{IO}$)	k_{SVR}	V_{CC} = ±15V to ±9V, V_O = 0, R_S = 50Ω, T_A = +25°C		70	95	–	dB
Total Power Dissipation	P_D	No Load, V_O = 0, T_A = +25°C		–	6.0	7.5	mW
Supply Current	I_{CC}	No Load, V_O = 0, T_A = +25°C		–	200	250	µA
Crosstalk Attenuation	V_{o1}/V_{o2}	A_{VD} = 100, T_A = +25°C		–	120	–	dB

Note 5. All characteristics are measured under open–loop conditions with zero common–mode voltage unless otherwise specified.

Note 6. Input bias currents of a FET–input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

Operating Characteristics: ($V_{CC}\pm$ = ±15V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Slew Rate at Unity Gain	SR	V_I = 10V, R_L = 10kΩ, C_L = 100pF	1.5	3.5	–	V/µs
Rise Time	t_r	V_I = 20mV, R_L = 10kΩ, C_L = 100pF	–	0.2	–	µs
Overshoot Factor			–	10%	–	
Equivalent Input Noise Voltage	V_n	R_S = 100Ω, f = 1kHz	–	42	–	nV/$\sqrt{Hz}$

Pin Connection Diagram