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## NTE937 Integrated Circuit JFET Input Operational Amplifier

### **Description:**

The NTE937 is a monolithic JFET input operational amplifier in an 8-Lead Metal Can type package incorporating well-matched, high voltage JFET's on the same chip with standard bi-polar transistors. This amplifier features low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. It is also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

### **Advantages:**

- Replaces Expensive Hybrid and Module FET OP Amps
- Rugged JFET's Allow Blow-Out Free Handling Compared with MOSFET Input Device
- Excellent for Low Noise Applications using either High or Low Source Impedance – Very Low 1/f Corner
- Offset Adjust does not Degrade Drift or Common-Mode Rejection as in Most Monolithic Amplifiers
- New Output Stage Allows use of Large Capacitive Loads (10,000pF) without Stability Problems
- Internal Compensation and Large Differential Input Voltage Capability

### **Applications:**

- Precision High Speed Integrators
- Fast D/A and A/D Converters
- High Impedance Buffers
- Wideband, Low Noise, Low Drift Amplifiers
- Logarithmic Amplifiers
- Photocell Amplifiers
- Sample and Hold Circuits

### **Absolute Maximum Ratings:**

Supply Voltage .....	±18V
Maximum Power Dissipation (at +25°C, Note 1), P <sub>d</sub> .....	570mW
Differential Input Voltage .....	±30V
Input Voltage Range (Note 2) .....	±16V
Output Short-Circuit Duration .....	Continuous
Maximum Operating Junction Temperature (Note 1), T <sub>Jmax</sub> .....	+115°C
Storage Temperature Range, T <sub>stg</sub> .....	-65° to +150°C
Lead Temperature (During Soldering, 10sec), T <sub>L</sub> .....	+300°C
Thermal Resistance, Junction-to-Ambient (Note 1), R <sub>thJC</sub> .....	+150°C/W

Note 1. The maximum power dissipation for this device must be derated at elevated temperatures and is dictated by T<sub>Jmax</sub>, R<sub>thJC</sub>, and the ambient temperature, T<sub>A</sub>. The maximum available power dissipation at any temperature is P<sub>d</sub> = (T<sub>Jmax</sub> - T<sub>A</sub>)/R<sub>thJC</sub> or the +25°C P<sub>dmax</sub>, whichever is less.

Note 2. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

**DC Electrical Characteristics:** ( $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	$I_{CC}$		–	5	10	mA

**DC Electrical Characteristics:** ( $V_S = \pm 15\text{V}$ ,  $0^\circ \leq T_A \leq +70^\circ\text{C}$ ,  $T_{HIGH} = +70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	$V_{OS}$	$R_S = 50\Omega$ , $T_A = +25^\circ\text{C}$	–	3	10	mV
		Over Temperature	–	–	13	mV
Average TC of Input Offset Voltage	$\Delta V_{OS}/\Delta T$	$R_S = 50\Omega$	–	5	–	$\mu\text{V}/^\circ\text{C}$
Change in Average TC with $V_{OS}$ Adjust	$\Delta\text{TC}/\Delta V_{OS}$	$R_S = 50\Omega$ , Note 3	–	0.5	–	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$I_{OS}$	$T_J = +25^\circ\text{C}$ , Note 4	–	3	50	pA
		$T_J \leq T_{HIGH}$	–	–	2	nA
Input Bias Current	$I_B$	$T_J = +25^\circ\text{C}$ , Note 4	–	30	200	pA
		$T_J \leq T_{HIGH}$	–	–	8	nA
Input Resistance	$R_{IN}$	$T_J = +25^\circ\text{C}$	–	$10^{12}$	–	$\Omega$
Large Signal Voltage Gain	$A_{VOL}$	$T_A = +25^\circ\text{C}$ , $V_O = \pm 10\text{V}$ , $R_L = 2\text{k}$	25	200	–	V/mV
		Over Temperature	15	–	–	V/mV
Output Voltage Swing	$V_O$	$R_L = 10\text{k}$	$\pm 12$	$\pm 13$	–	V
		$R_L = 2\text{k}$	$\pm 10$	$\pm 12$	–	V
Input Common-Mode Voltage Range	$V_{CM}$		$\pm 10$	+15.1 –12	–	V
Common-Mode Rejection Ratio	CMRR		–	80	100	dB
Supply Voltage Rejection Ratio	PSRR	Note 5	–	80	100	dB

Note 3. The temperature coefficient of the adjust input offset voltage changes only a small amount ( $0.5\mu\text{V}/^\circ\text{C}$  typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 4. The input bias currents are junction leakage currents which approximately double for every  $10^\circ\text{C}$  increase in the junction temperature,  $T_J$ . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation,  $P_d$ .  $T_J = T_A + R_{thJC} P_d$  where  $R_{thJC}$  is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

**AC Electrical Characteristics:** ( $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Slew Rate	SR	$A_V = 5$	30	50	–	$\text{V}/\mu\text{s}$	
Gain Bandwidth Product	GBW		–	20	–	MHz	
Settling Time to 0.01%	$t_s$	Note 6	–	1.5	–	$\mu\text{s}$	
Equivalent Input Noise Voltage	$e_N$	$R_S = 100\Omega$	$f = 100\text{Hz}$	–	15	–	$\text{nV}/\sqrt{\text{Hz}}$
			$f = 1000\text{Hz}$	–	12	–	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Current Noise	$i_N$	$f = 100\text{Hz}$	–	0.01	–	$\text{pA}/\sqrt{\text{Hz}}$	
		$f = 1000\text{Hz}$	–	0.01	–	$\text{pA}/\sqrt{\text{Hz}}$	
Input Capacitance	$C_{IN}$		–	3	–	pF	

Note 6.  $A_V = -5$ , the feedback resistor from output to input is  $2\text{k}\Omega$  and the output step is  $10\text{V}$ .

