

OPA177

Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 25 μ V max
- LOW DRIFT: 0.3 μ V/ $^{\circ}$ C
- HIGH OPEN-LOOP GAIN: 130dB min
- LOW QUIESCENT CURRENT: 1.5mA typ
- REPLACES INDUSTRY-STANDARD OP AMPS: OP-07, OP-77, OP-177, AD707, ETC.

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER

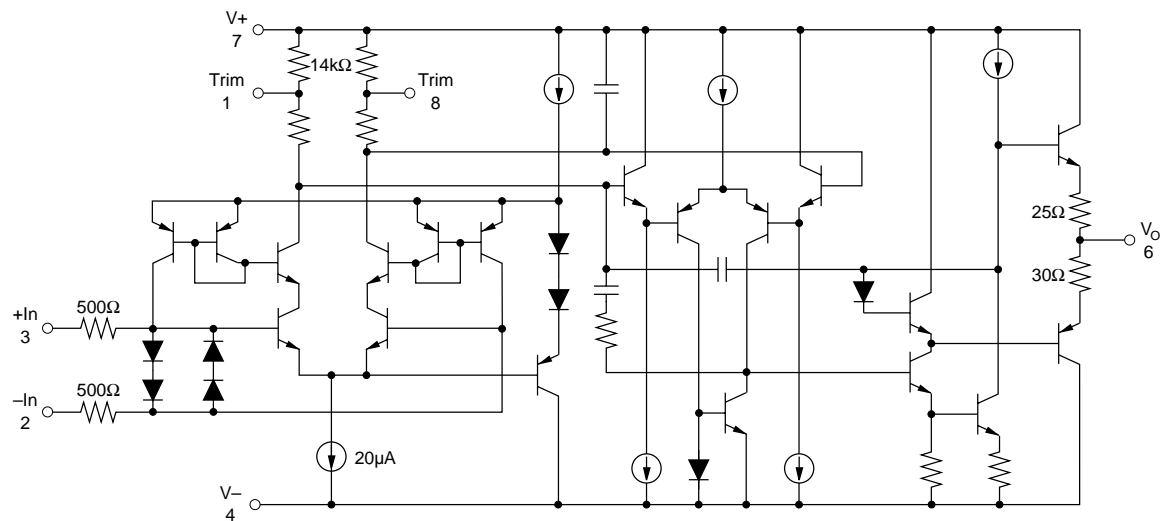
DESCRIPTION

The OPA177 precision bipolar op amp feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. The high performance and low cost make them ideally suited to a wide range of precision instrumentation.

The low quiescent current of the OPA177 dramatically reduce warm-up drift and errors due to thermo-

electric effects in input interconnections. It provides an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 maintains accuracy.

OPA177 performance gradeouts are available. Packaging options include 8-pin plastic DIP and SO-8 surface-mount packages.



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OPA177 SPECIFICATIONS

At $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	CONDITION	OPA177F			OPA177G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage Long-Term Input Offset ⁽¹⁾ Voltage Stability Offset Adjustment Range Power Supply Rejection Ratio	$R_P = 20k\Omega$ $V_S = \pm 3V$ to $\pm 18V$		10 0.3	25		20 0.4	60	μV $\mu V/Mo$ mV dB
INPUT BIAS CURRENT Input Offset Current Input Bias Current			0.3 0.5	1.5 ± 2		* *	2.8 ± 2.8	nA nA
NOISE Input Noise Voltage Input Noise Current	1Hz to 100Hz ⁽²⁾ 1Hz to 100Hz		85 4.5	150		* *	* *	nVrms pArms
INPUT IMPEDANCE Input Resistance	Differential Mode ⁽³⁾ Common-Mode	26	45 200		18.5	* *		M Ω G Ω
INPUT VOLTAGE RANGE Common-Mode Input Range ⁽⁴⁾ Common-Mode Rejection	$V_{CM} = \pm 13V$	± 13 130	± 14 140		* 115	* *		V dB
OPEN-LOOP GAIN Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_O = \pm 10V$ ⁽⁵⁾	5110	12,000		2000	6000		V/mV
OUTPUT Output Voltage Swing Open-Loop Output Resistance	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 13.5 ± 12.5 ± 12	± 14 ± 13 ± 12.5 60		* * *	* * *		V V V Ω
FREQUENCY RESPONSE Slew Rate Closed-Loop Bandwidth	$R_L \geq 2k\Omega$ $G = +1$	0.1 0.4	0.3 0.6		* *	* *		V/ μs MHz
POWER SUPPLY Power Consumption Supply Current	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load $V_S = \pm 15V$, No Load		40 3.5 1.3	60 4.5 2		* * *	* * *	mW mW mA

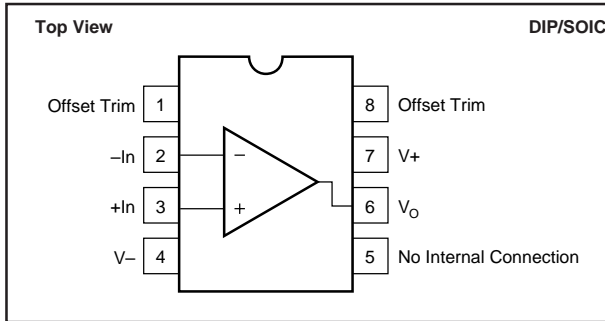
At $V_S = \pm 15V$, $-40^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

OFFSET VOLTAGE Input Offset Voltage Average Input Offset Voltage Drift Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		15 0.1	40 0.3		20 0.7	100 1.2	μV $\mu V/^\circ C$ dB
INPUT BIAS CURRENT Input Offset Current Average Input Offset Current Drift ⁽⁶⁾ Input Bias Current Average Input Bias Current Drift ⁽⁶⁾			0.5 1.5	2.2 40		* *	4.5 85	nA pA/ $^\circ C$ nA pA/ $^\circ C$
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{CM} = \pm 13V$	± 13 120	± 13.5 140		* 110	* *		V dB
OPEN-LOOP GAIN Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	2000	6000		1000	4000		V/mV
OUTPUT Output Voltage Swing	$R_L \geq 2k\Omega$	± 12	± 13		* *	* *		V
POWER SUPPLY Power Consumption Supply Current	$V_S = \pm 15V$, No Load $V_S = \pm 15V$, No Load		60 2	75 25		* *	* *	mW mA

* Same as specification for product to left.

NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than $2\mu V$. (2) Sample tested. (3) Guaranteed by design. (4) Guaranteed by CMRR test condition. (5) To insure high open-loop gain throughout the $\pm 10V$ output range, A_{OL} is tested at $-10V \leq V_O \leq 0V$, $0V \leq V_O \leq +10V$, and $-10V \leq V_O \leq +10V$. (6) Guaranteed by end-point limits.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	±V _S
Output Short Circuit	Continuous
Operating Temperature:	
Plastic DIP (P), SO-8 (S)	-40°C to +85°C
θ _{JA} (PDIP)	100°C/W
θ _{JA} (SOIC)	160°C/W
Storage Temperature:	
Plastic DIP (P), SO-8 (S)	-65°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) P packages	+300°C
(soldering, 3s) S package	+260°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
OPA177FP	8-Pin Plastic DIP	006	-40°C to +85°C
OPA177GP	8-Pin Plastic DIP	006	-40°C to +85°C
OPA177GS	SO-8 Surface-Mount	182	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

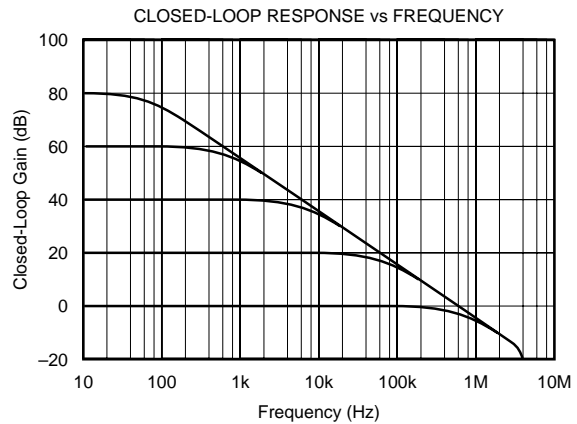
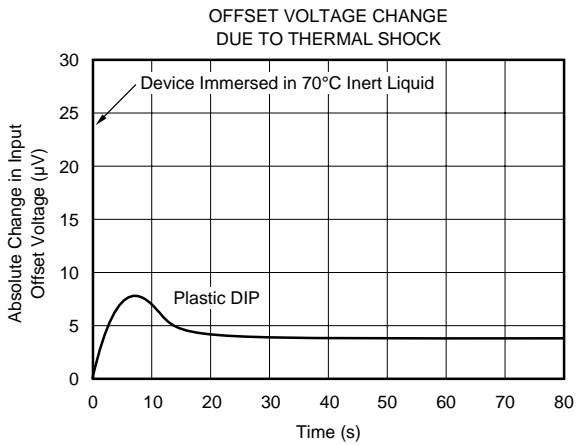
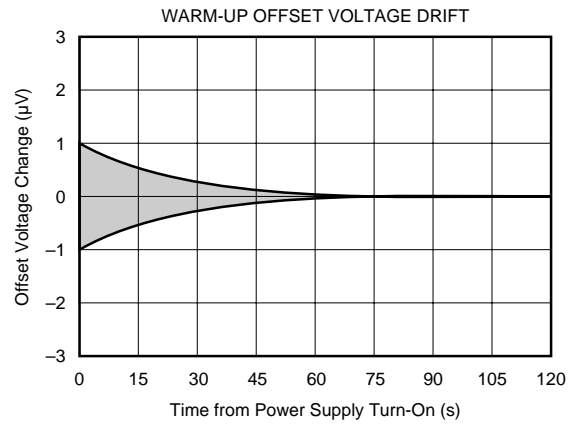
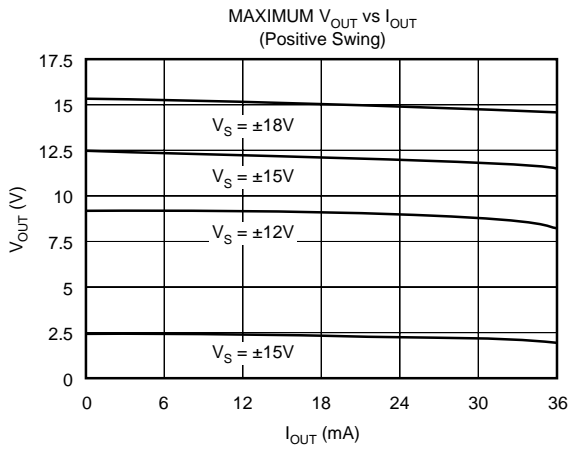
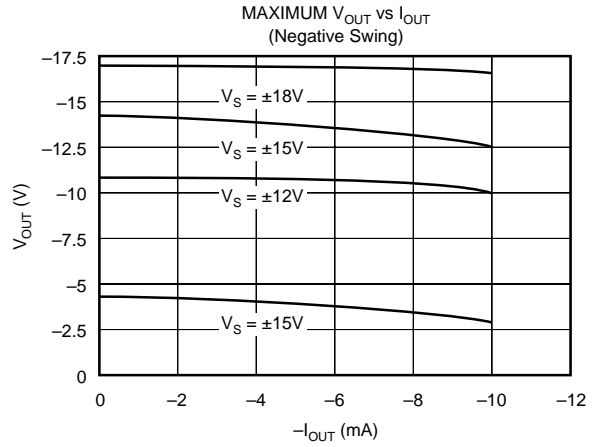
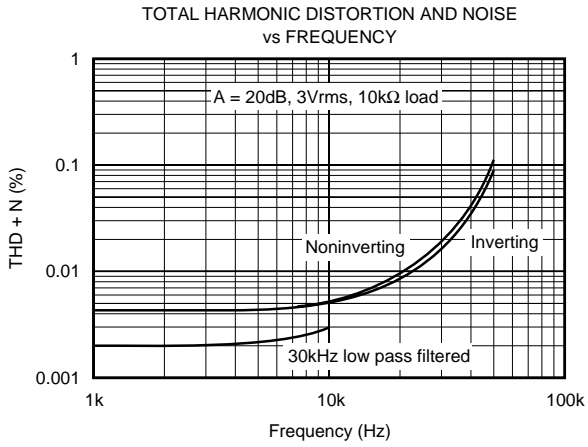
Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.

Failure to observe proper handling procedures could result in small changes to the OPA177's input bias current.

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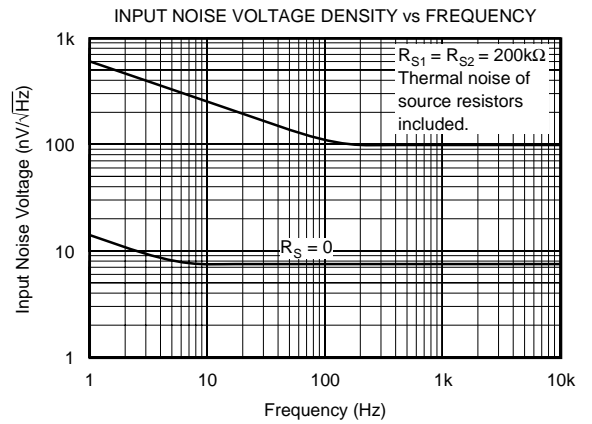
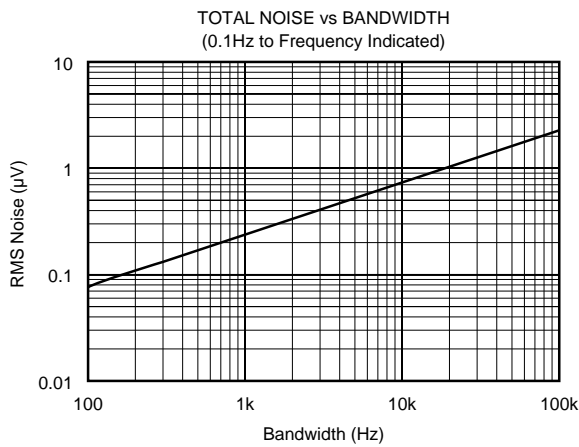
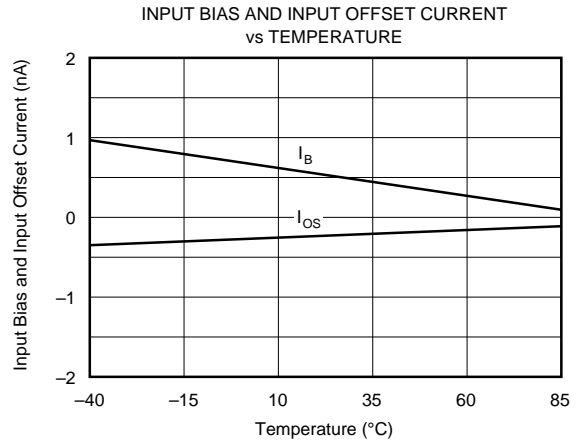
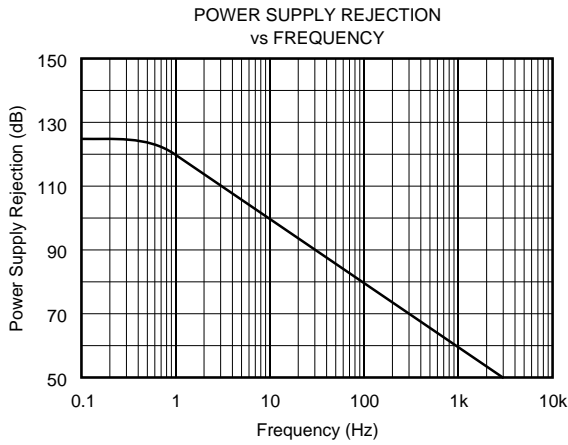
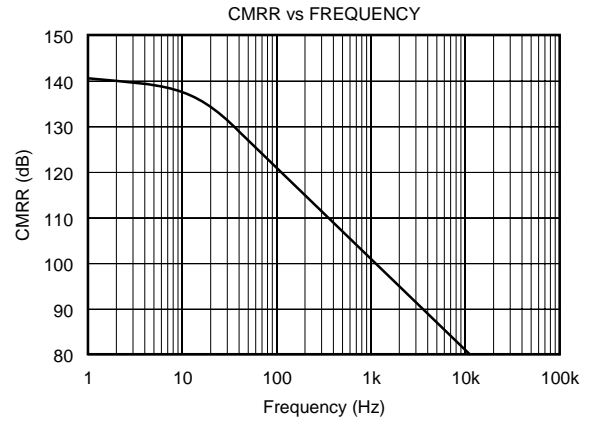
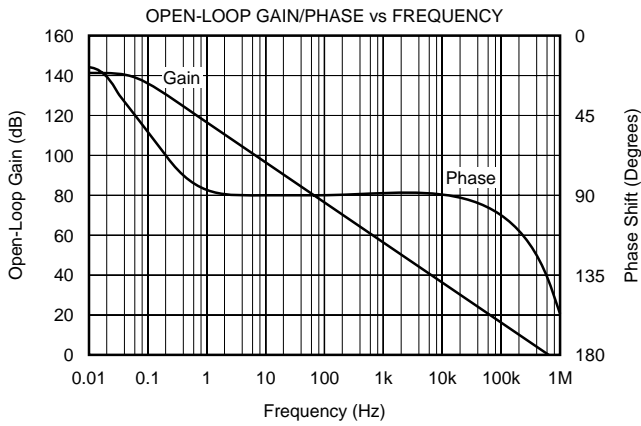
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



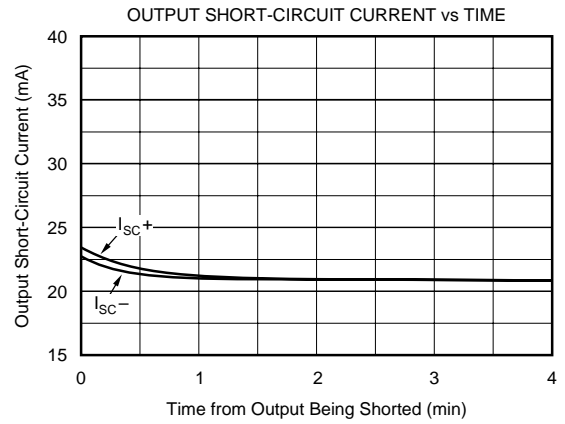
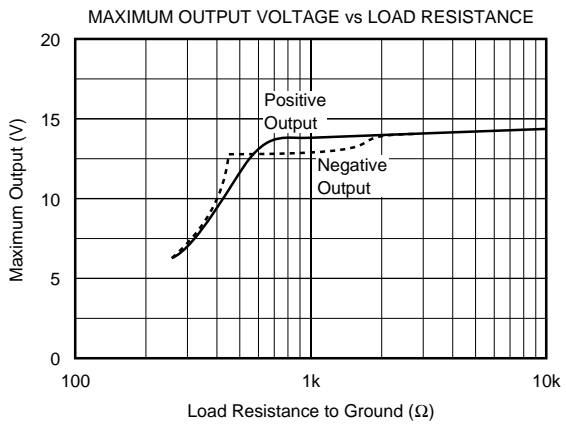
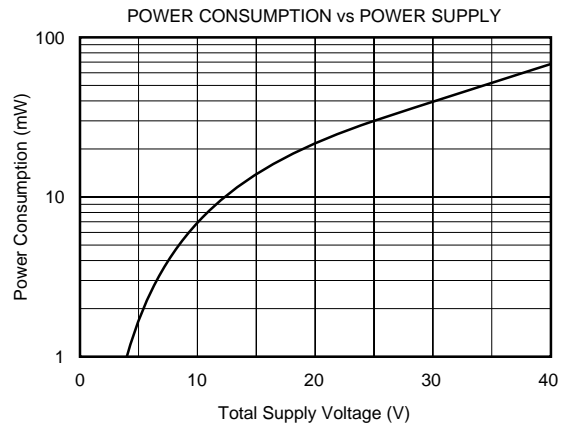
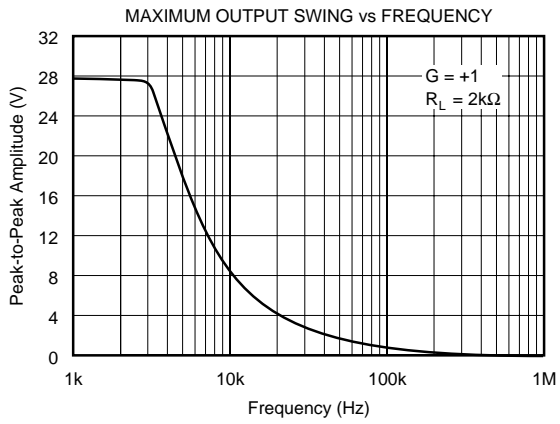
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATIONS INFORMATION

The OPA177 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 0.1 μ F ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions must be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can mask the ultimate performance of the OPA177. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

1. Keep connections made to the two input terminals close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents such as cooling fans.

OFFSET VOLTAGE ADJUSTMENT

The OPA177 has been laser-trimmed for low offset voltage and drift so most circuits will not require external adjustment. Figure 1 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce excessive temperature drift.

INPUT PROTECTION

The inputs of the OPA177 are protected with 500 Ω series input resistors and diode clamps as shown in the simplified circuit diagram. The inputs can withstand ± 30 V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

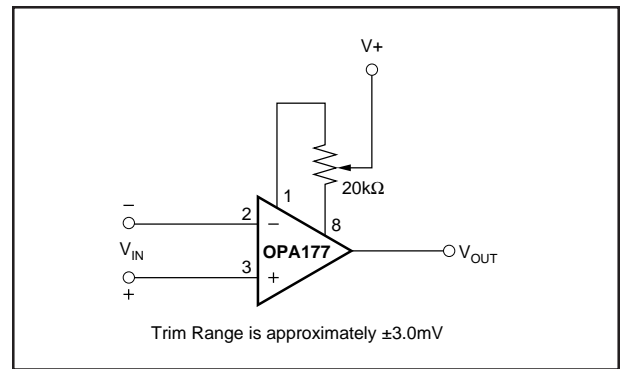


FIGURE 1. Optional Offset Nulling Circuit.

NOISE PERFORMANCE

The noise performance of the OPA177 is optimized for circuit impedances in the range of 2k Ω to 50k Ω . Total noise in an application is a combination of the op amp's input voltage noise and input bias current noise reacting with circuit impedances. For applications with higher source impedance, the OPA627 FET-input op amp will generally provide lower noise. For very low impedance applications, the OPA27 will provide lower noise.

INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to balance the DC resistance seen at the two input terminals (Figure 2). A resistor added to balance the input resistances may actually increase offset and noise.

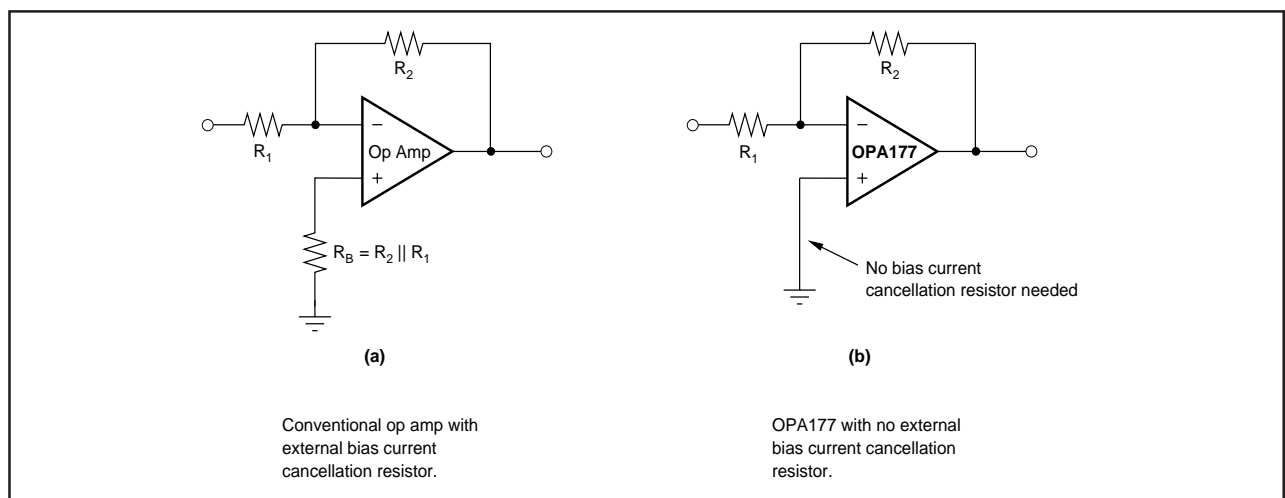


FIGURE 2. Input Bias Current Cancellation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA177FP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA177FP	Samples
OPA177FPG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA177FP	Samples
OPA177GP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA177GP	Samples
OPA177GPG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA177GP	Samples
OPA177GS	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 177GS	Samples
OPA177GS/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 177GS	Samples
OPA177GS/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 177GS	Samples
OPA177GS/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 177GS	Samples
OPA177GSG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 177GS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA177GS/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA177GS/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA177FP	P	PDIP	8	50	506	13.97	11230	4.32
OPA177FP	P	PDIP	8	50	506	13.97	11230	4.32
OPA177FPG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA177FPG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA177GP	P	PDIP	8	50	506	13.97	11230	4.32
OPA177GP	P	PDIP	8	50	506	13.97	11230	4.32
OPA177GPG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA177GPG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA177GS	D	SOIC	8	75	506.6	8	3940	4.32
OPA177GSG4	D	SOIC	8	75	506.6	8	3940	4.32

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