Change Summary

CHANGES

No.	Applicable Section	Description	Page(s)
1	Title	Change the title to read 'Phase-Shift PWM Controller'	1
2	Ordering Information	Add OZ964GN, OZ964IG, OZ964IGN, OZ964D & OZ964DN	1
3	General Description	Add 1st paragraph 'OZ964 is a high…LCD.'	1
4	Functional Block Diagram Description	Add 1st paragraph 1st sentence 'Specific DC/CD…'	5
5	Reference Application Circuit	Add DC/DC Reference Application Circuit	10
6	Package information	Correct 20 Pin SOIC 300mil drawing	12
7	Throughout data sheet	Miscellaneous corrections	---

REVISION HISTORY

Revision No.	Description of change	Release Date
0.95	Initial Release	1/13/2004
0.96	1. Ordering information: add OZ964SN & OZ964ISN. 2. Pin Description: modified pin description of CTIMR, DIM. 3. Electrical Characteristics: revise **a)** 'Nominal Voltage' Typ limit, **b)** 'Normal Operating Frequency' Typ limit, **c)** 'Ramp Peak' Typ limit, **d)** 'Operating Frequency' Typ limit, **e)** 'Negative-Going Threshold Voltage' Max limit, **f)** 'SST Current' Typ limit, **g)** 'CTIMR Current 1' Typ limit, **h)** 'Protection Release Threshold' Typ limit, **i)** 'PDR_A/ PDR_C' Typ`limit, **j)** 'Enable' Min limit, **k)** 'NDR_B/ NDR_D' Typ limit, **l)** 'BBM Time Between PDR and NDR' Typ limit, **m)** 'Minimum Overlap' Typ limit. 4. Simplified Functional Block Diagram. 5. Modified formula in No. 4 Ignition & No. 5 Normal Operation in Functional Information. 6. Revise Application Circuit. 7. Miscellaneous corrections.	3/19/2004
1.0	1. Electrical Characteristics: **a)** Fill in Min & Max limits of all parameters **b)** Correct 'SST Protection Release Threshold' Typ limit. 2. Application Circuit: Correct **a)** C10 to 6.8n, **b)** T1 to 28:2200. 3. Miscellaneous corrections.	4/5/2004
1.1	1. Footer: Add patent number 6,259,615 2. Application circuit: **a.)** Delete R3, R7, R6 & R11. **b)** Change R9 value from 45.3k to 47K	7/29/2004

OZ964

Phase-Shift PWM Controller

FEATURES

- Controller for high-voltage DC/DC and DC/AC converters
- High efficiency, zero-voltage switching
- Supports wide input voltage range
- Constant operating frequency
- Built-in PWM dimming control with wide dimming range
- Soft start function
- Built-in intelligence for ignition and normal operation of CCFLs
- Built-in open-lamp protection and over-voltage protection
- Shutdown delay for input voltage brownout condition
- Built-in under-voltage lockout protection
- Toggle pin to reset the IC after shutdown
- Low stand-by power

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ964S	**0° C to 70° C**	20-pin SSOP
OZ964SN	**0° C to 70° C**	20-pin SSOP, Leadfree
OZ964IS	**-40° C to +85°C**	20-pin SSOP
OZ964ISN	**-40° C to +85°C**	20-pin SSOP, Leadfree
OZ964G	**0° C to 70° C**	20-pin SOIC
OZ964GN	**0° C to 70° C**	20-pin SOIC, Leadfree
OZ964IG	**-40° C to +85°C**	20-pin SOIC
OZ964IGN	**-40° C to +85°C**	20-pin SOIC, Leadfree
OZ964D	**0° C to 70° C**	20-pin PDIP
OZ964DN	**0° C to 70° C**	20-pin PDIP, Leadfree

GENERAL DESCRIPTION

OZ964 is a high efficiency, Pulse Width Modulation (PWM) controller designed for both DC/DC and DC/AC high-voltage applications. The average current mode control is suitable for DC/DC converters where both voltage and current feedback are required, as well as for Cold Cathode Fluorescent Lamp (CCFL)_ backlight applications for small and large Liquid Crystal Displays (LCD).

OZ964 operates in a zero-voltage switching mode that minimizes electromagnetic interference (EMI). In addition, OZ964 achieves a high power-conversion efficiency resulting in a lower operating temperature and higher system reliability.

OZ964 supports a wide input voltage range and provides a constant, user-defined, operating frequency, ensuring that the CCFLs operate at a fixed frequency. This eliminates interference among CCFLs and the LCD panel. Interference causes electromagnetic compatibility (EMC) problems and may create visual effects (waterfall) on LCD panels. The controller provides a phase-shift square wave output that is able to drive a full bridge power train.

OZ964 utilizes a pulse width modulation (PWM) dimming method to achieve a wide dimming range. The IC performs the CCFL dimming function with an analog or low frequency PWM control. The PWM frequency is user-defined.

To avoid over-shoot and in-rush current to the CCFLs during ignition, a soft start function is provided for reliable CCFL operation.

The controller provides open-lamp protection and over-voltage protection, while providing an appropriate response for either open-lamp ignition or removal of a CCFL during normal operation. Intelligent open-lamp protection and over voltage protection provides design flexibility with various transformer characteristics. Open-lamp protection time is user-defined.

In addition, OZ964 provides a shutdown delay function that will keep the inverter module in normal operation for a short period of time if the input voltage suddenly drops and subsequently resumes to a normal level. The shutdown delay time is user-defined.

OZ964 provides under-voltage lockout protection and will disable the IC if VDDA falls below a threshold. OZ964 will resume normal operation when VDDA exceeds the threshold.

To reset the IC, toggle the enable (ENA) pin. OZ964 operates with a standby current of approximately 200uA.

PIN DESCRIPTION

Names	Pin No.	Description
CTIMR	1	Timing capacitor to provide striking time and timing resistor to provide shutdown delay time
OVP	2	Voltage feedback
ENA	3	Enable input
SST	4	Timing capacitor to provide Soft-Start Time
VDDA	5	Supply voltage
GNDA	6	Signal ground
REF	7	Reference voltage output
RT1	8	Timing resistor to provide striking frequency
FB	9	Current sense feedback
CMP	10	Voltage control loop compensation
NDR_D	11	N-MOSFET gate drive output
PDR_C	12	P-MOSFET gate drive output
LPWM	13	Low-frequency PWM signal for dimming control
DIM	14	DC voltage input for LPWM duty cycle
LCT	15	Timing capacitor to provide LPWM frequency
PGND	16	Power MOSFET driver ground
RT	17	Timing resistor to provide striking and operating frequency
CT	18	Timing capacitor to provide striking and operating frequency
PDR_A	19	P-MOSFET gate drive output
NDR_B	20	N-MOSFET gate drive output

ABSOLUTE MAXIMUM RATINGS(1)

VDDA	7.0V
GNDA, PGND	+/- 0.3V
Signal inputs	-0.3V to (VDDA +0.3)V

Operating Temp.	OZ964	OZ964I
	0°C to 70°C	-40°C to +85°C

Operating junction temp.	125 °C
Storage temp.	-55 °C to 150 °C

RECOMMENDED OPERATING RANGE

VDDA	4.6V to 5.5V
f_{OP}- operating frequency	40 kHz to 150kHz(2)
Resistor connected to RT (R_{RT})	20 kΩ to 150 kΩ
Capacitor connected to CT (C_{CT})	100pF to 470pF
f_{LF}- LPWM frequency	100Hz to 500Hz
Thermal Impedance (θ_{J-A}) - 20-pin SSOP - 20-pin SOIC	 80°C/W 105°C/W

Note (1): The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The "Functional Specifications" table will define the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note (2): The frequency of PDR_A, NDR_B, PDR_C, and NDR_D outputs pulses, f_{OP}, is half of fosc value, f_{OP} =(fosc/2).

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions		Limits		Unit
		VDDA=5V; Tamb=25°C;	Min	Typ	Max	
Reference Voltage						
Nominal voltage	Vref	I_{load} = 30μA	3.22	3.35	3.48	V
		Temp coefficient (Tamb=25°C)	-	125	-	ppm/°C
Line regulation	K_L	VDDA=4.6V to 5.5V	-	2	-	mV/V
Load regulation	K_V	I_{load} = 5 μA to 80 μA	-	2	-	mV
Operating Frequency						
Normal Operating Frequency	f_{op}	C_{CT} =220pF(1); R_{RT} =47kΩ(1)	61.5	63.0	65.5	kHz
		Temp coefficient (Tamb=25°C)	-	125	-	ppm/°C
Ramp peak	CT V_{peak}		2.35	2.50	2.65	V
Ramp valley	CT V_{valley}		1.00	1.05	1.12	V
Low Frequency Oscillator						
Operating frequency	f_{LF}	C_{LCT}=6.8nF(2); V_{DIM}=1.2V	209	220	225	Hz
		Temp coefficient (Tamb=25°C)	-	470	-	ppm/°C
Ramp peak	LCT V_{peak}		1.96	2.06	2.18	V
Ramp valley	LCT V_{valley}		0.27	0.31	0.33	V
Duty Cycle Range	LPWM		0	-	100	%
Error Amplifier						
Reference voltage at non-inverting input pin (internal)	V_{ADJ}	V_{SST}=0V	0.49	0.50	0.55	V
		V_{SST}=2V	0.79	0.80	0.81	V
		V_{SST}=4V	1.19	1.24	1.29	V
Under-Voltage Lockout						
Positive-Going Threshold Voltage			4.3	-	-	V
Negative-Going Threshold Voltage			-	-	3.2	V
Supply						
Stand-by Current	I_{OFF}	ENA=low	-	200	300	μA
Supply Current	I_{ON}	DIM=1.2V; LPWM=50kΩ Ca=Cb=Cc=Cd=0.5nF(3) C_{CT} =220pF(1), R_{RT} =47kΩ(1) ;C_{LCT}=6.8nF(2)	-	3.0	4.2	mA
Soft Start						
SST current			4.5	5.5	6.2	μA
		Temp coefficient (Tamb=25°C)	-	420	-	ppm/°C
SST Protection Release Threshold			VDDA -1.25	VDDA -1.0	VDDA -0.93	V
CTIMR						
CTIMR current 1			2.0	2.5	2.9	μA
		Temp coefficient (Tamb=25°C)	-	395	-	ppm/°C
CTIMR current 2			20	30	40	μA
Protection release threshold			2.9	3.1	3.3	V

ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Test Conditions		Limits		Unit
		VDDA=5V; Tamb=25°C;	Min	Typ	Max	
Output Driver Rds(on)						
PDR_A / PDR_C		Sourcing=75mA	12	25	35	Ω
NDR_B / NDR_D		Sinking=75mA	13	25	36	Ω
Enable Thresholds						
Enable			2.3	-	-	V
Disable			-	-	1.0	V
Over-Voltage Protection						
Threshold Voltage	OVP		1.95	2.00	2.20	V
Open-Lamp Protection Threshold						
Open-Lamp Threshold		CMP> open-lamp threshold causes shutdown	2.54	2.70	2.82	V
Break-Before-Make (BBM)						
BBM Time Between PDR and NDR			150	200	220	ns
		Temp coefficient (Tamb=25°C)	-	495	-	ppm/ °C
Maximum / Minimum Duty Cycle						
Maximum Overlap		Vsst = 3.75V ; Vcmp = 3.24V	91	95	-	%
Minimum Overlap		Vsst = 0.8V ; Vcmp = 3.5V	-	2.5	3.9	%

Note (1)
C_{CT}: capacitor from "CT" (Pin 18) to ground
R_{RT}: resistor from "RT" (Pin 17) to ground

Note (2)
C_{LCT}: capacitor from "LCT" (Pin 15) to ground

Note (3)
Ca: capacitor from PDR_A (Pin 19) to VDDA
Cb: capacitor from NDR_B (Pin 20) to ground
Cc: capacitor from PDR_C (Pin 12) to VDDA
Cd: capacitor from NDR_D (Pin 11) to ground

FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

Specific DC/DC applications can be shown with a Reference Application Circuit in Figure 3, page 10. The following discussions will address the OZ964 driving a DC/AC CCFL application. Refer to the Functional Block Diagram in Figure 1, page 6 and the Reference Application Circuit in Figure 2 , page 9. The drive circuit consists of four outputs, PDR_A, NDR_B, PDR_C and NDR_D, (pins 19, 20, 12 and 11) respectively. The drive circuit is designed to achieve high efficiency, zero-voltage switching operation. The four power MOSFET gate output drives, PDR_A, NDR_B, PDR_C and NDR_D are designed such that switches QA/QB and QC/QD never turn-on simultaneously. The configuration prevents any shoot-through issues associated with bridge-type power conversion applications. CCFL current regulation is achieved by adjusting the overlap conduction between diagonal switches QA/QD and QB/QC. The overlap is adjusted when the power source voltage varies.

The Reference Block provides a precision reference voltage for both internal and external uses.

OZ964 is enabled with a voltage greater than 2V applied to ENA (pin 3). A voltage of less than 1V to ENA pin will disable the controller. Toggling ENA (pin 3) from High-Low-High will reset the controller.

Soft-start circuitry provides a gradual increase in power to the drive circuit to power the CCFLs during the ignition period. The Soft-Start Time (SST) is user-defined by an external capacitor connected to SST (pin 4) coupled with an SST current source of 5.5uA.

A High Frequency Oscillator Block generates a user-defined operating frequency determined by an external capacitor (C5) and timing resistor (R9) connected to CT (pin 18) and RT (pin 17) respectively. An external resistor (R10) connected to RT1 (pin 8) in parallel with RT determines the striking frequency.

The current control loop monitors CCFL current that is sensed with a voltage at FB (pin 9). The voltage at FB (pin 9) is input to an Error Amplifier and the output, CMP (pin 10), regulates the CCFL current.

OZ964 provides an Over-Voltage Protection (OVP) function to safely operate the CCFLs under all conditions. The OVP Block regulates the striking voltage for the CCFL during start-up. The striking time is user-defined and determined by an external capacitor connected to CTIMR (pin 1) coupled with the CTIMR current source of 2.6uA.

The Protection Block intelligently monitors and differentiates the striking condition and open-lamp condition. The open-lamp protection function disables the drive circuit if a fault condition is encountered.

A current source of 30uA coupled with an external capacitor and external resistor connected to pin 1 controls the shutdown delay time. The shutdown delay time will keep the inverter module in normal operation for a short period of time if the input voltage suddenly drops and subsequently increases to a normal level. The shutdown delay time is user-defined.

The Under-Voltage Lockout block provides a brown-out period during which the output signals are disabled while the VDDA voltage drops below a ~3.4V threshold. OZ964 resumes normal operation once VDDA voltage reaches a voltage threshold of greater than ~4.3V.

The LPWM Generator Block provides a low frequency PWM (LPWM) function that provides wide dimming control for the CCFLs. The LPWM frequency is user-defined by connecting an external capacitor to LCT (pin 15). An analog voltage at DIM (pin 14) is compared with the LCT waveform that yields a LPWM signal to control the power delivered to the CCFLs.

FUNCTIONAL BLOCK DIAGRAM

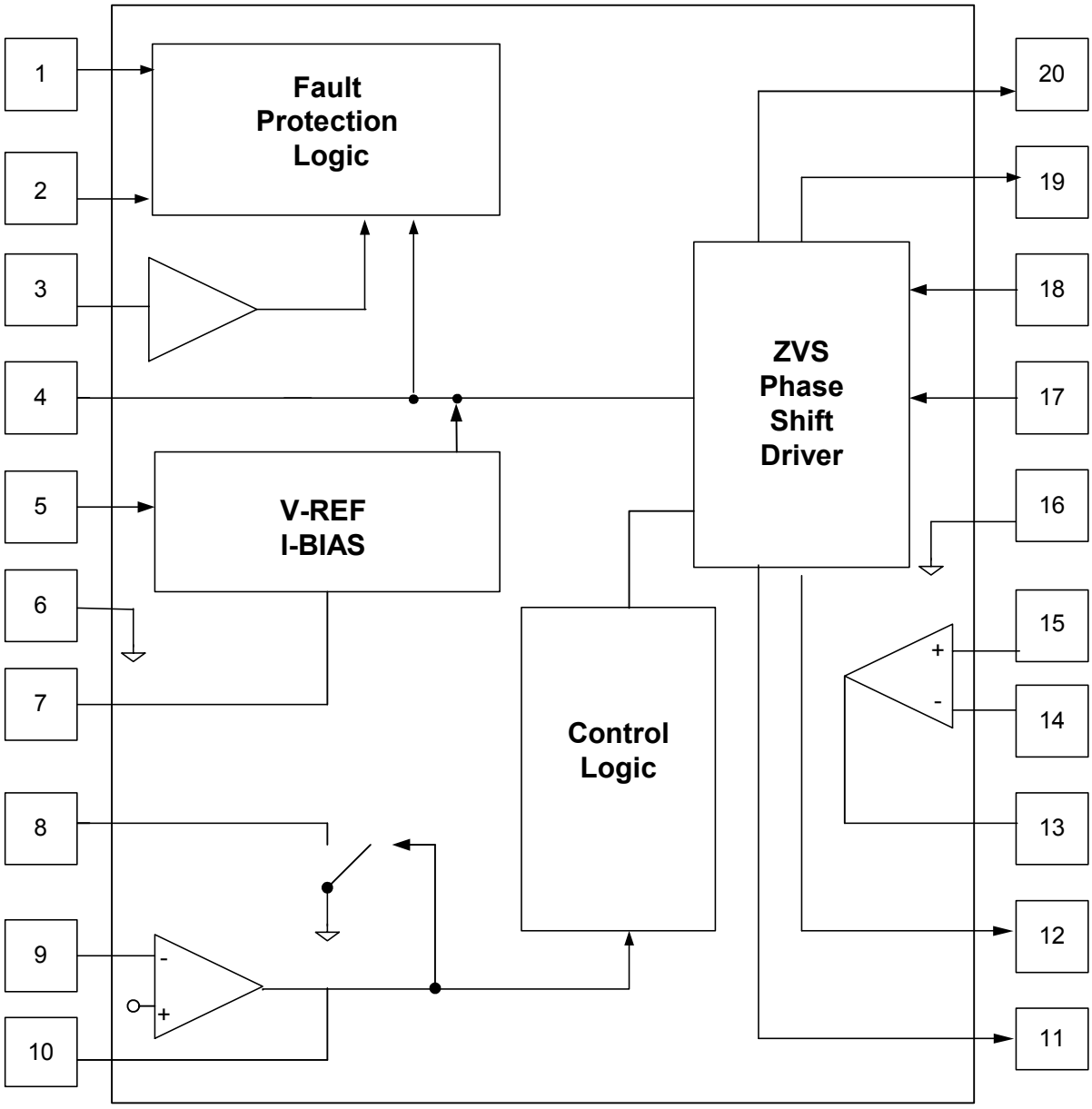


Figure 1

FUNCTIONAL INFORMATION

1. Steady-State Operation

Referring to the example schematic shown in Figure 2, page 9, OZ964 drives a full-bridge power train where the transformer couples the energy from the power supply source to the CCFL. The switches in the bridge denoted as QA, QB, QC and QD are configured such that the transistors in each pair, QA/QB and QC/QD, are turned-on complementarily. The turn-on duration of the diagonal switches, QA/QD and QB/QC, simultaneously determines the amount of energy delivered to the transformer and subsequently to the CCFL. The current in the CCFL is sensed and regulated by adjusting the turn-on time (overlap) for both diagonal switches. This is accomplished through an error amplifier in the current feedback loop.

A voltage loop is used to regulate the output voltage for CCFL ignition and is programmable by using a capacitor divider (C8/C13).

Over Voltage Protection (OVP) limits the transformer voltage under an open-lamp condition. A soft-start circuit ensures a gradual increase in power to the CCFL. The soft-start capacitor (C9) determines the rate of rise of the voltage on the SST pin. Meanwhile, the voltage level determines the turn-on time of the diagonal switches QA/QD and QB/QC.

The output drives for the power MOSFET gates include PDR_A, NDR_B, PDR_C and NDR_D that output a complementary square pulse. The operation of the four switches is implemented with zero-voltage switching that provides a high-efficiency power conversion.

2. Enable

OZ964 is enabled when the voltage on ENA (pin 3) is greater than 2V. A voltage of less than 1V disables the IC. When the inverter controller is disabled, it draws approximately 200uA. An under-voltage lockout protection feature is provided that will disable the IC if VDDA voltage drops below an ~3.4V threshold. The IC will resume normal operation once VDDA reaches a threshold voltage of greater than ~4.3V.

3. Soft-Start

To avoid component stresses and in-rush current to the CCFLs during ignition, a soft start function is implemented to provide reliable CCFL operation. The soft-start function is initiated when the voltage at ENA (pin 3) is greater than 2V. The soft-start time is determined by an external capacitor (C9) connected to the SST (pin 4). At start-up, as C9 charges via a charging current, the voltage level at the capacitor controls the gradual increase in power delivered to the transformer T1.

4. Ignition

The OZ964 provides an option of selecting a different frequency for striking the CCFLs. The striking time is user-defined and determined by an external capacitor C_{CTIMR} (C6) and external resistor R_{CTIMR} (R5) connected to CTIMR (pin 1). The approximate striking time is determined by the following equation.

$$T[\text{second}] = \frac{C_{CTIMR}[\mu F] \times (3-(R_{CTIMR}[k\Omega] \times 0.0026))}{2.6}$$

The approximate striking frequency is determined by the following equation.

$$f_{striking}[kHz] = \frac{65 \bullet 10^4}{C_{CT}[pF] \bullet (R_{RT} // R_{RT1})\ [k\Omega]}$$

Note: $R_{RT} // R_{RT1}$ means R_{RT} is in parallel with $R_{RT.1.}$

5. Normal Operation

Once the IC is enabled, the voltage at SST (pin 4) controls the rate of power delivered to the load. SST voltage increases to a level such that the CCFLs are ignited. The striking frequency is determined by external components R10, R9 and C5 connected to RT1 (pin 8), RT (pin 17) and CT (pin 18) respectively.

Once the external resistor R16 senses sufficient current, the control loop takes control and regulates the CCFL current. The normal operating frequency is determined by the combination of external resistor R9 and external capacitor C5. The operating frequency is approximated by the following equation.

$$f_{op}[kHz] = \frac{65 \bullet 10^4}{C_{CT}[pF] \bullet R_{RT}[k\Omega]}$$

6. Open Lamp Protection

If the controller encounters an open lamp, damaged lamp or lamp removal during normal operation, the control loop generates a protection signal and will immediately shutdown the controller.

OZ964 provides a shutdown delay feature that keeps the inverter module in normal operation if the input voltage suddenly drops and subsequently recovers. The shutdown delay time is user-defined by external resistor R_{CTIMR} (R5) and external capacitor C_{CTIMR} (C6) connected to CTIMR (pin 1).

The shutdown delay time is approximated by the following equation:

$$T[\text{second}] = \frac{C_{CTIMR}[\mu F] \times (3 - (R_{CTIMR}[k\Omega] * 0.03))}{30}$$

Note: R_{CTIMR} (R5) value equal or greater than 110kΩ will result in zero delay time.

Toggling ENA (pin 3) from High-Low-High resets the controller.

7. Over-Voltage Protection & Striking Time

During start-up, once the voltage at the transformer secondary reaches a programmed threshold, the control loop takes over and regulates the voltage at the transformer secondary. SST voltage at pin 4 is held constant and CTIMR is activated to provide additional time to ignite an aged CCFL. If no current is sensed after approximately 1 to 2 seconds, the controller shuts down. Toggling the ENA pin will reset the controller.

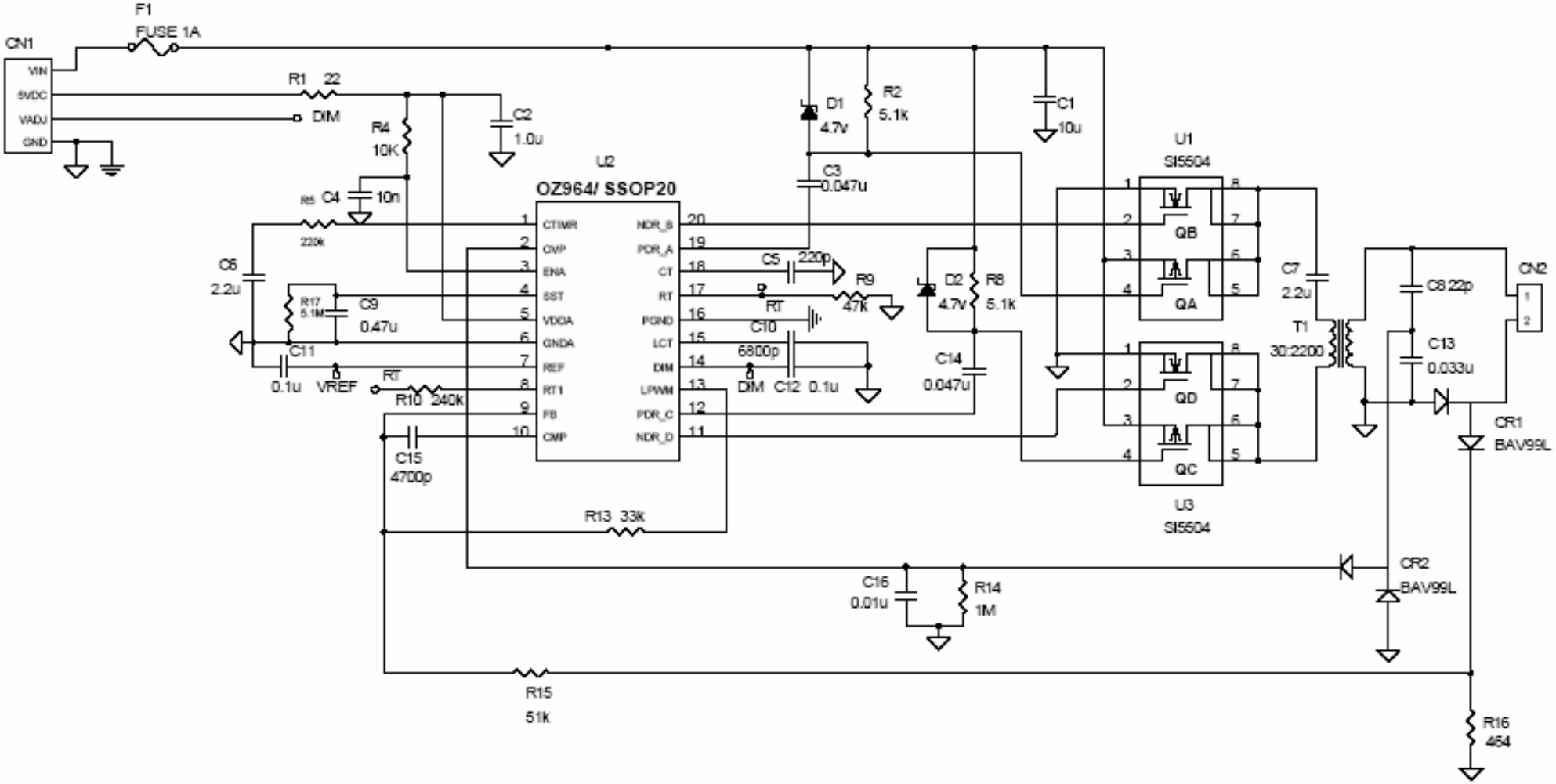
8. PWM Dimming Control

OZ964 provides a low frequency PWM (LPWM) dimming function to perform a wide dimming range of 0% to 100%. The LPWM frequency is determined by external capacitor C10 connected to LCT (pin 15). The frequency is approximated by the following equation.

$$f_{LF}[Hz] = \frac{1496}{C_{LCT}[nF]}$$

The LPWM frequency is user-defined by the selection of external capacitor C10. An analog voltage at DIM (pin 14) is compared with the LCT waveform that yields a LPWM signal to control the power delivered to the CCFLs. The typical peak and valley of the LCT waveform is ~2.06V and ~0.31V respectively.

REFERENCE APPLICATION CIRCUIT



VIN: 8.0V - 22V
VADJ: 2.1V Max. Brightness; 0.6V Min. Brightness
Striking frequency: 75.1KHz
Operating frequency: 63KHz
5VDC: 4.75V – 5.25V

Figure 2

DC/DC REFERENCE APPLICATION CIRCUIT

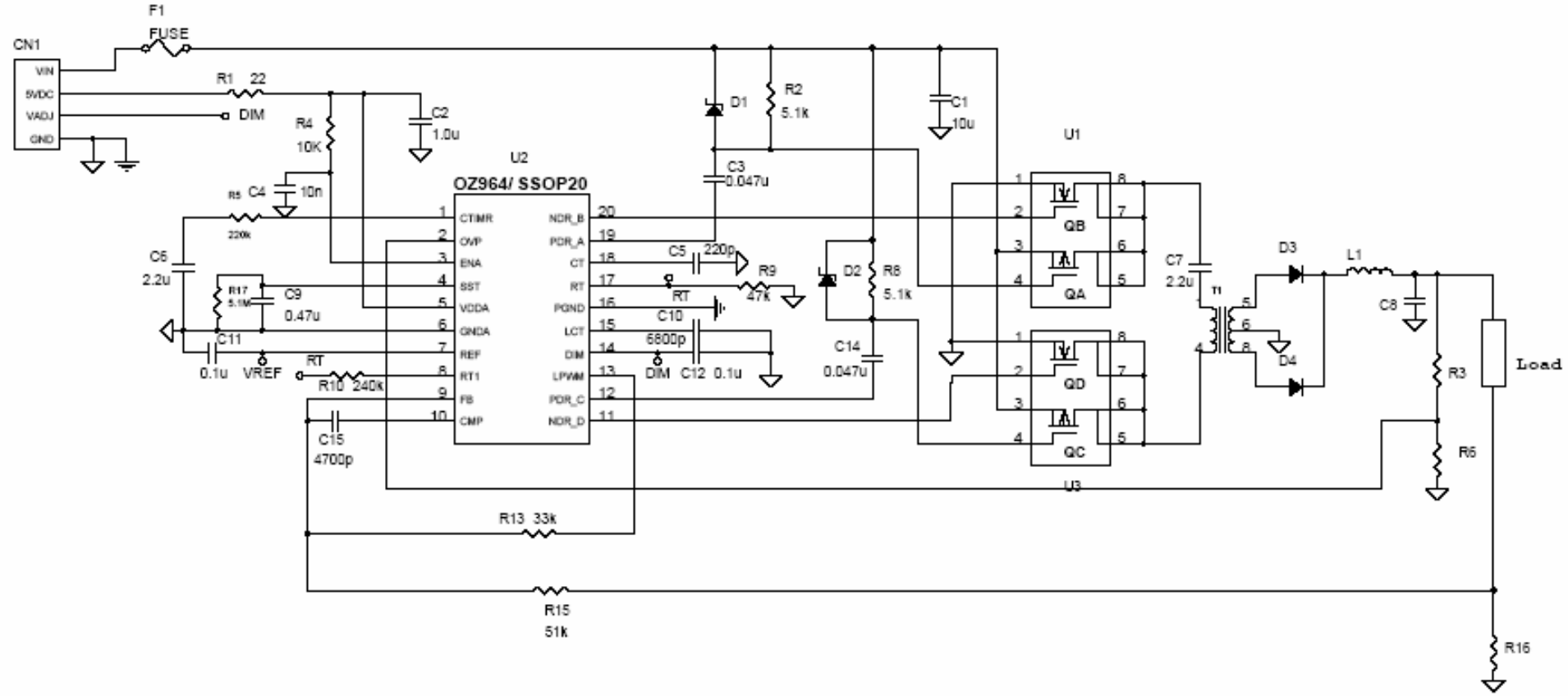
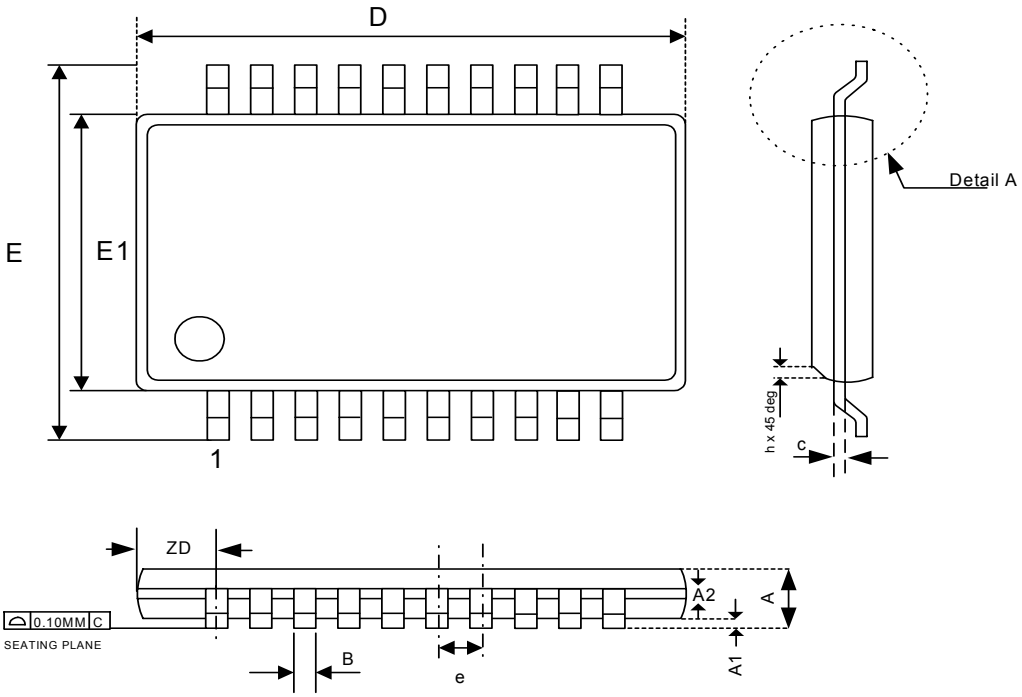
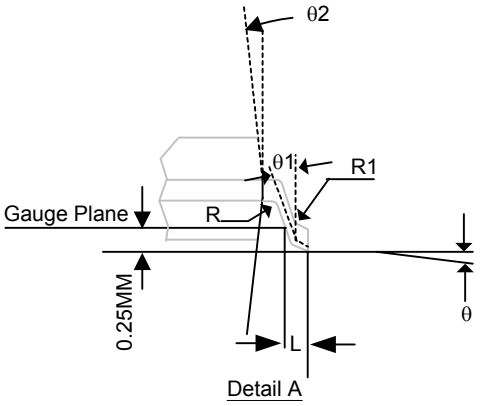


Figure 3

PACKAGE INFORMATION – 20-PIN SSOP 150mil: OZ964S

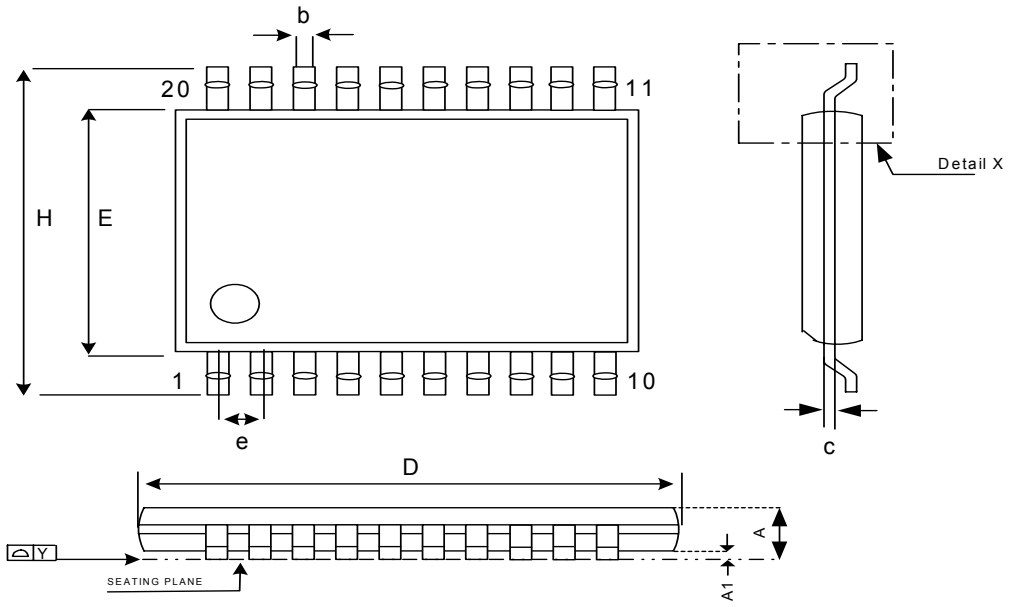


NOTES:
DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 6 MIL PER SIDE

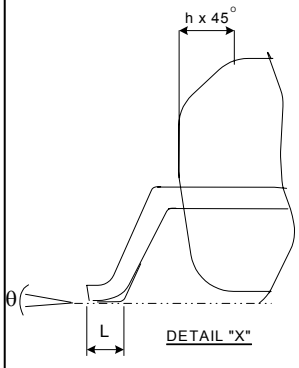


DIM	MILLIMETERS			MIL		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.63	1.75	53	64	69
A1	0.10	0.15	0.25	4	6	10
A2	-	-	1.50	-	-	59
B	0.20	-	0.30	8	-	12
c	0.18	-	0.25	7	-	10
e	0.635 BASIC			25 BASIC		
D	8.56	8.66	8.74	337	341	344
E	5.79	5.99	6.20	228	236	244
E1	3.81	3.91	3.99	150	154	157
L	0.41	0.635	1.27	16	25	50
h	0.25	-	0.50	10	-	20
ZD	1.4732 REF			58 REF		
R1	0.20	-	0.33	8	-	13
R	0.20	-	-	8	-	-
θ	0°	-	8°	0°	-	8°
θ1	0°	-	-	0°	-	-
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AD)					

PACKAGE INFORMATION – 20-PIN SOIC 300mil: OZ964G



NOTES:
1. REFER TO JEDEC STD. MS-013 AC.
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6mil) PER SIDE.
3. DIMENSIONS "E" DOSE NOT INCLUDE INTERLEAD FLASH OR PROTURSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm (10mil) PER SIDE.
4. CONTROLLING DIMENSION: MILLIMETER



SYMBOL	MILLIMETERS			MIL		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.36	2.54	2.64	93	100	104
A1	0.10	0.20	0.30	4	8	12
b	0.35	0.406	0.48	14	16	19
c	0.23	0.254	0.31	9	10	12
D	12.60	12.80	13.00	496	504	512
E	7.40	7.50	7.60	291	295	299
e	1.27 BSC			50 BSC		
H	10.00	10.31	10.65	394	406	419
h	0.25	0.66	0.75	10	26	30
L	0.51	0.76	1.02	20	30	40
Y	-	-	0.075	-	-	3
θ	0°	-	8°	0°	-	8°

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