Change Summary

CHANGES

No.	Applicable Section	Description	Page(s)
1.	Application Circuit Figs. 2 & 3	Add reference note.	3, 4
2.	Functional Specifications	Correct a) 'Operating Frequency on DRV1 & 2 Pin' Min., Typ. and Max. limits, b) 'LPWM Frequency' Min. and Typ. limits, c) 'Ignition Time' parameter title, and d) 'Lamp Current Reference' parameter title and unit.	6
3.	Functional Description, 4.	Last sentence, add "CT" pin number.	7
4.	Functional Description, 5.	Last sentence, add "pin 2" name, and correct formula.	7
5.	Functional Description, 8.	4th line, correct to read "....voltage at the CCFL for **approximately two seconds.**"	7
6.	Functional Description, 9.	3rd paragraph, 5th line, correct to read "....is set by external capacitors C9 **and C11 connected to CT (Pin 2)**", deleting "...CT (Pin 2)" from the following sentence.	7, 8
7.	Functional Description, 9.	4th paragraph, correct formula and add last sentence.	8
8.	Throughout data sheet	Miscellaneous corrections.	---

REVISION HISTORY

Revision No.	Description of change	Release Date
0.90	Initial release	03/27/03

DEVIN LAI

OZ9RR

LCD Monitor CCFL Inverter Controller

FEATURES

- Low cost LCD monitor inverter solution
- Constant operating frequency
- Operating frequency can be synchronized with external signal
- Integrated synchronized PWM dimming control with wide dimming range
- Built-in intelligence for ignition and normal operation of CCFLs
- Built-in open-lamp protection and over-voltage protection
- Optimized soft-start function
- Higher reliability and longer life
- Supports multiple CCFLs
- Minimum external components

ORDERING INFORMATION

OZ9RRG – 8 pin plastic SOIC
OZ9RRD – 8 pin plastic DIP

GENERAL DESCRIPTION

The patent pending OZ9RR is a cost-effective CCFL (Cold Cathode Fluorescent Lamp) Power Management controller designed for multiple CCFL LCDM (Liquid Crystal Display Monitor) applications.

OZ9RR operates at a constant operating frequency. The operating frequency can be synchronized with an external signal that eliminates any undesired interference between the controller and LCD panel.

The controller provides a wide dimming range control with a low-frequency Pulse Width Modulation (LPWM) dimming function. The control logic provides a regulated ignition voltage and appropriate protection for over-voltage or over-current conditions.

The OZ9RR offers a high level of integration, while maintaining flexibility and high-efficiency operation that reduces component heating. This results in higher reliability and longer CCFL life. The proprietary (patent pending) design technique provides a simpler, lower-cost system solution.

Operating in a zero-voltage switching, push-pull topology, the OZ9RR achieves high power conversion efficiency. The highly integrated controller encompasses current and voltage regulation, soft-start operation, over-voltage protection and an external enabling function while maintaining a high-degree of design flexibility. The application requires a minimum number of off-the-shelf components.

The CCFL backlight controller is designed for a wide range of input voltages. It provides a wide dimming range by converting an external analog control input into a built-in LPWM dimming function. The controller converts unregulated DC voltages into a nearly sinusoidal lamp voltage and current waveforms.

The OZ9RR is available in 8-pin SOIC and 8-pin PDIP packages.

OZ9RR is specified over the commercial temperature range from 0°C to 70°C.

Figure 1. OZ9RR Functional Block Diagram

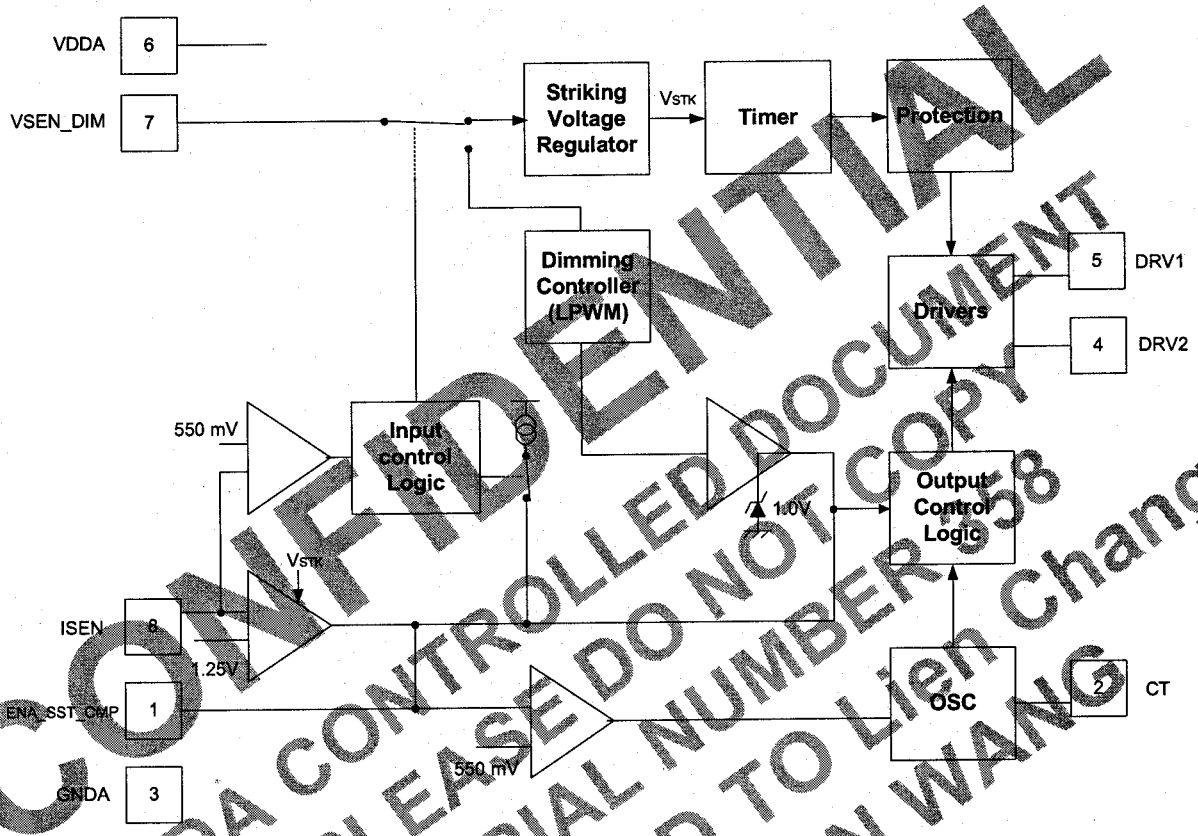
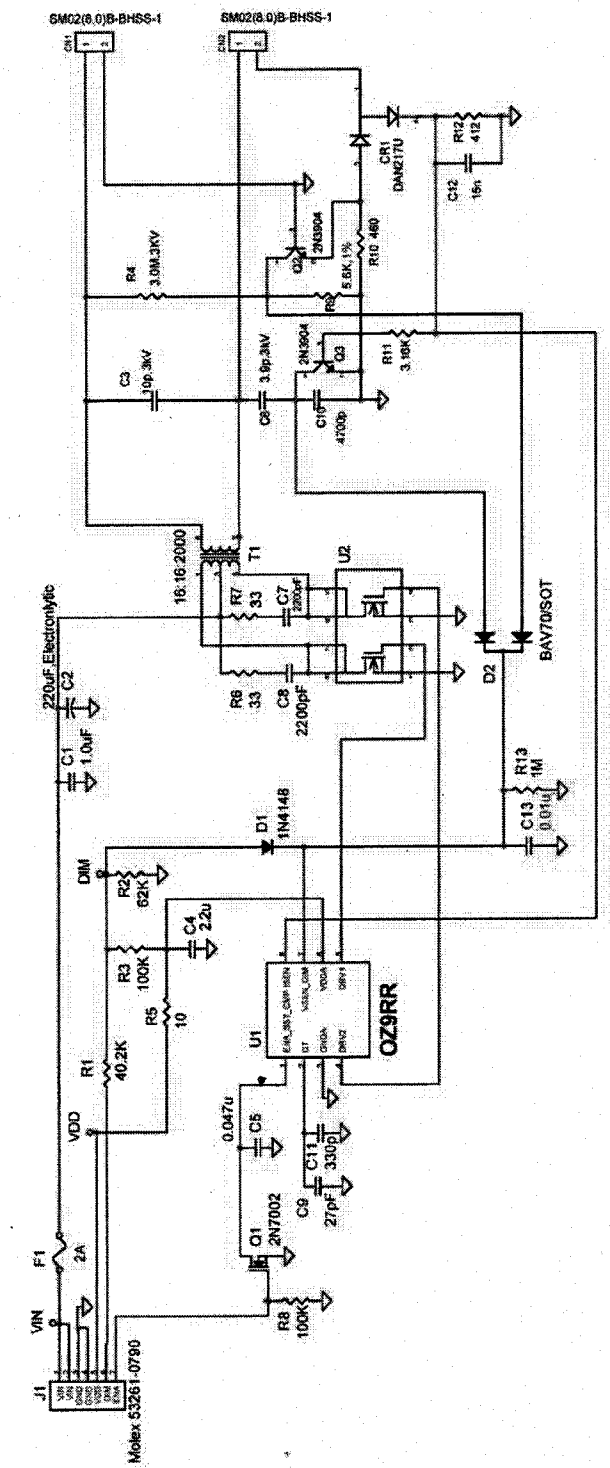


Figure 2. OZ9RR Typical Application Circuit: Separate Ground

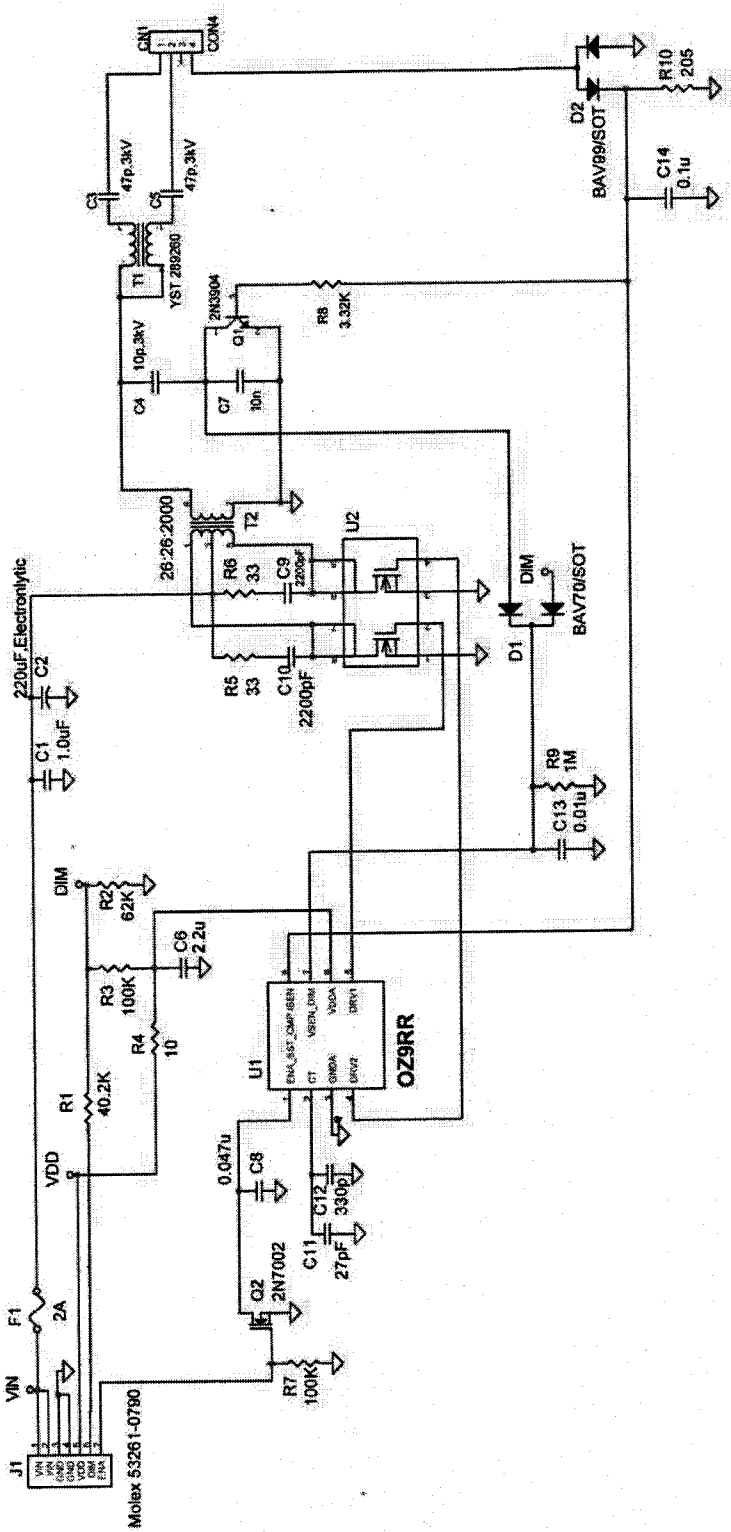


VIN : 10.8V -13.2v
VDD : 4.75V---5.25V
ENA : 0V---1V, enable; 3V---5V, disable
DIM: 0.5V Min. Brightness; 3.6V Max. Brightness

Note: Each CCFL has its individual ground

Refer to: OZ9RR PCB Layout Design Guideline

Figure 3. OZ9RR Typical Application Circuit: Common Ground



VIN : 10.8V ~ 13.2V
VDD : 4.75V~5.25V
ENA : 0V~1V, enable; 3V~5V, disable
DIM: 0V Min. Brightness; 4.3V Max. Brightness

Note: Both CCFLs' ground wires are common

Refer to: OZ9RR PCB Layout Design Guideline

OZ9RR PIN DESCRIPTION

Names	Pin No.	I/O	Description
ENA_SST_CMP	1	I/O	Enable, Soft Start Time and Compensation of Current Error Amplifier
CT	2	I/O	Timing Capacitor to Set Operating Frequency
GNDA	3		Ground
DRV2	4	O	N MOSFET Drive Output
DRV1	5	O	N MOSFET Drive Output
VDDA	6		Supply Voltage Input
VSEN_DIM	7	I	Voltage Sense_ Input Analog Signal for PWM Dimming Control
ISEN	8	I	Lamp Current Detection & Control

ABSOLUTE MAXIMUM RATINGS WITH RESPECT TO INPUT POWER SOURCE RETURN REFERENCE

Input Voltage VDDA	7.0V[(1)]
GNDA	+/- 0.3V
Logic inputs	-0.3V to VDDA +0.3V

Operating temp.	0°C to +70 °C
Operating junction temp.	125 °C
Storage temp.	-55 °C to 150 °C

RECOMMENDED OPERATING RANGE

Input Voltage	4.5V to 5.5V
f_{op}	30KHz to 150KHz

Note [(1)]: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The "Functional Specifications" table will define the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

FUNCTIONAL SPECIFICATION

Parameter	Symbol	Test Conditions		Limits		Unit
		VDDA=5V; C_T=357pF; C_{SST}=12.1nF; Tamb=25°C unless otherwise specified	Min	Typ	Max	
Supply Current						
Stand By	I_{dds}	V_1=0V; V_8=0V	-	350	470	µA
Operating	I_{dd}	V_1=2V; V_8=0V	-	3.9	6.0	mA
Soft Start Current Source	I_{SST}	V_1=0V; V_8=0V; V_7=0V	2.4	3.0	3.5	µA
Under Voltage Lockout	UVLO	V_1=1V; VDDA from 0V to 5V	3.2	3.8	4.2	V
ENA_SST_CMP Pin - Low	V_{CMP}		0.96	1.07	1.10	V
CT Pin Peak Valley						
CT Pin Peak	Vpeak	V_1=2V; V_8=660mV; V_7=2.8V	2.90	3.06	3.20	V
CT Pin Valley	Vvalley	V_1=2V; V_8=660mV; V_7=2.8V	0.95	1.02	1.15	V
Operating Frequency on DRV1 & DRV2 Pin	fop	V_1=1.2V; V_8=660mV; V_7=2.8V	44.0	48.5	53.0	kHz
LPWM Frequency	f_{LF}	V_1=1.2V; V_8=660mV; V_7=1.5V	190	210	231	Hz
Dimming						
Minimum Brightness	VSEN_DIM	Typical 10%		-	0.22	V
Maximum Brightness	VSEN_DIM		2.39	-	-	V
Pulse Width on DRV1 & DRV2 (active high)						
Minimum		V_1=0.8V; V_8=0V; V_7=0V	0.1	0.2	0.3	µsec
Maximum		V_1=3V; V_8=0V; V_7=0V	6.6	6.8	7.0	µsec
Over Voltage Protection Threshold	OVP (V_7)	V_1=1.5V; V_8=0V	2.90	3.10	3.25	V
Open Lamp Protection Threshold	OPLAMP (V_1)	V_8=0V; V_7=0V	3.4	3.8	4.2	V
Ignition Time (Open Lamp Time Out)		V_8=0V; V_7=0V	1.7	2.0	2.3	sec
Lamp Current Reference Voltage	ISEN		1.19	1.25	1.31	V
V_1 (ENA_SST_CMP Pin) Threshold			500	550	600	mV
Drivers						
DRV1	Ron	For Iout= 70 mA	10	18	26	Ω
DRV2	Ron	For Iout= 70 mA	10	18	26	Ω

Note: Parameters, symbol and test conditions columns, V_x=$V_{PIN\ NUMBER}$

FUNCTIONAL DESCRIPTION

1. Power Conversion

The power train uses a zero voltage switching push-pull topology to provide symmetrical drive pulses to the tank circuit that includes the transformer(s), output capacitors and the CCFL/panel load, to yield quasi-sinusoidal CCFL voltage and current waveforms. High-efficiency operation of the OZ9RR yields lower heat dissipation for the inverter system resulting in higher reliability.

OZ9RR controller provides a low system cost.

Refer to Figures 1 and 2 on pages 2 and 3, respectively for the following sections.

2. Enable

The OZ9RR is enabled when the voltage on Pin 1 is greater than 0.55V.

3. Soft Start (SST)

Connecting an external capacitor to Pin 1 provides the SST function. A charging current is provided to capacitor C5. At Start-up, as capacitor C5 charges, the voltage level controls the gradual increase in power to the transformer. This reduces in-rush current and provides reliable operation to the CCFL.

4. Ignition

The ignition process requires a higher striking frequency to strike the CCFL. The striking frequency is approximately 1.3 times the normal operating frequency. The striking frequency is determined by CT (Pin 2) external capacitors, C9 and C11.

5. Normal Operation

Once the CCFL is ignited and current is sensed at Pin 8 (ISEN), the control loop regulates the CCFL current. The operating frequency is determined by the external capacitors C_T(C9 & C11) at CT (Pin 2), where the approximate operating frequency is calculated by the following equation.

$$f_{op} = \frac{19 \times 10^3}{1.1 \times C_T\ [pF]} \quad [kHz]$$

6. Over-Voltage Protection

The control logic protects the transformer from an abnormal high voltage at the secondary output.

During start up, VSEN_DIM (Pin 7) senses the voltage on the transformer secondary. When VSEN reaches 3V, the output voltage is regulated. An internal timer is activated to provide sufficient time for CCFL ignition. If no current is sensed after approximately 2.0 seconds, the OZ9RR shuts off. Toggling the enable signal from low to high will resume normal operation.

7. Open Lamp Protection

When a CCFL is removed or damaged during normal operation, the OZ9RR shuts off the output drives. When the damaged lamp is replaced, toggling the enable pin from low to high resumes normal operation.

8. Aged CCFL Ignition

During the ignition process, the controller senses the voltage at the CCFL. For an open-circuit condition, the power train delivers a regulated voltage at the CCFL for approximately two seconds. This is to ensure that any aged, slow-turn-on CCFL is provided with sufficient voltage and time to ignite.

9. Dimming Control

The OZ9RR internal LPWM dimming control circuitry provides a wide low-frequency dimming range. The input to Pin 7 (VSEN_DIM) is an analog voltage of 0.2V to 2.3V that produces a LPWM duty cycle of 10% to 100%.

The output of the LPWM signal has a duty cycle proportional to the input dimming signal command (VDIM). A resistive network (R1, R2 and R3) is inserted between the external dimming input and Pin 7 to provide user flexibility for different dimming input voltage ranges, such as 0V to 3V or 0V to 5V.

A wide dimming range is achieved by utilizing LPWM control method, via the low-frequency PWM generator circuitry. OZ9RR operates in a constant frequency mode, in which the frequency is set by external capacitors C9 and C11 connected to CT (Pin 2). The operating frequency

and LPWM frequency are internally synchronized. The operating frequency can also be synchronized to the LCD monitor system by providing an external signal to pin 2. This eliminates any undesired interference between the controller and LCD panel, as the interference is usually associated with variable-frequency design. Interference may result in a poor user experience because of "waterfall" display distortion and other poor display appearance.

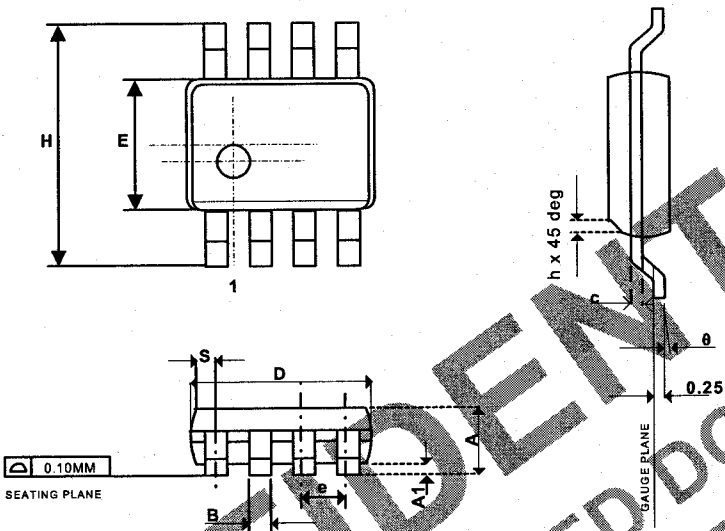
The approximate dimming frequency (low frequency) is internally generated and calculated using the following equation:

$$f_{LF} = \frac{75 \times 10^3}{C_T\,[pF]}\,[Hz]$$

Please contact your local field office for implementation details.

PACKAGE INFORMATION

8-PIN SOIC

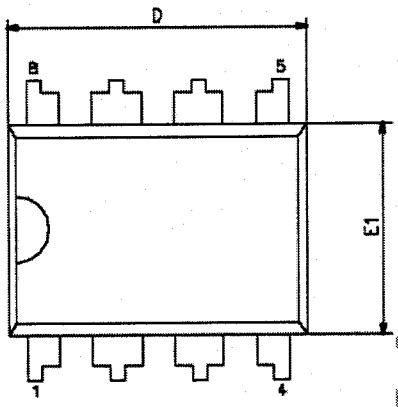


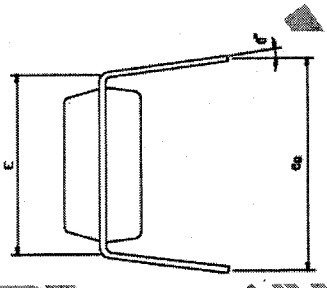
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
c	0.008	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050 BSC.		1.27 BSC.	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
S	0.0155	0.0255	0.394	0.648
θ	0°	8°	0°	8°
D	-	-	4.80	5.00
JEDEC	MS-012AA			

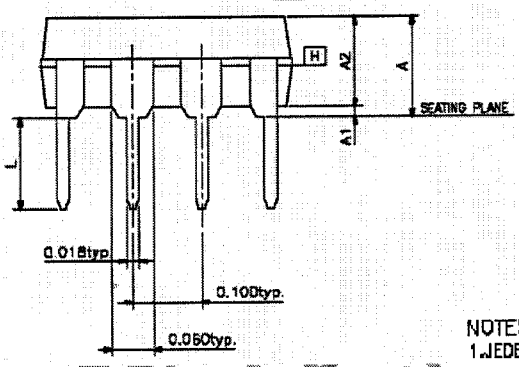
Notes:
1. Controlling dimensions are in millimeter (mm).
2. Pin #1 count orientation shall be at counterclockwise direction as viewed in live-bug position.

PACKAGE INFORMATION

8-PIN DIP







SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

NOTES:
1. JEDEC OUTLINE : MS-001 BA
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

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