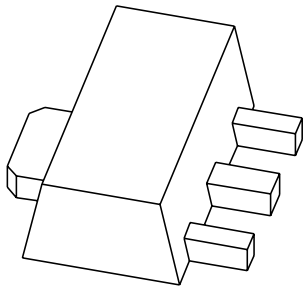


# DATA SHEET



**PBSS5350X**

50 V, 3 A

PNP low  $V_{CEsat}$  (BISS) transistor

Product data sheet  
Supersedes data of 2003 Nov 21

2004 Nov 04

**50 V, 3 A**  
**PNP low  $V_{CEsat}$  (BISS) transistor**

**PBSS5350X**

**FEATURES**

- SOT89 (SC-62) package
- Low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability:  $I_C$  and  $I_{CM}$
- Higher efficiency leading to less heat generation
- Reduced printed-circuit board requirements.

**APPLICATIONS**

- Power management
  - DC/DC converters
  - Supply line switching
  - Battery charger
  - LCD backlighting.
- Peripheral drivers
  - Driver in low supply voltage applications (e.g. lamps and LEDs).
  - Inductive load driver (e.g. relays, buzzers and motors).

**DESCRIPTION**

PNP low  $V_{CEsat}$  transistor in a SOT89 plastic package.  
 NPN complement: PBSS4350X.

**MARKING**

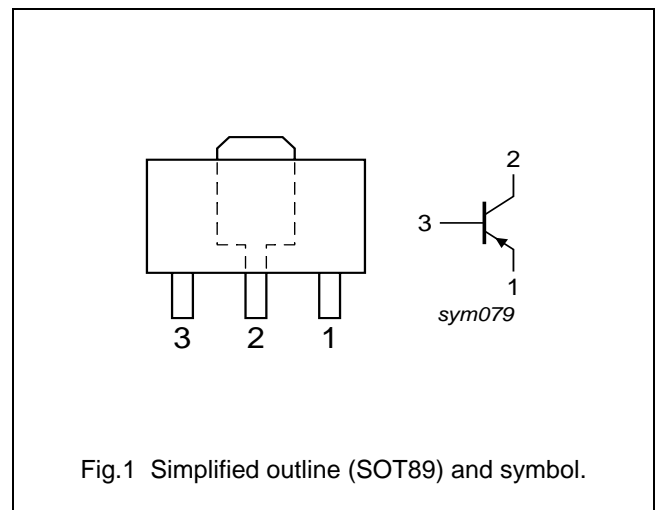
TYPE NUMBER	MARKING CODE
PBSS5350X	S46

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
$V_{CEO}$	collector-emitter voltage	-50	V
$I_C$	collector current (DC)	-3	A
$I_{CM}$	peak collector current	-5	A
$R_{CEsat}$	equivalent on-resistance	135	m $\Omega$

**PINNING**

PIN	DESCRIPTION
1	emitter
2	collector
3	base



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**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS5350X	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

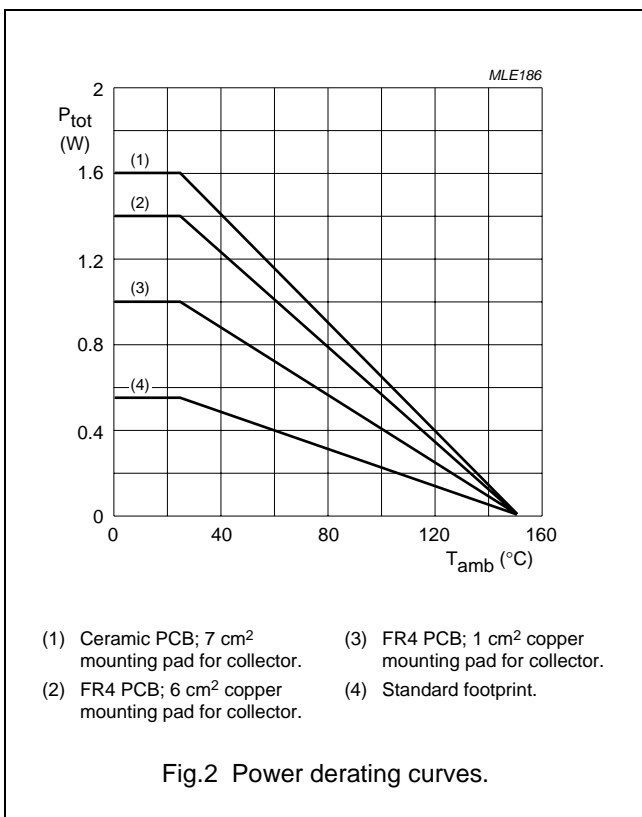
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–50	V
$V_{CEO}$	collector-emitter voltage	open base	–	–50	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)	note 4	–	–3	A
$I_{CM}$	peak collector current	limited by $T_{j(max)}$	–	–5	A
$I_B$	base current (DC)		–	–0.5	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ note 1 note 2 note 3 note 4	–	550 1 1.4 1.6	mW W W W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	ambient temperature		–65	+150	°C

**Notes**

1. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; standard footprint.
2. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; mounting pad for collector 1 cm<sup>2</sup>.
3. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; mounting pad for collector 6 cm<sup>2</sup>.
4. Device mounted on a ceramic printed-circuit board 7 cm<sup>2</sup>, single-sided copper, tin-plated.

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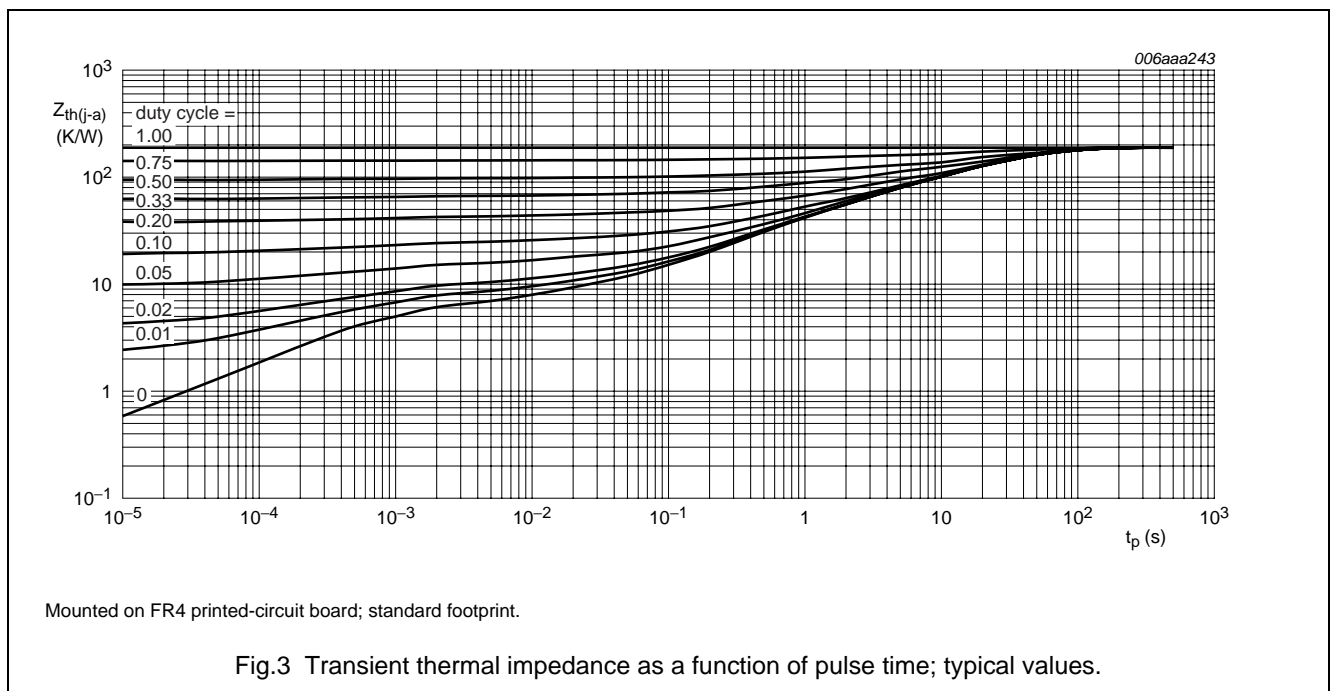
PBSS5350X

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		note 1	225	K/W
		note 2	125	K/W
		note 3	90	K/W
		note 4	80	K/W
$R_{th(j-s)}$	thermal resistance from junction to soldering point		16	K/W

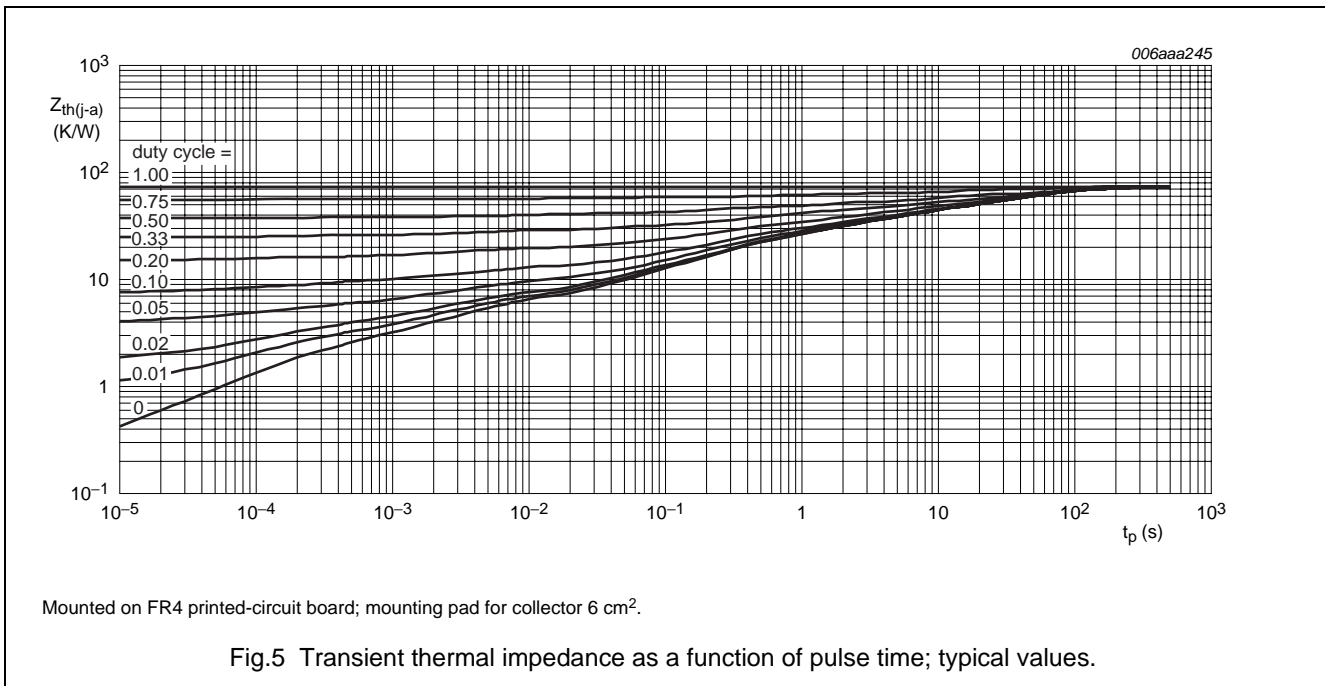
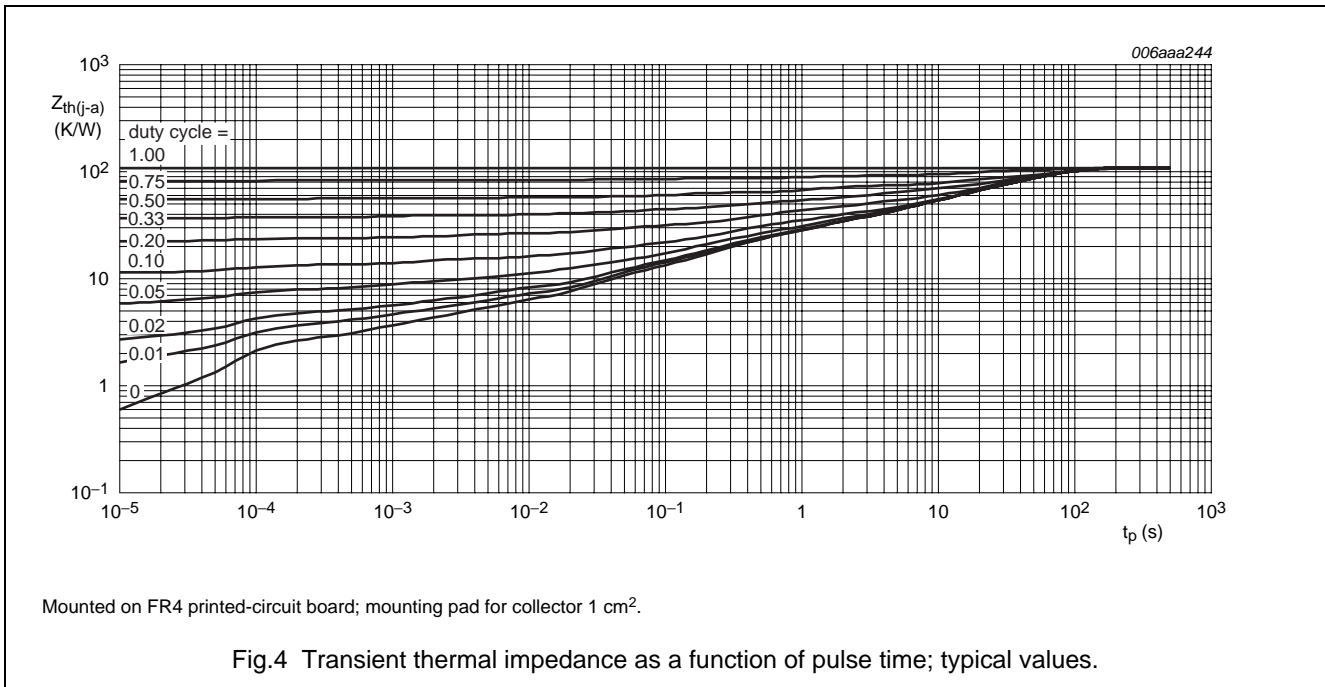
**Notes**

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2. Device mounted on a FR4 printed-circuit board; single-sided copper; tin-plated; mounting pad for collector 1 cm<sup>2</sup>.
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**PBSS5350X**

**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

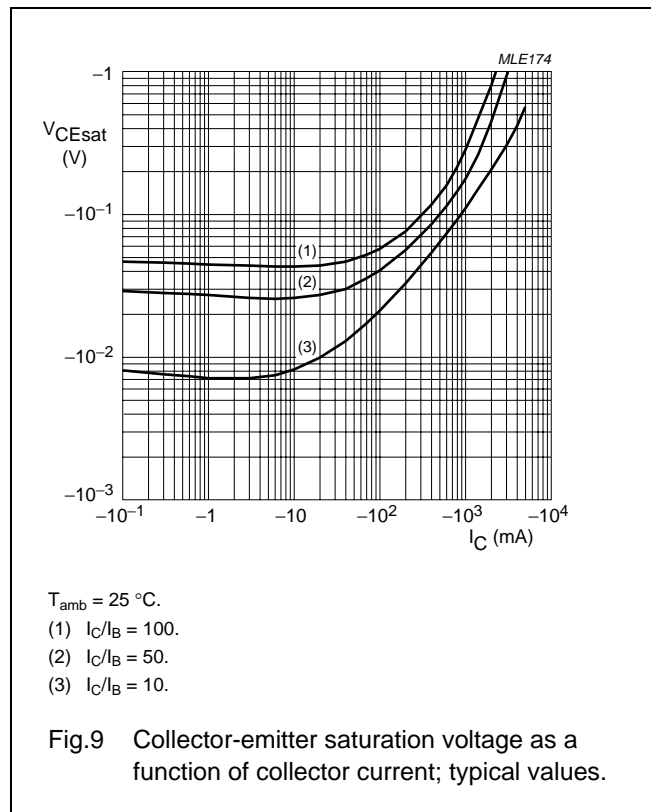
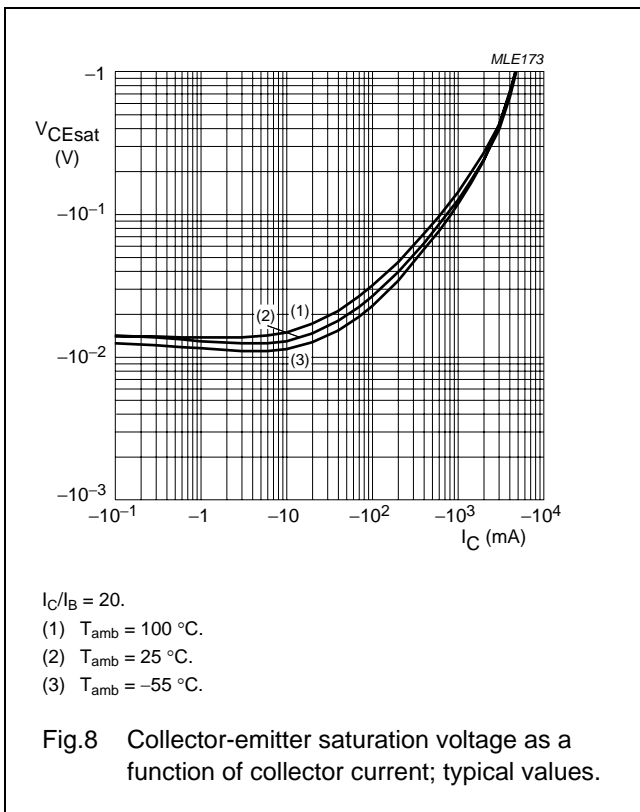
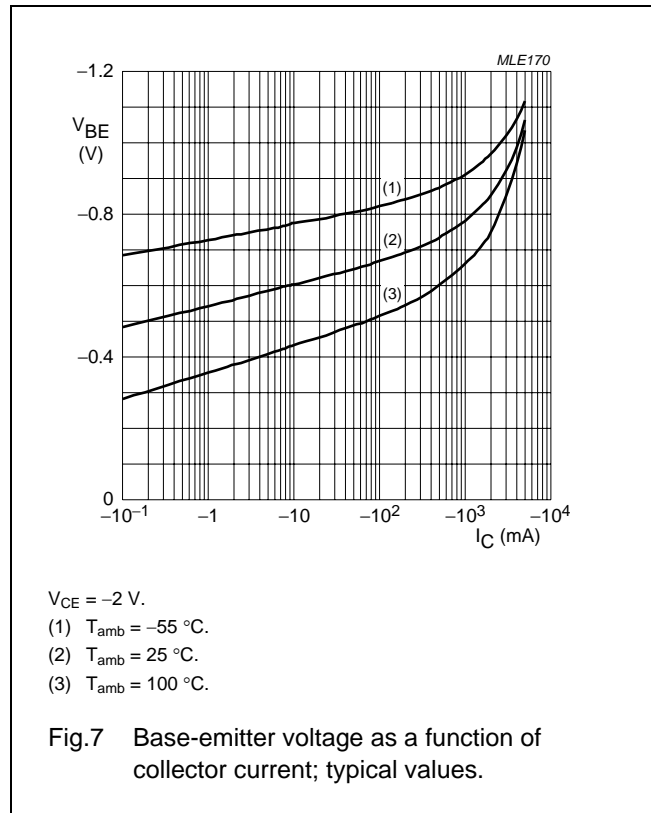
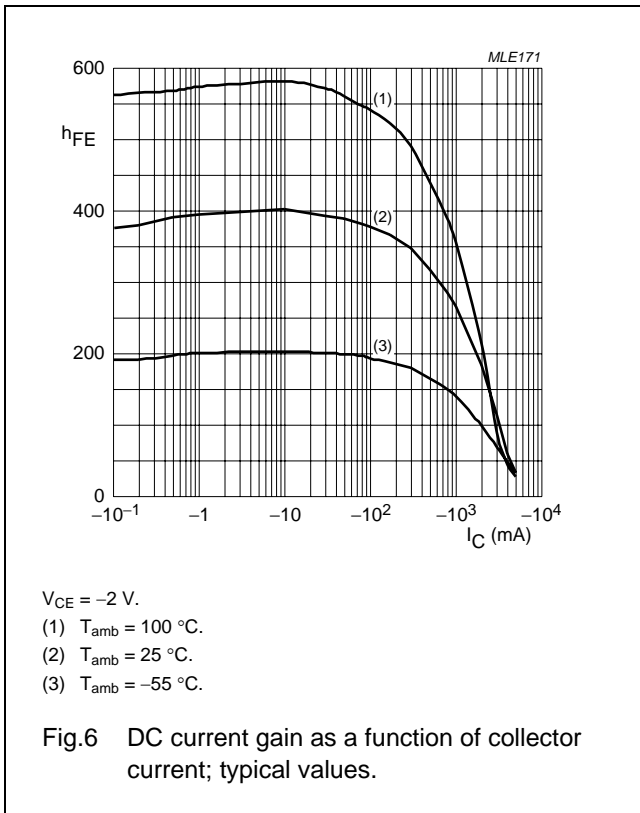
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -50\text{ V}; I_E = 0\text{ A}$	-	-	-100	nA
		$V_{CB} = -50\text{ V}; I_E = 0\text{ A}; T_J = 150\text{ °C}$	-	-	-50	$\mu\text{A}$
$I_{CES}$	collector-emitter cut-off current	$V_{CE} = -50\text{ V}; V_{BE} = 0\text{ V}$	-	-	-100	nA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-100	nA
$h_{FE}$	DC current gain	$V_{CE} = -2\text{ V}$				
		$I_C = -0.1\text{ A}$	200	-	-	
		$I_C = -0.5\text{ A}$	200	-	-	
		$I_C = -1\text{ A}; \text{note 1}$	200	-	450	
		$I_C = -2\text{ A}; \text{note 1}$	130	-	-	
		$I_C = -3\text{ A}; \text{note 1}$	80	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -50\text{ mA}$	-	-	-90	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	-	-	-180	mV
		$I_C = -2\text{ A}; I_B = -100\text{ mA}$	-	-	-320	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	-	-	-270	mV
		$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	-	-	-390	mV
$R_{CEsat}$	equivalent on-resistance	$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	-	90	135	$\text{m}\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -2\text{ A}; I_B = -100\text{ mA}$	-	-	-1.1	V
		$I_C = -3\text{ A}; I_B = -300\text{ mA}; \text{note 1}$	-	-	-1.2	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -1\text{ A}$	-1.1	-	-	V
$f_T$	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	100	-	-	MHz
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	35	pF

**Note**

1. Pulse test:  $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02$ .

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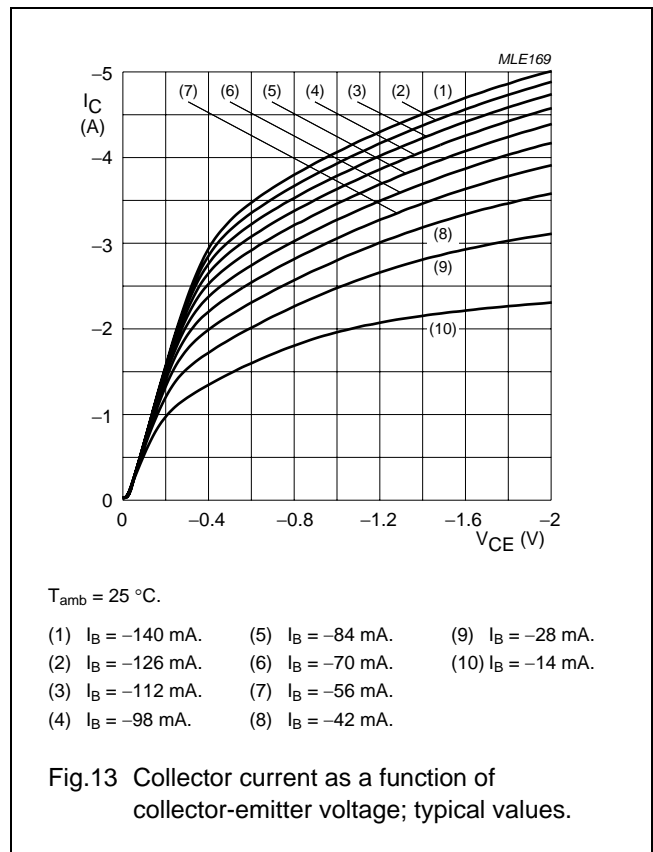
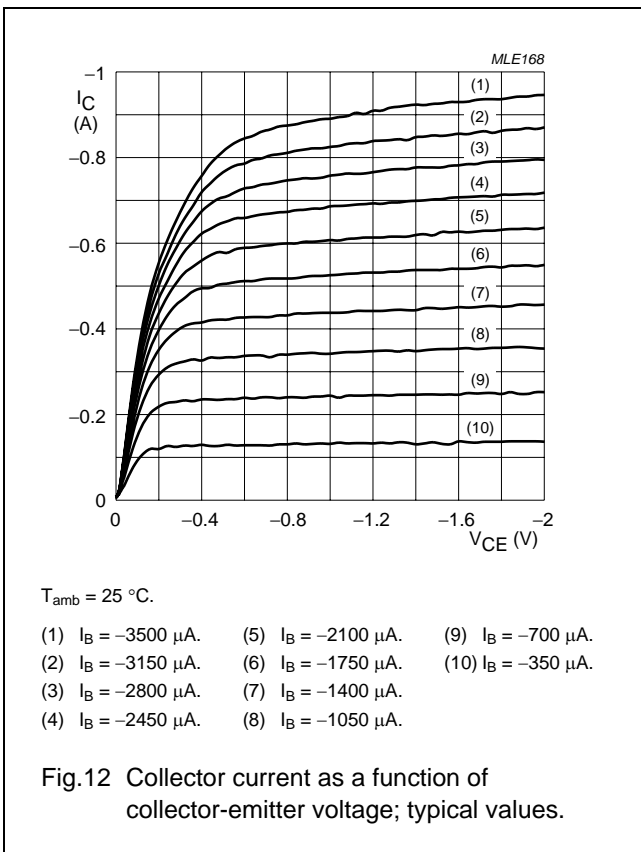
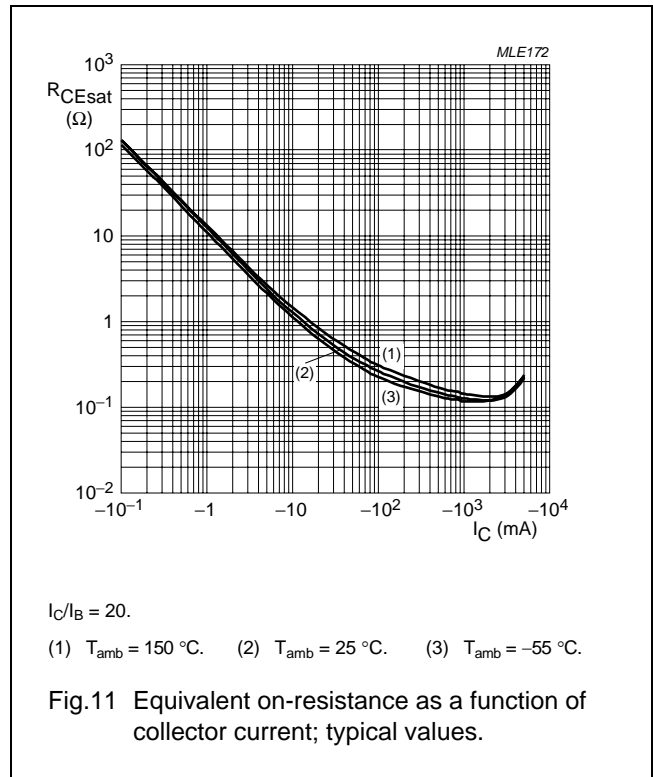
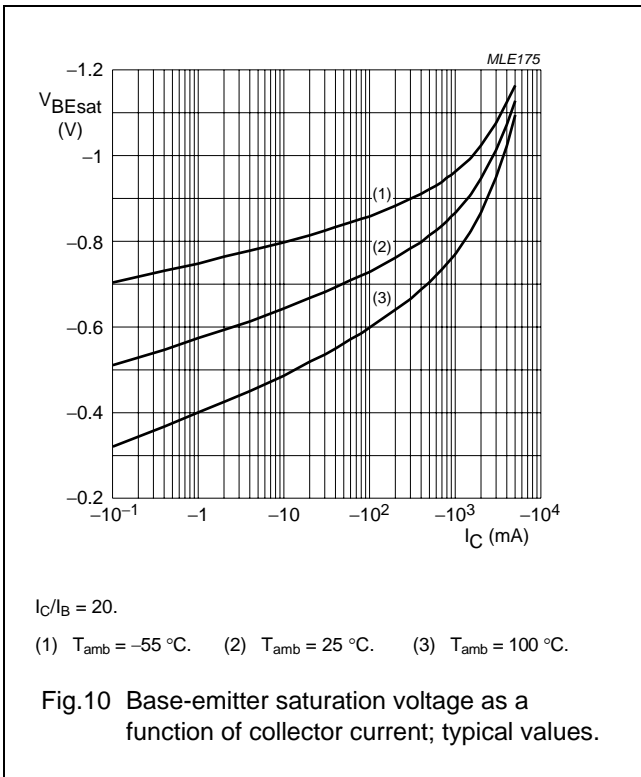
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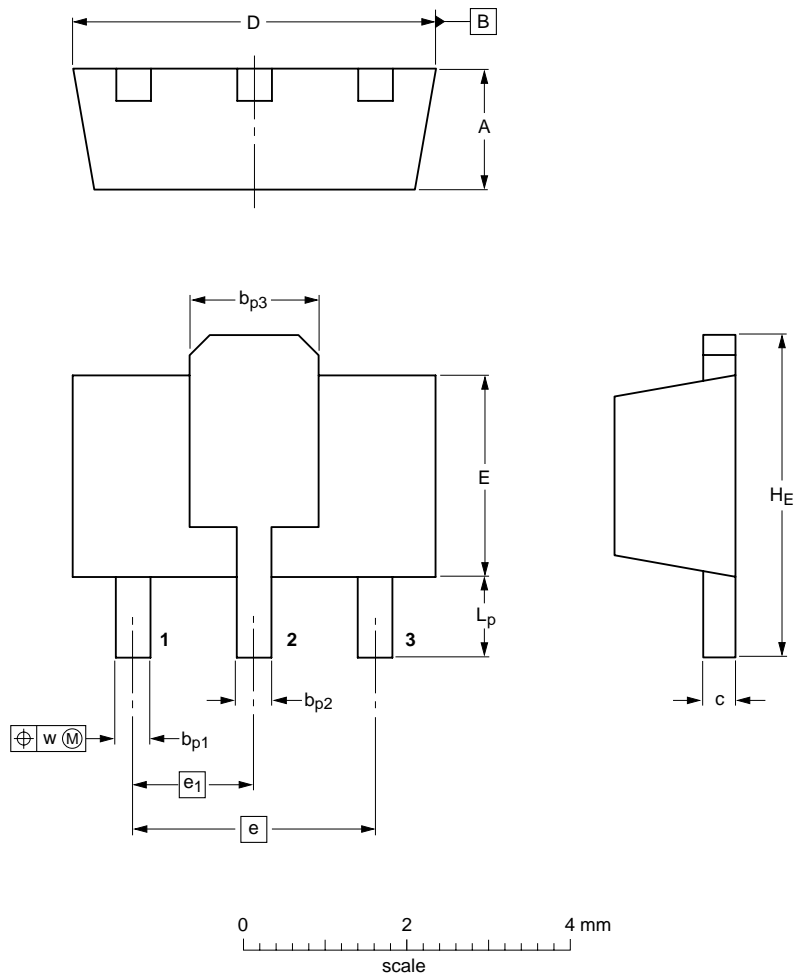
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PACKAGE OUTLINE

Plastic surface-mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p1</sub>	b <sub>p2</sub>	b <sub>p3</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT89		TO-243	SC-62		04-08-03 06-03-16

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**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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# ***NXP Semiconductors***

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

## **Contact information**

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

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