

# PHB/PHD/PHU108NQ03LT

N-channel TrenchMOS™ logic level FET

Rev. 03 — 18 April 2005

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

### 1.2 Features

- Logic level threshold
- Lead-free construction
- Very low on-state resistance
- Low gate charge

### 1.3 Applications

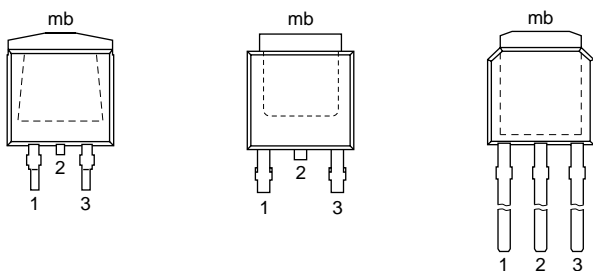
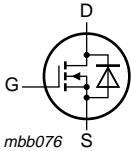
- DC-to-DC converter
- Switch-mode power supplies

### 1.4 Quick reference data

- $V_{DS} \leq 25$  V
- $R_{DS(on)} \leq 6$  m $\Omega$
- $I_D \leq 75$  A
- $Q_{gd} = 5.6$  nC (typ)

## 2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol	
1	gate (G)			
2	drain (D) <sup>[1]</sup>			
3	source (S)			
mb	mounting base; connected to drain			
		SOT404 (D2PAK)	SOT428 (DPAK)	SOT533 (IPAK)

[1] It is not possible to make a connection to pin 2 of the SOT404 and SOT428 packages.

### 3. Ordering information

**Table 2: Ordering information**

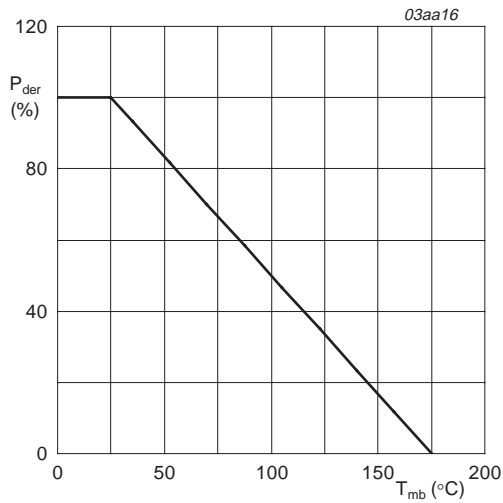
Type number	Package		Version
	Name	Description	
PHB108NQ03LT	D2PAK	plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT404
PHD108NQ03LT	DPAK	plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT428
PHU108NQ03LT	IPAK	plastic single-ended package; 3 leads (in-line)	SOT533

### 4. Limiting values

**Table 3: Limiting values**

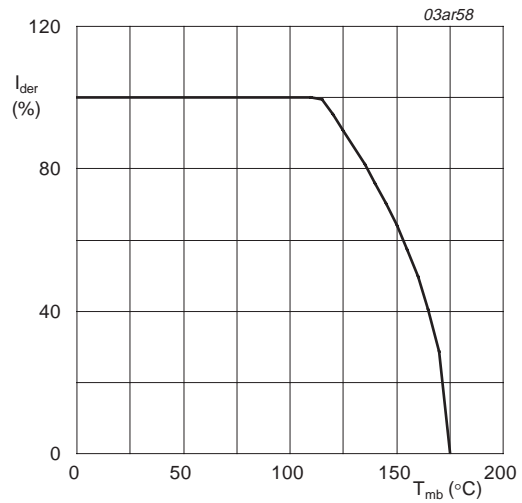
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	25	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; <a href="#">Figure 2</a> and <a href="#">3</a>	-	75	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; <a href="#">Figure 2</a>	-	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <a href="#">Figure 3</a>	-	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Figure 1</a>	-	187	W
$T_{stg}$	storage temperature		-55	+175	°C
$T_j$	junction temperature		-55	+175	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	75	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	240	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 43\text{ A}$ ; $t_p = 0.25\text{ ms}$ ; $V_{DD} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; starting at $T_j = 25\text{ °C}$	-	180	mJ



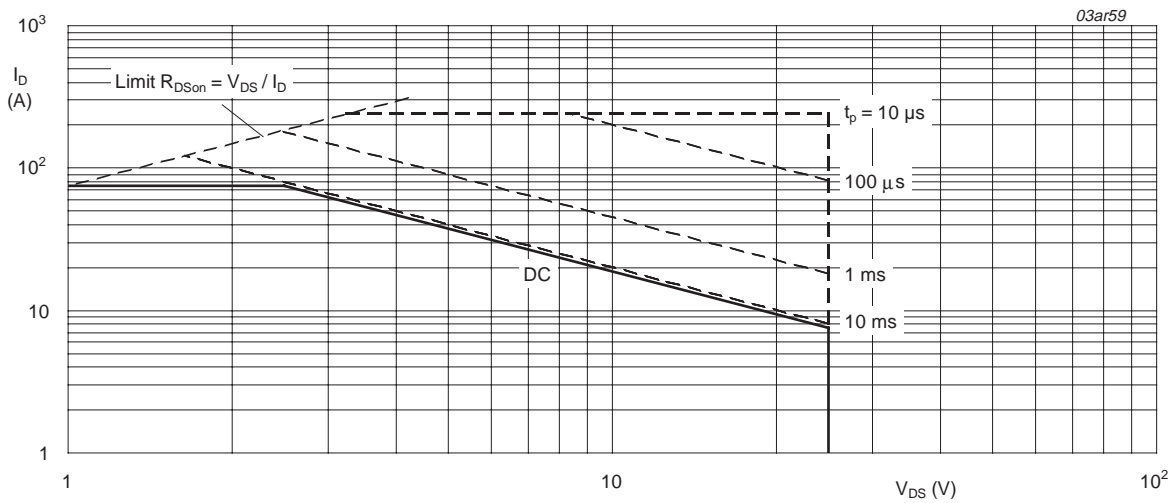
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



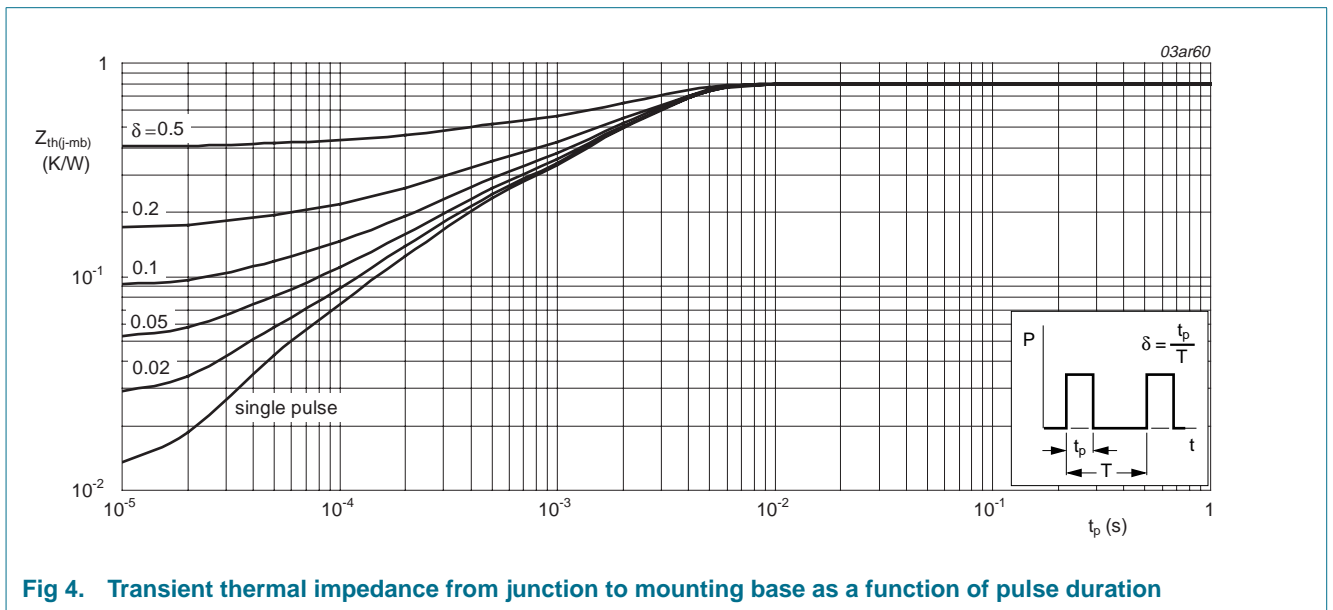
T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse; V<sub>GS</sub> = 5 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 4: Thermal characteristics

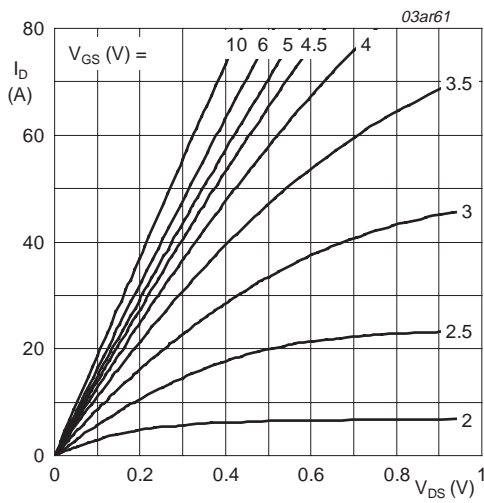
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Figure 4</a>	-	-	0.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT404	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W
	SOT428	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	75	-	K/W
		mounted on a printed-circuit board; vertical in still air; SOT404 minimum footprint	-	50	-	K/W
	SOT533	vertical in free air	-	70	-	K/W



## 6. Characteristics

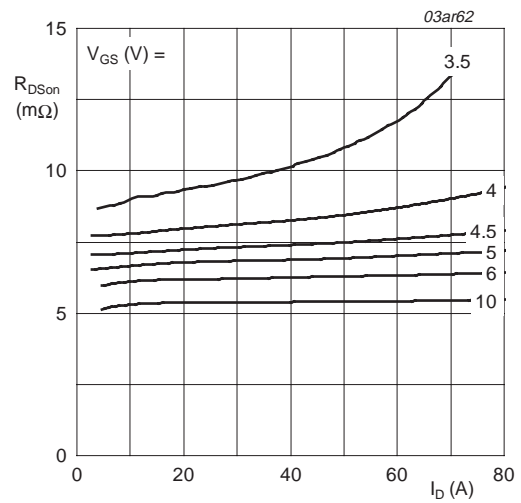
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C T <sub>j</sub> = -55 °C	25 22	- -	- -	V V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <a href="#">Figure 9</a> and <a href="#">10</a> T <sub>j</sub> = 25 °C T <sub>j</sub> = 175 °C T <sub>j</sub> = -55 °C	1 0.5 -	1.5 - -	2 - 2.2	V V V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C T <sub>j</sub> = 175 °C	- - -	- - -	1 500	μA μA
R <sub>G</sub>	gate resistance	f = 1 MHz	-	1.2	-	Ω
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±10 V; V <sub>DS</sub> = 0 V	-	0.02	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; <a href="#">Figure 6</a> and <a href="#">8</a> T <sub>j</sub> = 25 °C T <sub>j</sub> = 175 °C V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; <a href="#">Figure 6</a> and <a href="#">8</a>	- - -	6.7 12.1 5.3	7.5 13.5 6	mΩ mΩ mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 12 V; V <sub>GS</sub> = 4.5 V; <a href="#">Figure 11</a> and <a href="#">12</a>	-	16.3	-	nC
Q <sub>gs</sub>	gate-source charge		-	4	-	nC
Q <sub>gs1</sub>	pre-V <sub>GS(th)</sub> gate-source charge		-	2.5	-	nC
Q <sub>gs2</sub>	post-V <sub>GS(th)</sub> gate-source charge		-	1.5	-	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		-	5.6	-	nC
V <sub>plat</sub>	plateau voltage		-	2.4	-	V
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 4.5 V	-	12.5	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 12 V; f = 1 MHz; <a href="#">Figure 14</a>	-	1375	-	pF
C <sub>oss</sub>	output capacitance		-	640	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	250	-	pF
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 0 V; f = 1 MHz	-	2120	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 12 V; R <sub>L</sub> = 0.5 Ω; V <sub>GS</sub> = 4.5 V;	-	15	-	ns
t <sub>r</sub>	rise time	R <sub>G</sub> = 5.6 Ω	-	38	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	32	-	ns
t <sub>f</sub>	fall time		-	25	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; <a href="#">Figure 13</a>	-	0.86	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V;	-	34	-	ns
Q <sub>r</sub>	recovered charge	V <sub>R</sub> = 25 V	-	21	-	nC



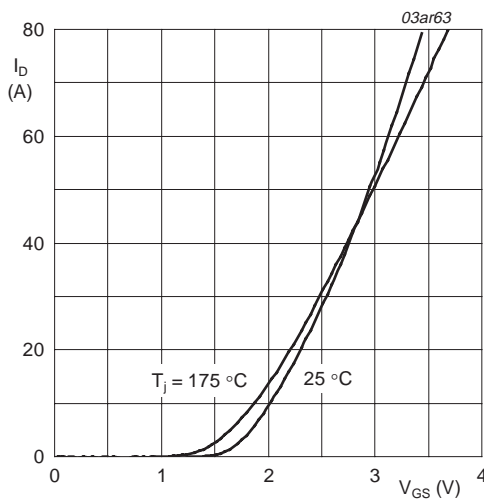
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



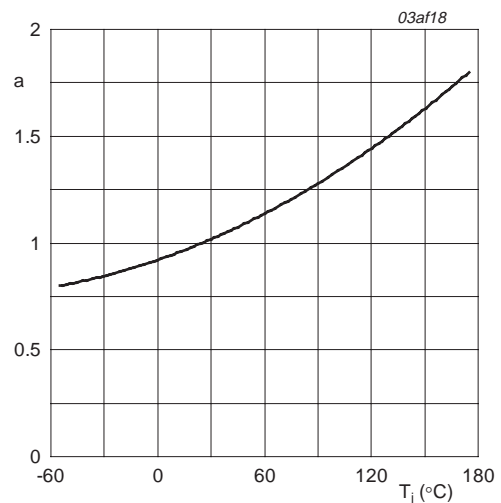
$T_j = 25\text{ }^\circ\text{C}$

**Fig 6. Drain-source on-state resistance as a function of drain current; typical values**



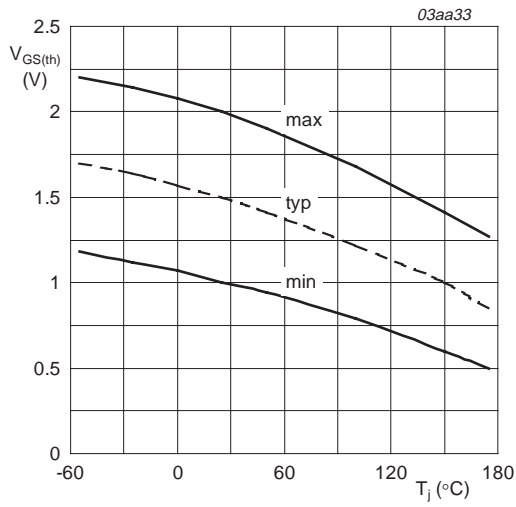
$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



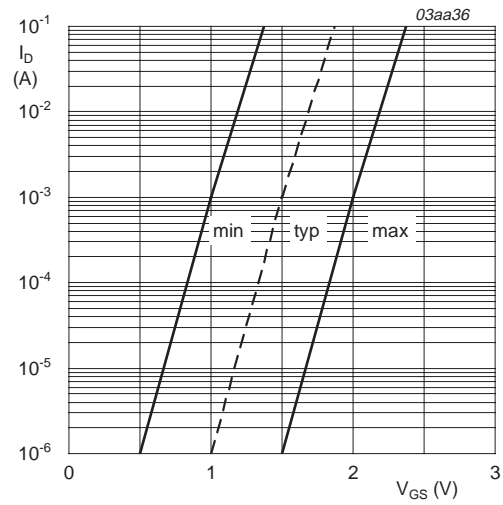
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**



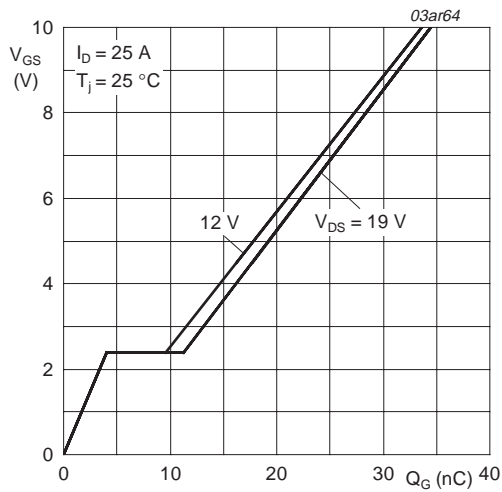
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



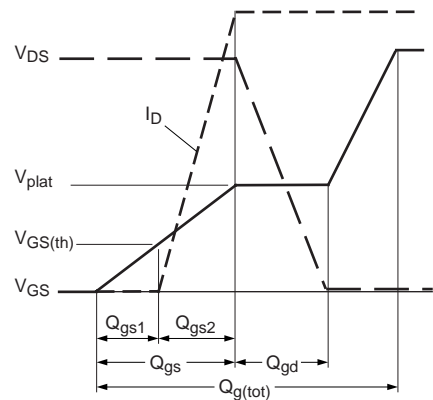
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



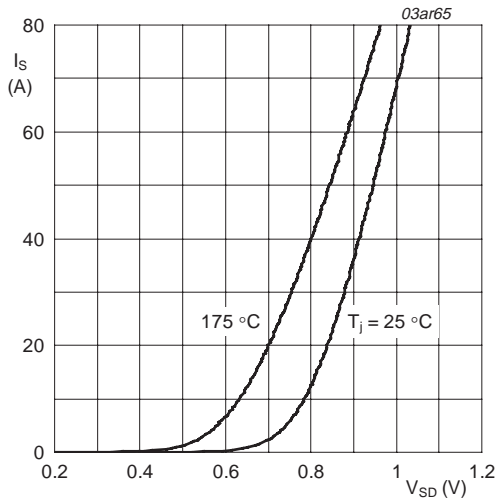
$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V and } 19 \text{ V}$

**Fig 11. Gate-source voltage as a function of gate charge; typical values**



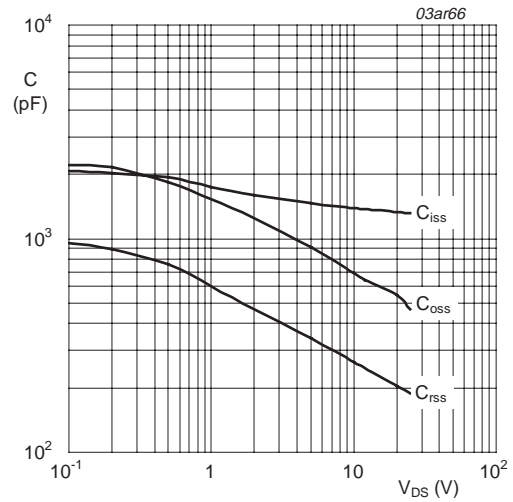
003aaa508

**Fig 12. Gate charge waveform definitions**



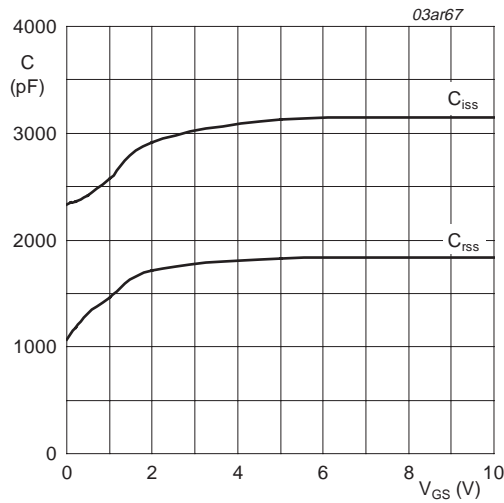
$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}$ ;  $V_{GS} = 0\text{V}$

**Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



$V_{GS} = 0\text{V}$ ;  $f = 1\text{MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$V_{DS} = 0\text{V}$

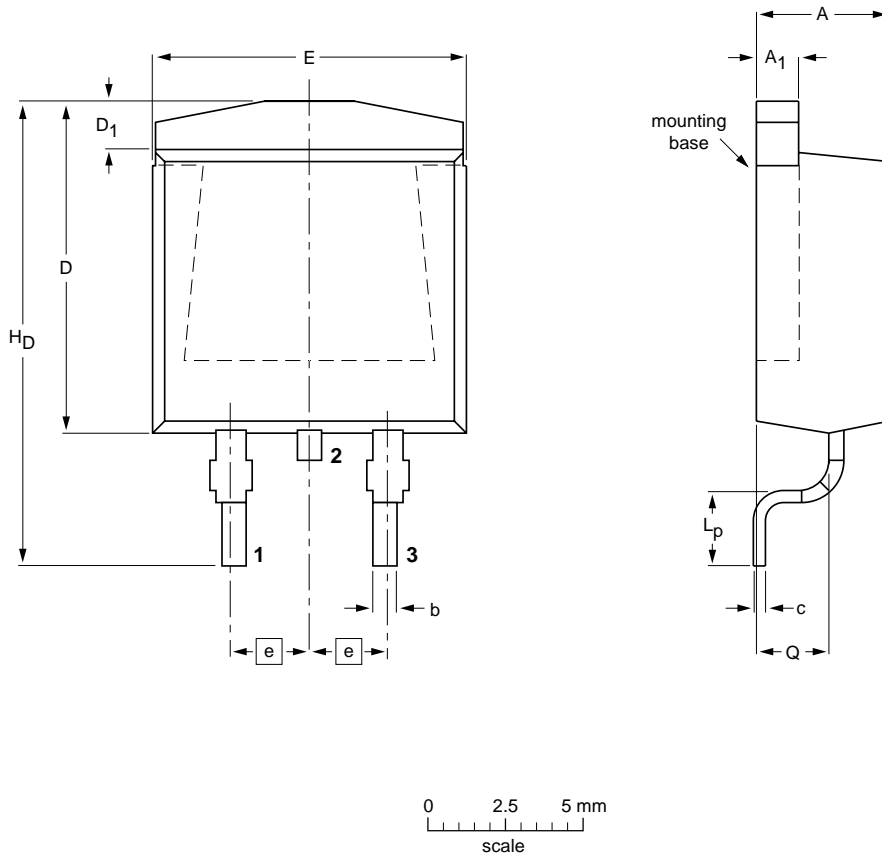
**Fig 15. Input and reverse transfer capacitances as a function of gate-source voltage; typical values**



7. Package outline

Plastic single-ended surface mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D max.	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						04-10-13 05-02-11

Fig 16. Package outline SOT404 (D2PAK)

Plastic single-ended surface mounted package (DPAK); 3 leads (one lead cropped)

SOT428

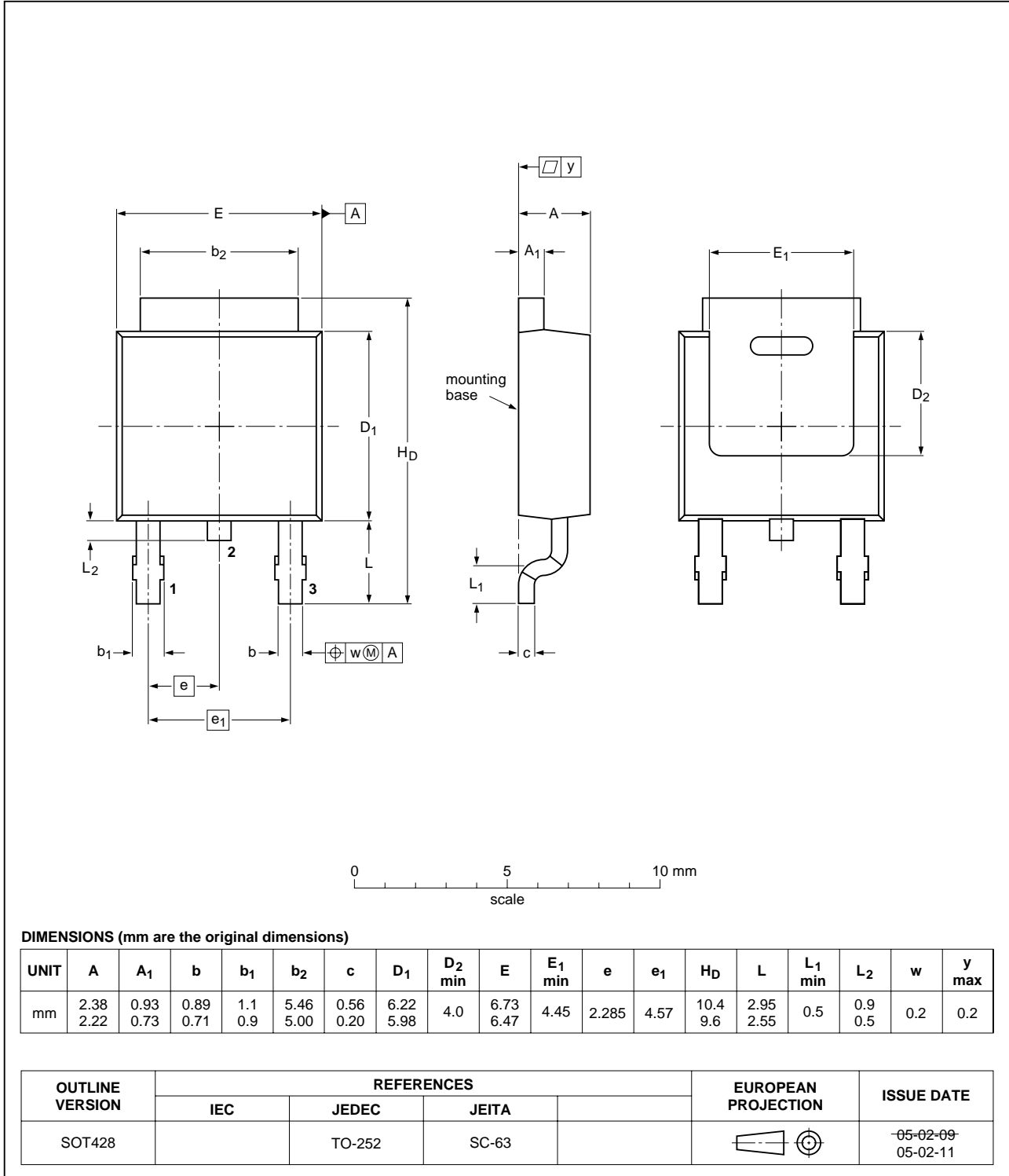
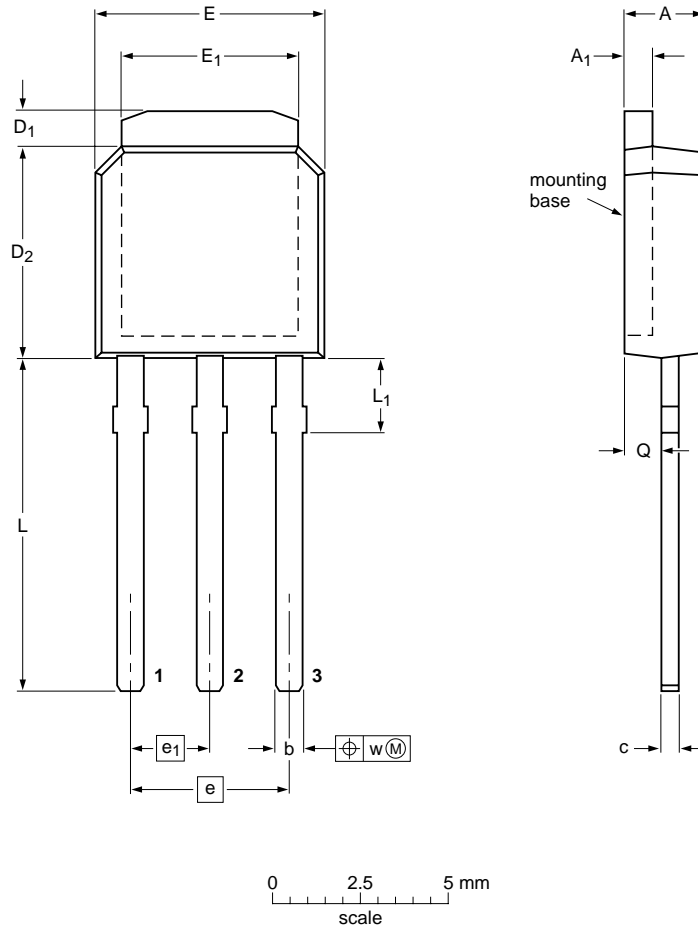


Fig 17. Package outline SOT428 (DPAK)

Plastic single-ended package (IPAK); 3 leads (in-line)

SOT533



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	A <sub>1</sub>	b	c	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(2)</sup> max	Q	w
mm	2.38 2.22	0.89 0.71	0.89 0.71	0.56 0.46	1.10 0.96	6.23 5.97	6.73 6.47	5.21 5.00	4.57 BSC <sup>(1)</sup>	2.285 BSC <sup>(1)</sup>	9.6 9.2	2.7	1.1 1.0	0.3

**Notes**

1. Basic spacing between centers.
2. Terminal dimensions are uncontrolled within zone L<sub>1</sub>.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT533		TO-251			-04-09-22- 05-02-11

Fig 18. Package outline SOT533 (IPAK)

## 8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PHB_PHD_PHU108NQ03LT_3	20050418	Product data sheet	2004070095	9397 750 14707	PHP_PHB_PHD108NQ03LT-02
Modifications: <ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li>• Removal of PHP108NQ03LT</li> <li>• Addition of PHU108NQ03LT</li> <li>• <a href="#">Section 4 “Limiting values”</a> <math>I_D</math>, <math>I_{DM}</math>, <math>P_{tot}</math> and <math>I_{SM}</math> data corrected.</li> <li>• <a href="#">Table 5 “Characteristics”</a> <math>R_{DS(on)}</math>, <math>Q_{g(tot)}</math>, <math>Q_{gs}</math>, <math>Q_{gd}</math>, <math>C_{iss}</math>, <math>C_{oss}</math>, <math>C_{rss}</math>, <math>t_{d(on)}</math>, <math>t_r</math>, <math>t_{d(off)}</math>, <math>t_f</math> and <math>Q_r</math> test conditions and/or typical values modified.</li> <li>• <a href="#">Table 5 “Characteristics”</a> <math>R_G</math>, <math>Q_{gs1}</math>, <math>Q_{gs2}</math> and <math>V_{plat}</math> tests added.</li> <li>• <a href="#">Table 5 “Characteristics”</a> <math>V_{GS(th)}</math>, <math>C_{iss}</math>, <math>C_{rss}</math> and <math>Q_{g(tot)}</math> data added.</li> <li>• <a href="#">Figure 2</a>, <a href="#">3</a>, <a href="#">4</a>, <a href="#">5</a>, <a href="#">6</a>, <a href="#">7</a>, <a href="#">8</a>, <a href="#">11</a>, <a href="#">13</a> and <a href="#">14</a> modified.</li> <li>• <a href="#">Figure 12</a> and <a href="#">15</a> added.</li> </ul>					
PHP_PHB_PHD108NQ03LT-02	20020911	Product data	-	9397 750 10159	PHP_PHB_PHD108NQ03LT-01
PHP_PHB_PHD108NQ03LT-01	20011218	Product data	-	9397 750 09065	-

## 9. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 10. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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## 13. Contact information

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## 12. Trademarks

**TrenchMOS** — is a trademark of Koninklijke Philips Electronics N.V.

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 Document number: 9397 750 14707

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