

System Reset Monolithic IC PST591 ~595 Series

Outline

These ICs function in a variety of CPU systems and other logic systems, to detect power supply voltage and reset the system accurately when power is turned on or interrupted, and has a built-in fixed delay time generating circuit. This series has been represented in the past by PST574/PST575, but these new low reset type system reset ICs expand the delay time series with a counter timer using an analog/digital hybrid circuit.

Features

- | | | |
|---|--|---|
| 1. Fixed delay time setting by counter timer | Excellent delay time temperature characteristics | ±800ppm/°C |
| 2. Low operating limit voltage | | 0.65V typ. |
| 3. Hysteresis voltage provided in detection voltage | | 50mV typ. |
| 4. Current consumption for no-load | | I _{CC} L=300μA typ. I _{CC} H=200μA typ. |
| 5. 5 delay time products available | | PST591 50mS PST594 400mS
PST592 100mS PST595 800mS
PST593 200mS |
| 6. Each product has 9 detection voltage ranks. | | C : 4.5V typ. H : 3.1V typ.
D : 4.2V typ. I : 2.9V typ.
E : 3.9V typ. J : 2.7V typ.
F : 3.6V typ. K : 2.5V typ.
G : 3.3V typ. |

Package

MMP-4A (PST59 × □ M)

TO-92A (PST59 × □)

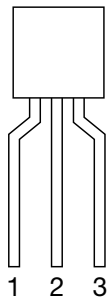
*□ contains detection voltage rank.

(MMP-4A has a manual reset pin, which should be set at GND or NC during normal operation.)

Applications

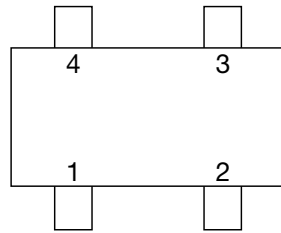
1. Reset circuits in microcomputers, CPUs and MPUs
2. Logic circuit reset circuits.
3. Battery voltage check circuits.
4. Back-up power supply switching circuits.
5. Level detection circuits.
6. Mechanical reset circuits

Pin Assignment



TO-92A

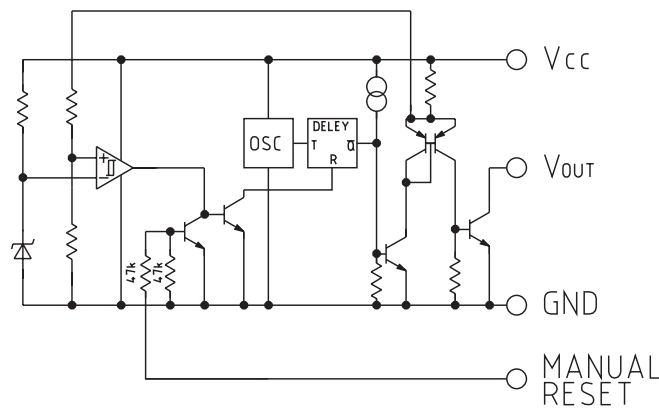
1	V _{CC}
2	GND
3	V _{OUT}



MMP-4A

1	V _{OUT}
2	Manual Reset
3	V _{CC}
4	GND

Equivalent Circuit Diagram



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC} max.	-0.3~10	V
Manual reset input voltage	V _{RES} max.	-0.3~10	V
Allowable loss	P _d	200 (MMP-4P) 300 (TO-92)	mW

Electrical Characteristics (Ta=25°C) (Except where noted otherwise, resistance unit isΩ)

Item	Symbol	Measuring circuit	Measurement conditions	Min.	Typ.	Max.	Unit	
Detection voltage	Vs	1	R _L =470 V _{OL} ≤ 0.4V V _{CC} =H→L	C	4.3	4.5	4.7	V
				D	4.0	4.2	4.4	
				E	3.7	3.9	4.1	
				F	3.4	3.6	3.8	
				G	3.1	3.3	3.5	
				H	2.9	3.1	3.3	
				I	2.75	2.90	3.05	
				J	2.55	2.70	2.85	
K	2.35	2.50	2.65					
Hysteresis voltage	ΔVs	1	R _L =470, V _{CC} =L→H→L	30	50	100	mV	
Detection voltage temperature coefficient	Vs/ΔT	1	R _L =470, Ta=-20°C~+75°C		±0.01		%/°C	
Low-level output voltage	V _{OL}	1	V _{CC} =Vs min.-0.05V, R _L =470		0.1	0.4	V	
Output leakage current	I _{OH}	1	V _{CC} =10V			±0.1	μA	
Circuit current while on	I _{CCL}	1	V _{CC} =Vs min.-0.05V, R _L =∞		300	600	μA	
Circuit current while off	I _{CCH}	1	V _{CC} =Vs typ./0.85V, R _L =∞		200	350	μA	
"H" transport delay time	t _{PLH}	2	R _L =4.7k C _L =100PF *1	PST591	30	50	75	mS
				PST592	60	100	150	
				PST593	120	200	300	
				PST594	240	400	600	
				PST595	480	800	1200	
"L" transport delay time	t _{PHL}	2	R _L =4.7k, C _L =100PF *1		10		μS	
Operating power supply voltage	V _{OPL}	1	R _L =4.7k, V _{OL} ≤ 0.4V		0.65	0.85	V	
Output current while on 1	I _{OL1}	1	V _{CC} =Vs min.-0.05V, R _L =0	8			mA	
Output current while on 2	I _{OL2}	1	Ta=-20°C~+75°C, R _L =0 *2	6			mA	
Manual reset pin	Input high voltage	V _{RESH}		2.0			V	
	Input high current	V _{RESH}	V _{RES} =2V			80	μA	
	Input low voltage	V _{RESL}				0.8	V	

*1 t_{PLH} : V_{CC}= (Vs typ.-0.4V) → (Vs typ.+0.4V), t_{PHL} : V_{CC}= (Vs typ.+0.4V) → (Vs typ.-0.4V)

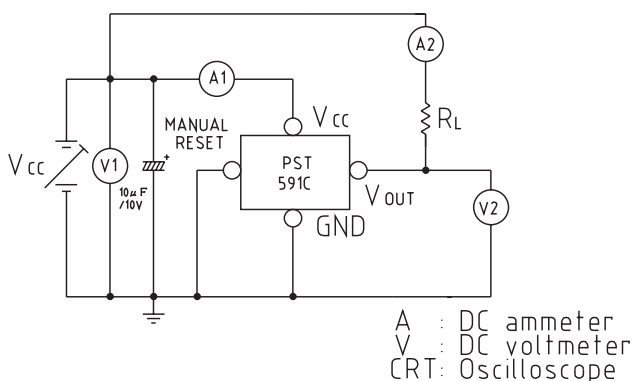
*2 V_{CC}=Vs min.-0.15V

Note 3: V_{OUT} pin is low when manual reset pin is high.

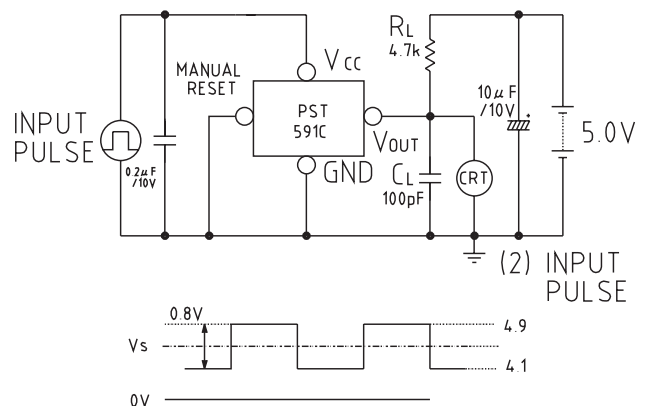
V_{OUT} pin is high when manual reset pin is low.

Measuring Circuit

[1]



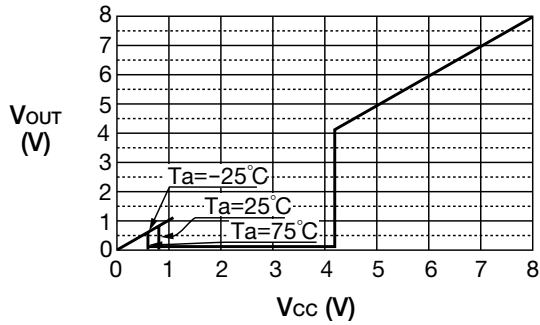
[2]



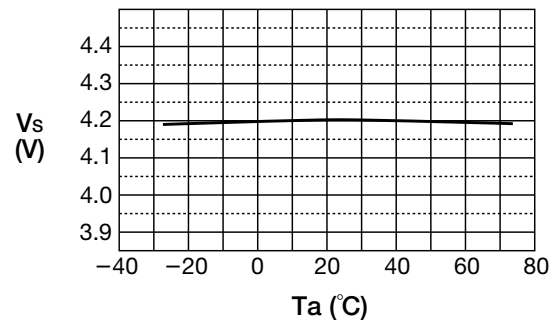
Note: Input model is an example for PST591C.

Characteristics (Example: PST591D)

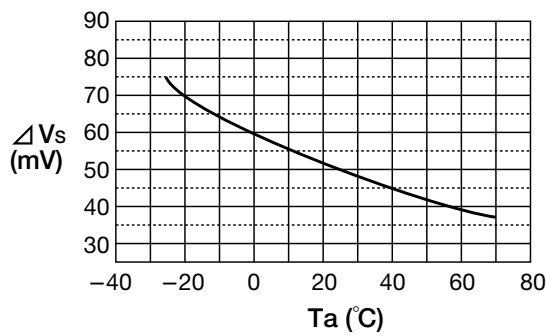
■ **V_{CC} vs. V_{OUT}**



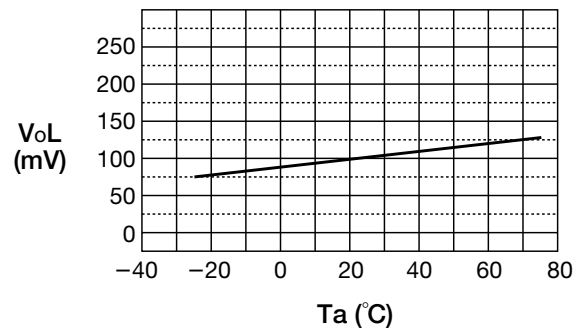
■ **V_s vs. Ta**



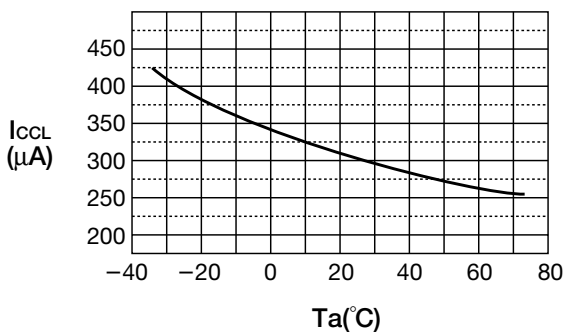
■ **ΔVs vs. Ta**



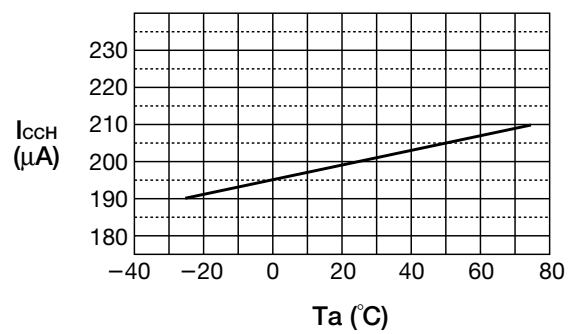
■ **VoL vs. Ta**



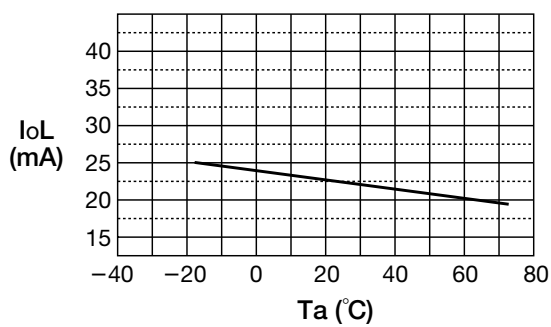
■ **I_{CC}L vs. Ta**



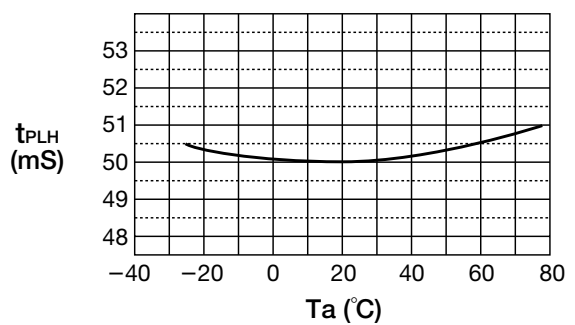
■ **I_{CC}H vs. Ta**



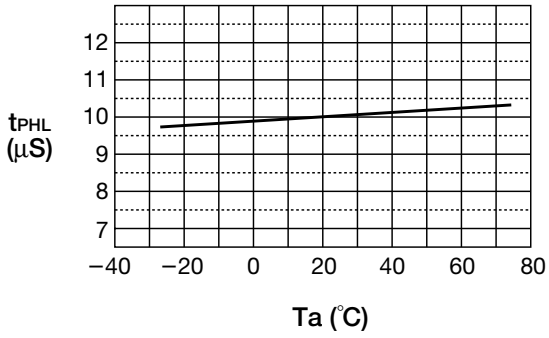
■ **I_oL vs. Ta**



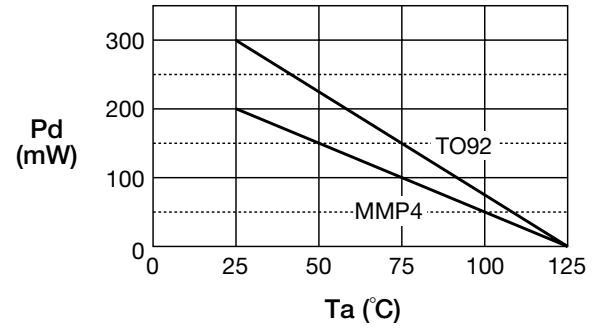
■ **t_{PLH} vs. Ta**



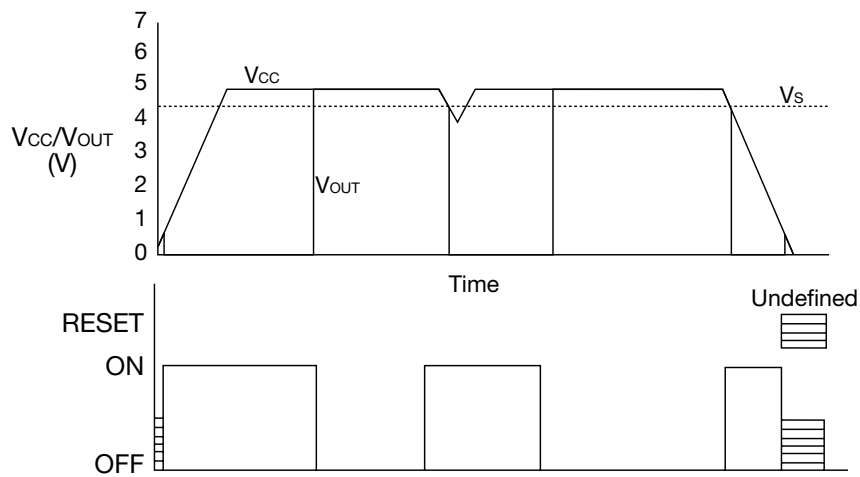
■ t_{PHL} vs. Ta



■ Pd vs. Ta

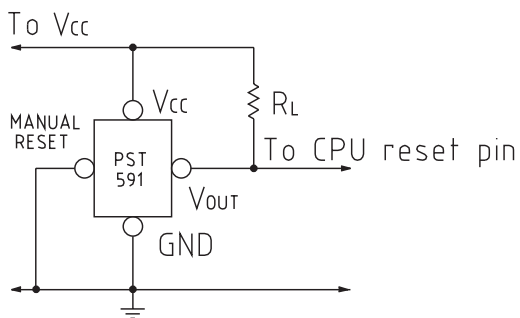


Timing Chart



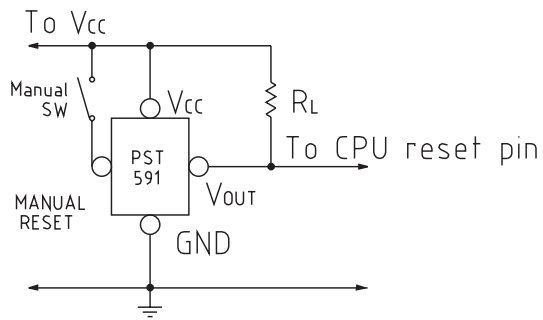
Application circuits

1. Normal hard reset



Note: Connect a capacitor between IC V_{CC} and GND pins if V_{CC} line impedance is high.

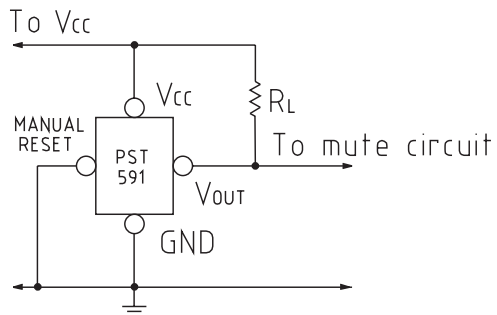
2. Manual reset



V_{OUT} pin low for manual switch ON.
 V_{OUT} pin high for manual switch OFF.

Note: Connect a capacitor between IC V_{CC} and GND pins if V_{CC} line impedance is high.

3. Mute circuit



Note: Connect a capacitor between IC V_{CC} and GND pins if V_{CC} line impedance is high.