## PCMCIA Power Controller

## ■DESCRIPTION

The R5531V002 switches between the three VCC voltages ( $0 \mathrm{~V} / 3.3 \mathrm{~V} / 5.0 \mathrm{~V}$ ) and the Vpp voltages (off/0V/3.3V/5.0V). If VCC pin or VPP pin may be clamped to the GND, short current limit works at $1 \mathrm{~A}(\mathrm{Min}$.$) for VCC and 0.2 \mathrm{~A}(\mathrm{Min}$.) for VPP.
The R5531V002 is suitable for standard PCMCIA power controllers.

## - FEATURES

- Low on resistance P-channel MOSFET Switch
- Over- Current Limit Protection
- Thermal Shutdown Protection
- Built-in Open-drain Flag Pin
- Low Consumption Current
- Break-Before-Make Switching
- SSOP-16 pin Package


## ■APPLICATIONS

- PC card Power Supply Pin Voltage Switch
- Card-bus Slot Power Supply Control
- PC Card Reader/Writer


## $\square$ PIN CONFIGURATION (Top view)



## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Rating | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage(5V) | $\mathrm{V}_{\mathrm{cc} 5}$ | -0.3 to 6.0 | V |
| Input Voltage(3V) | $\mathrm{V}_{\mathrm{cc} 3}$ | -0.3 to 6.0 | V |
| Flag Voltage | VFLG | -0.3 to 6.0 | V |
| Logic Input Voltage | VIN | -0.3 to 6.0 | V |
| Output Current | $\mathrm{Io}(\mathrm{VCC})$ | $>1 \mathrm{~A}$ Internal Limited |  |
|  | $\mathrm{Io}(\mathrm{VPP})$ | $>200 \mathrm{~mA}$ Internal Limited |  |
|  | Pd |  |  |
| Operating Temperature Range | Topt | -40 to 85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | Tstg | -55 to 125 | ${ }^{\circ} \mathrm{C}$ |

[Note] Absolute maximum ratings are threshold limit values that must not be exceeded even for any moment under any conditions. More over, such values for any two or more items of the ratings must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or fatal damage to the device. These mean stress ratings and do not necessarily imply functional operation below these limits.

ELECTRICAL CHARACTERISTICS

| Symbol | Item | Conditions | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Vcc5 | Supply Voltage(5V) |  | 3.0 | 5.0 | 5.5 | V |
| $\mathrm{V}_{\mathrm{cc} 3}$ | Supply Voltage(3V) |  | 3.0 | 3.3 | 5.5 | V |
| Icc5 | Supply Current(each slot) | Vcc OUT $=5 \mathrm{~V}$ or 3.3 V |  | 30 | 60 | $\mu \mathrm{A}$ |
| Islps |  | Vcc OUT $=0 \mathrm{~V}$ (sleep mode) |  | 0.2 | 10.0 | $\mu \mathrm{A}$ |
| Icc3 |  | Vcc OUT $=5 \mathrm{~V}$ or 3.3 V |  | 10 | 30 | $\mu \mathrm{A}$ |
| IsLp3 |  | Vcc OUT $=0 \mathrm{~V}$ (sleep mode) |  | 0.1 | 10 | $\mu \mathrm{A}$ |
| RoV Vcc | Vccout switch resistance | Select Vcc out $=5 \mathrm{~V}$ |  | 85 | 140 | $\mathrm{m} \Omega$ |
|  |  | Select Vcc OUT $=3.3 \mathrm{~V}$ |  | 100 | 150 | $\mathrm{m} \Omega$ |
|  |  | Select Vcc OUT $=0 \mathrm{~V}$ |  | 500 | 3900 | $\Omega$ |
| RoVpp | Vppout switch resistance | Select Vpp out $=5 \mathrm{~V}$ |  | 1.8 | 2.5 | $\Omega$ |
|  |  | Select Vpp out $=3.3 \mathrm{~V}$ |  | 3.3 | 5.0 | $\Omega$ |
|  |  | Select Vpp out $=0 \mathrm{~V}$ |  | 2500 | 3900 | $\Omega$ |
| IPPL | Vppout Leakage Current | Select Vpp out $=\mathrm{Hi}$-Z |  | 1 | 10 | $\mu \mathrm{A}$ |
| ICCSC | Short Current Limit | Vcc out $=0 \mathrm{~V}$ | 1 | 1.4 |  | A |
| IpPsC |  | $V_{\text {pp out }}=0 \mathrm{~V}$ | 0.2 | 0.3 |  | A |
| VIH | Logic Input "H" Voltage |  | 2.2 |  | 6.0 | V |
| VIL | Logic Input "L" Voltage |  | -0.3 |  | 0.8 | V |
| IIN | Logic Input Current |  | -1 |  | 1 | $\mu \mathrm{A}$ |
| TsD | Thermal Shutdown Temperature |  |  | 135 |  | ${ }^{\circ} \mathrm{C}$ |
| VoOK | Flag Threshold Voltage | FLG is pulled up to VCC3IN with $10 \mathrm{k} \Omega$ |  | $\begin{aligned} & \text { Vcc-1 } \\ & \text { VPP-1 } \end{aligned}$ |  | V |
| t1 | Vcc Turn-on Delay Time (*Note 2) | Vcc out $=0 \mathrm{~V}$ to $10 \%$ of 3.3 V |  | 300 | 1500 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{2}$ |  | Vcc out $=0 \mathrm{~V}$ to $10 \%$ of 5.0 V |  | 500 | 3000 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{3}$ | Vcc Rising Time (*Note 2) | Vcc OUT $=10 \%$ to $90 \%$ of 3.3 V | 200 | 800 | 2500 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{4}$ |  | Vcc OUT $=10 \%$ to $90 \%$ of 5.0 V | 200 | 1800 | 6000 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{7}$ | $\begin{aligned} & \text { Vcc Turn-off Delay Time } \\ & (* \text { Note } 1,2,4) \end{aligned}$ | Vcc OUT $=3.3 \mathrm{~V}$ to $\mathrm{Hi}-\mathrm{Z}$ |  | 2.3 | 8.0 | ms |
| t8 |  | Vcc out $=5 \mathrm{~V}$ to Hi-Z |  | 2.8 | 8.0 | ms |
| t5 | Vcc Falling Time (*Note 3) | Vcc OUT $=90 \%$ to $10 \%$ of 3.3 V | 100 | 700 | 1500 | $\mu \mathrm{s}$ |
| t6 |  | Vcc OUT $=90 \%$ to $10 \%$ of 5.0 V | 100 | 600 | 2000 | $\mu \mathrm{s}$ |
| t9 | Vpp Turn-on Delay Time <br> (*Note 3) | Vpp OUT $=0 \mathrm{~V}$ to $10 \%$ of 3.3 V |  | 15 | 50 | $\mu \mathrm{s}$ |
| t10 |  | Vpp out $=0 \mathrm{~V}$ to $10 \%$ of 5.0 V |  | 25 | 50 | $\mu \mathrm{s}$ |
| t11 | Vpp Rising Time (*Note 3) | Vpp out $=10 \%$ to $90 \%$ of 3.3 V | 100 | 200 | 800 | $\mu \mathrm{s}$ |
| t12 |  | Vpp ouT $=10 \%$ to $90 \%$ of 5.0 V | 100 | 280 | 1000 | $\mu \mathrm{s}$ |
| t15 | Vpp Turn-off Delay Time (*Note 1,3) | Vpp out $=3.3 \mathrm{~V}$ to $\mathrm{Hi}-\mathrm{Z}$ |  | 0.1 | 1.0 | $\mu \mathrm{s}$ |
| t16 |  | Vpp out $=5 \mathrm{~V}$ to $\mathrm{Hi}-\mathrm{Z}$ |  | 0.1 | 1.0 | $\mu \mathrm{s}$ |
| t13 | Vpp Falling Time (*Note 3) | Vpp out $=90 \%$ to $10 \%$ of 3.3 V |  | 0.05 | 1.00 | $\mu \mathrm{s}$ |
| t14 |  | Vpp out $=90 \%$ to $10 \%$ of 5.0 V |  | 0.05 | 1.00 | $\mu \mathrm{s}$ |

(*Note1) Delay from commanding Hi-Z or 0 V to beginning slope
(*Note2) t1 to t 8 Test Condition: RL=10
(*Note3) t9 to t 15 Test Condition: $\mathrm{RL}=100 \Omega$
(*Note4) Do not apply to current limit or thermal shutdown conditions during these terms

## TEST CIRCUITS

(1) ICCSC

(2) IPPSC

(3) t1 to t8

(4) t9 to t16

(Note 1) Except VCCOUT pin and VPPOUT pin, test circuits are same as typical application circuit. (Note 2) At the measurement of Flag threshold voltage, add $10 \mathrm{k} \Omega$ between FLG pin and Vcc3IN pin.

## - TIMING DIAGRAMS



Vcc Timing Diagram


VPP Timing Diagram

## OPERATION

## (1) Operation Description

When the VCCOUT $=0 \mathrm{~V}$ is selected, the IC switches into the sleep mode, and draws only nano-amperes of leakage current.
Without being $\mathrm{V}_{\text {CCOUT }}=0 \mathrm{~V}$, if commanded to immediately switch from 5 V to 3.3 V or vice versa, enhancement of the second switch begins after the first is OFF, realizing "break-before-make switching".
In case that an OUT pin may be clamped to the GND, if over-current would continue, the temperature of the IC would increase drastically. If the temperature of the IC is beyond Typ. $135^{\circ} \mathrm{C}$, the switch transistor turns off. Then, when the temperature of the IC decreases by approximately $10^{\circ} \mathrm{C}$, the switch transistor turns on. Unless the abnormal situation of OUT pin is removed or turned off, the switch transistor repeats on and off.
Short over-current level is set internally in the IC. There are two types of response against over-current: (1) Under the condition that OUT pin is short or large capacity is loaded, if the IC is enabled, the IC becomes constant current state immediately. Current level of constant current is short current limit. (2) While the switch transistor is on, if OUT pin is short or large capacity is loaded, until the current limit circuit responds, large transient current flows. The transient current depends on the impedance between the power supply circuit, VCC5IN/VCC3IN and load capacitance. In other words, the transient current depends on the transient response characteristics of the power supply circuit, VCC5IN/VCC3IN, PCB layout, and the connector of the card. After the transient current is beyond the current limit threshold and current limit circuit responds, the IC becomes into the constant current mode, and the current level is equal to short current limit.
(2) Typical Application 1

(3) Typical Application 2

(Note1) Control Input 1 through 4 means a signal from PCMCIA controller.
(Note2) 12 V through 15 V voltage can be forced to VCC_12V
(4) Control Logic Table

| Vcc5_EN | Vcc3_EN | EN1 | EN0 | Vcc OUT | Vpp out |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0V | 0V |
| 0 | 0 | 0 | 1 | 0 V | Hi-Z |
| 0 | 0 | 1 | 0 | 0 V | Hi-Z |
| 0 | 0 | 1 | 1 | 0V | Hi-Z |
| 0 | 1 | 0 | 0 | 5 V | 0V |
| 0 | 1 | 0 | 1 | 5 V | 5 V |
| 0 | 1 | 1 | 0 | 5 V | Hi-Z |
| 0 | 1 | 1 | 1 | 5 V | Hi-Z |
| 1 | 0 | 0 | 0 | 3.3 V | 0V |
| 1 | 0 | 0 | 1 | 3.3 V | 3.3 V |
| 1 | 0 | 1 | 0 | 3.3 V | Hi-Z |
| 1 | 0 | 1 | 1 | 3.3 V | Hi-Z |
| 1 | 1 | 0 | 0 | 0 V | 0V |
| 1 | 1 | 0 | 1 | 0 V | Hi-Z |
| 1 | 1 | 1 | 0 | 0 V | Hi-Z |
| 1 | 1 | 1 | 1 | 0V | Hi-Z |

## APPLICATION NOTES

* Set a bypass capacitor with a capacity range from $0.1 \mu \mathrm{~F}$ to $1 \mu \mathrm{~F}$ between VCC5IN pin and GND pin, and between VCC3IN and GND pin, each.
* VCC5IN voltage should be equal or more than VCC3IN.
* Same name pins should be connected one another.
* There is a parasitic diode between source and drain of the switch transistors. (Refer to the block diagram.) Therefore, even If the switch may be disabled, in case the OUT voltage is higher than VCC5IN, some current flows from OUT to VCC5IN.


## $\square$ TYPICAL CHARACTERISTICS

1) Supply Current Iccs vs. Temperature
2) Supply Current Iссз vs. Temperature


3) Short Current Limit vs. Temperature (Select VCCOUT=5V)

4) Short Current Limit vs. Temperature (Select VPPOUT=5V)

5) VCCOUT Switch Resistance vs. Temperature (Select VCCOUT=5V)

6) Short Current Limit vs. Temperature (Select VCCOUT=3.3V)

7) Short Current Limit vs. Temperature (Select VCCOUT=3.3V)

8) Vccout Switch Resistance vs. Temperature (Select Vccout=3.3V)

9)Vcc Turn on speed (Select Vccout=5V)

9) Vcc Turn on speed (Select Vccout $=3.3 \mathrm{~V}$ )

10) Vcc Turn off speed (Select VccouT=5V)

11) Vcc Turn off speed (Select Vccout=3.3V)

