35V Gate Pulse Modulator for LCD Panels

General Description

The Gate Pulse Modulator (GPM) is specially designed for the application of gate driver in TFT LCD panels. The GPM is controlled by frame signals from timing controller to modulate the Gate-On voltage that acts a flicker compensation circuit to reduce the coupling effect between gate lines and pixels. It also can delay the Gate-On voltage while power-on for achieving a correct power-on-sequence for gate driver ICs. Both of the delay time for flicker compensation and power-on-sequence are programmable by external resistors and capacitors.

Features

- **Flicker Compensation Circuit**
- **Reduction of Coupling Effect Between Gate Line and Pixel**
- **Programmable Power Sequence for Gate Driver IC**
- **Operation from 20V to 35V Positive Supply Input**
- **Adjustable Output Delay Time**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- TFT-LCD Panels

Ordering Information

RT8901 □ □

Package Type
S : SOP-8

Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

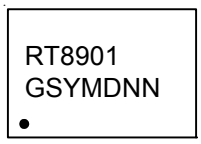
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT8901GS

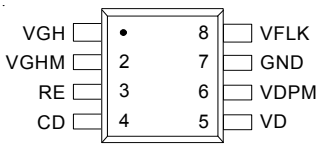


RT8901GS : Product Number

YMDNN : Date Code

Pin Configurations

(TOP VIEW)



SOP-8

Typical Application Circuit

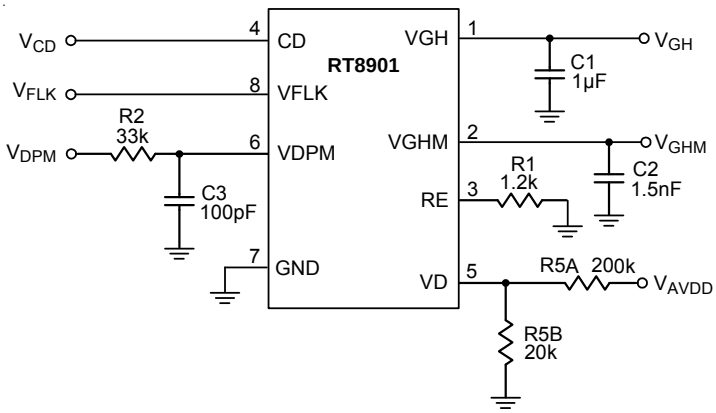


Figure 1. Typical Application Circuit for Mode A and Mode C

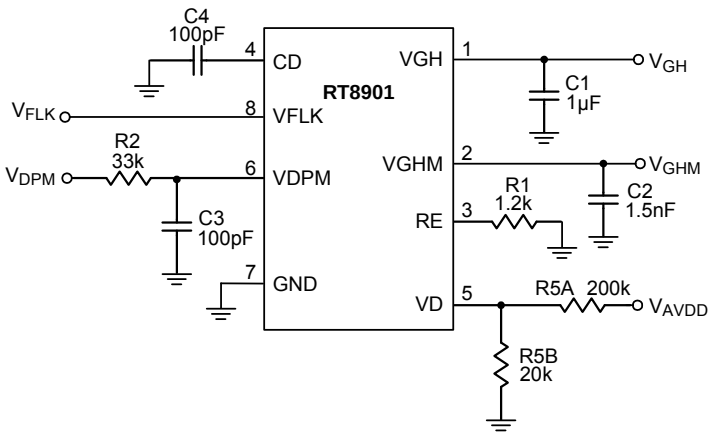


Figure 2. Typical Application Circuit for Mode B

Timing Diagram

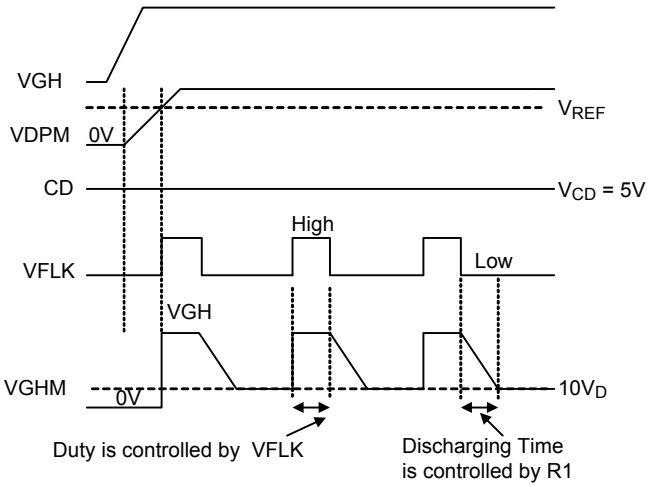


Figure 3. Timing Sequence of Mode A

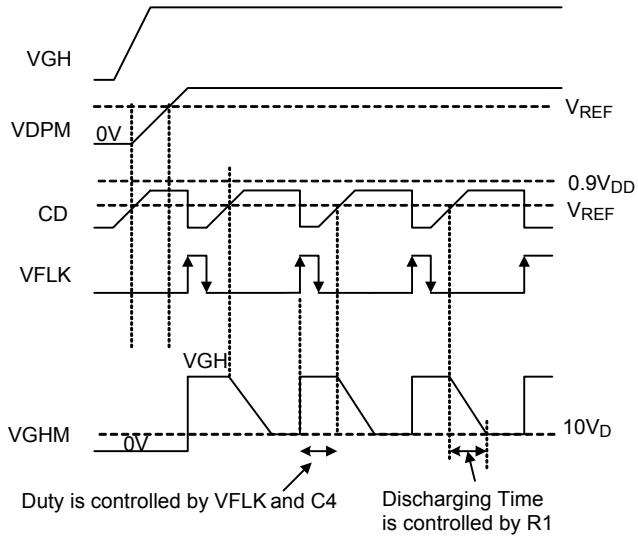


Figure 4. Timing Sequence of Mode B

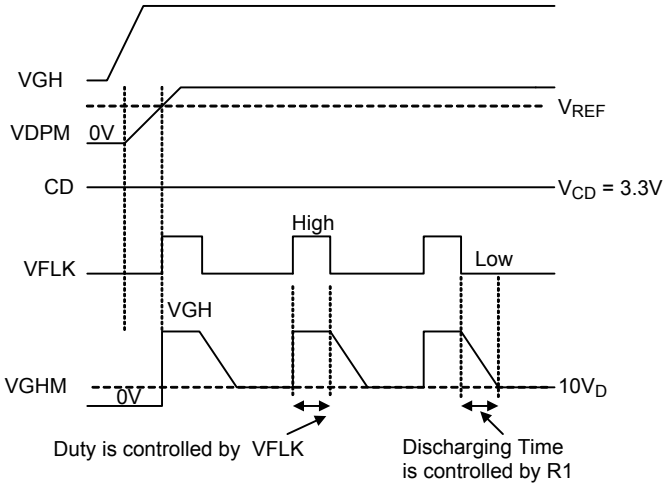
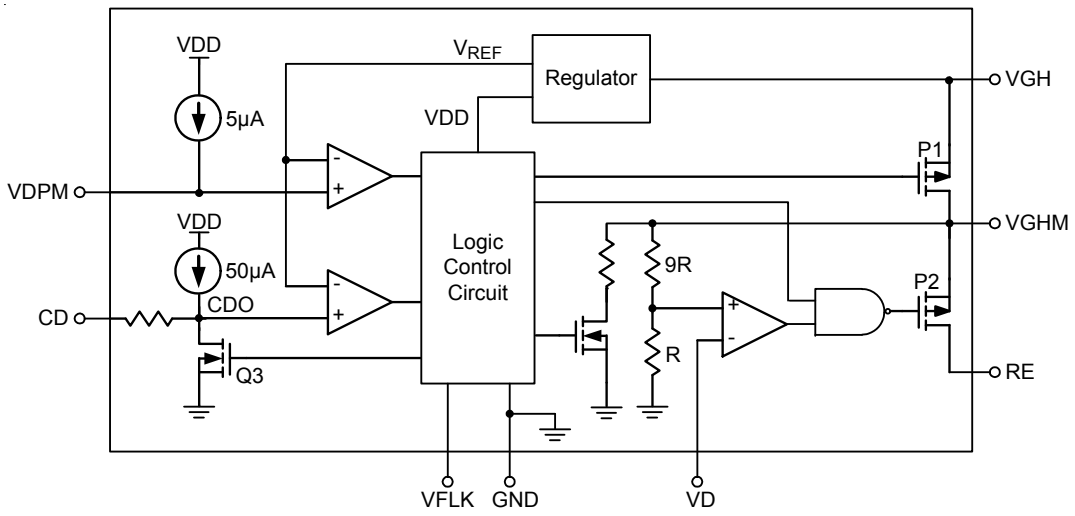


Figure 5. Timing Sequence of Mode C

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VGH	Power Supply Input.
2	VGHM	Switch output directly drives the power supply of Gate Driver IC.
3	RE	Source of the internal high-voltage MOSFET P2 connect to a resistor from this pin to ground.
4	CD	VGHM Discharging Delay Input. For mode selection and VGHM discharging delay time setting.
5	VD	VGHM Low-Level Regulation Set-Point Input. The voltage level is 10VD.
6	VDPM	High-Voltage Switch Delay Input. Connect a capacitor from VDPM to GND to set the delay time. The internal current source is 5μA.
7	GND	Ground.
8	VFLK	Control Signal Input Pin. VFLK is produced from timing controller in LCD module.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- VGH, VGHM, RE to GND ---------- –0.3V to 40V
- VFLK, VDPM, VD, CD to GND ---------- –0.3V to 6.5V
- Output Current Source from VGH (Pulse Width <500ns with period >2.5µs) ---------- 1A
- Output Current (rms value), R1 = 0Ω ---------- 133mA
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 ---------- 0.833W
- Package Thermal Resistance (Note 2)
  SOP-8, θ_{JA} ---------- 120°C/W
  SOP-8, θ_{JC} ---------- 30°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(VGH = +30V, GND = 0V, T_A = 25°C, unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply Voltage		V_{VGH}		20	--	35	V
Input Supply Current		I_{VGH}	CD = VDPM = 5V, V_{VFLK} = 5V	--	0.5	1.5	mA
Adjustable VGHM Falling Regulation Voltage		$10V_D$	f_{VFLK} = 25kHz, VGHM at Low, VGHM with 1.5nF, R1 = 1.2kΩ	3	--	V_{GH}	V
VFLK Threshold Voltage	Logic- High	V_{VFLK_H}		1.5	--	5.5	V
	Logic- Low	V_{VFLK_L}		0	--	0.4	
VFLK Input Leakage Current		I_{Leak}	V_{VFLK} = 0V or High	–1		1	µA
VFLK to VGHM Rising Propagation Delay		t_{PLH}	R1 = 1.2kΩ, VGHM with 1.5nF, V_{VFLK} = 0 to 3V, measure V_{VFLK} = 1.5V to 10% VGHM	--	100	200	ns
VFLK to VGHM Falling Propagation Delay at Mode A		t_{PHL}	CD = 5V, R1 = 1.2kΩ, VGHM with 1.5nF , V_{VFLK} = 3 to 0V, measure V_{VFLK} = 1.5V to 90% VGHM	--	100	200	ns
VFLK to VGHM Falling Propagation Delay at Mode C		t_{PHL}	CD = 3.3V, R1 = 1.2kΩ, VGHM with 1.5nF , V_{VFLK} = 3 to 0V, measure V_{VFLK} = 1.5V to 90% VGHM	--	260	--	ns
Operation Frequency		f_{OSC}		--	--	300	kHz
VDPM Voltage Threshold		V_{DPM_H}	VDPM High Logic Threshold	2.4	2.5	2.6	V
CD Mode A Operation Range		V_{CD_A}		--	5	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CD Mode B Voltage Threshold	V_{CD_THB}		2.4	2.5	2.6	V
CD Mode C Operation Range	V_{CD_C}		3	--	3.6	V
VDPM Charge Current	I_{VDPM}	Connect VDPM to GND, V_{VGH} = 30V, V_{VFLK} = 5V	4	5	6	μA
CD Charge Current	I_{CD}	Connect CD to GND, V_{VGH} = 30V, V_{VFLK} = 0V	40	50	60	μA
VGH Switch On Resistance	R_{P1}	V_{VGH} = 30V/-20mA at V_{VFLK} = 5V	--	15	30	Ω
RE Switch On Resistance	R_{P2}	V_{VGH} = 30V/+20mA at V_{VFLK} = 0V	--	15	30	Ω
CD Switch On Resistance	R_{Q3}	I_{CD} = +1mA at V_{VFLK} = 5V	--	1	--	kΩ

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

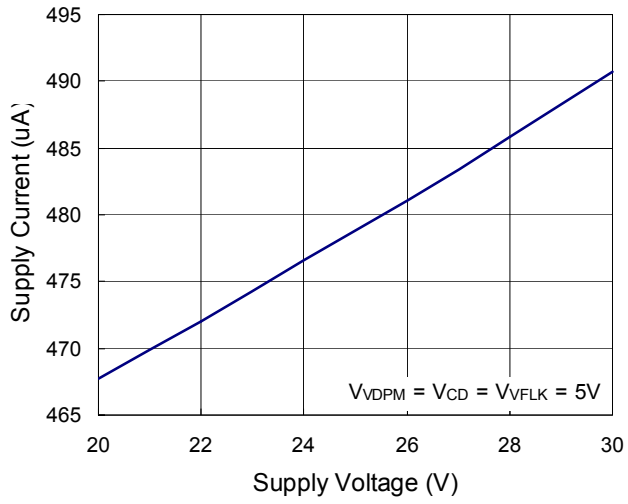
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

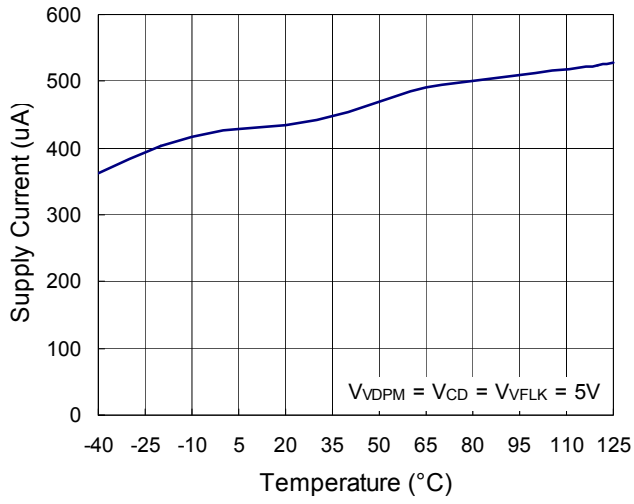
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

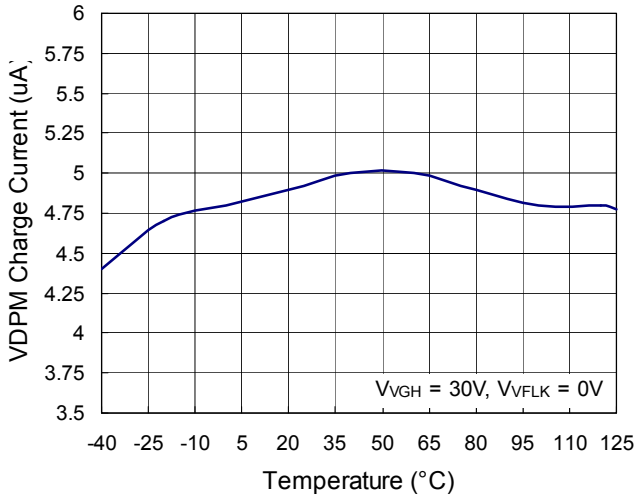
Supply Current vs. Supply Voltage



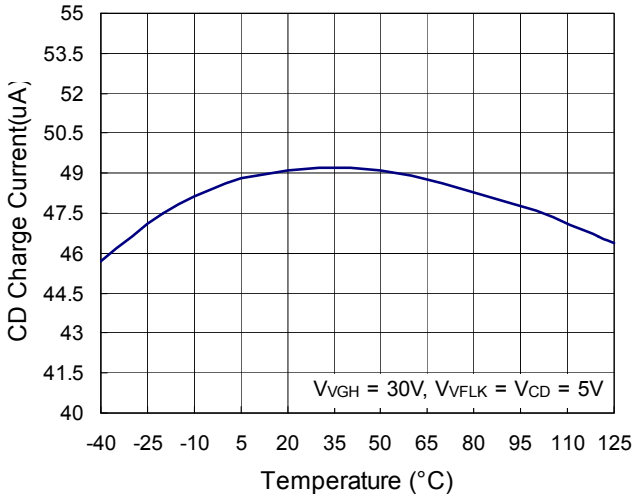
Supply Current vs. Temperature



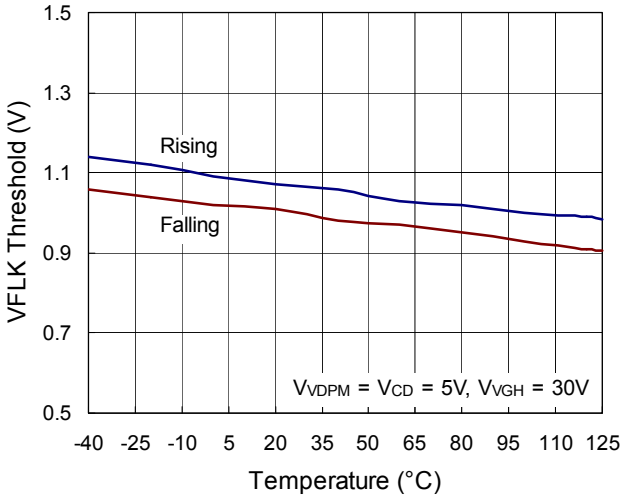
VDPM Charge Current vs. Temperature



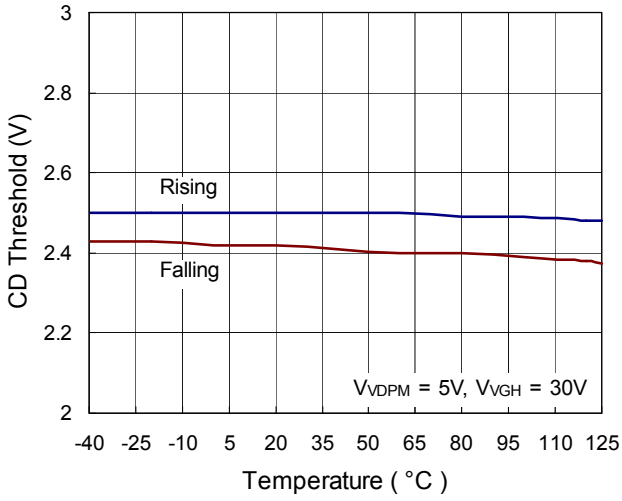
CD Charge Current vs. Temperature



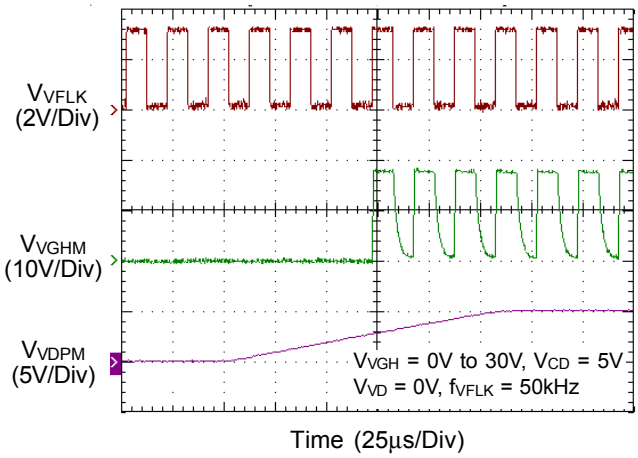
VFLK Threshold vs. Temperature



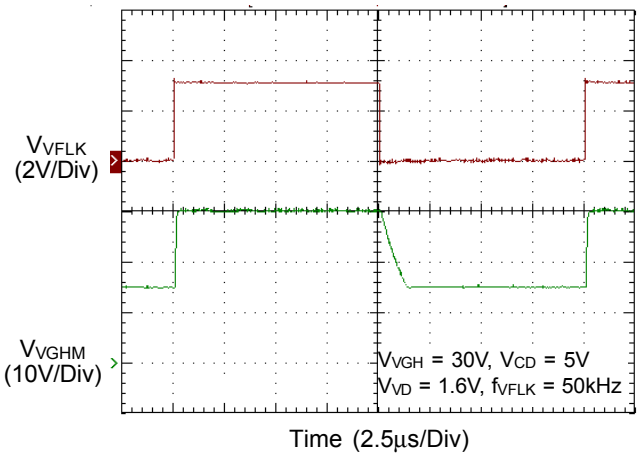
CD Threshold vs. Temperature



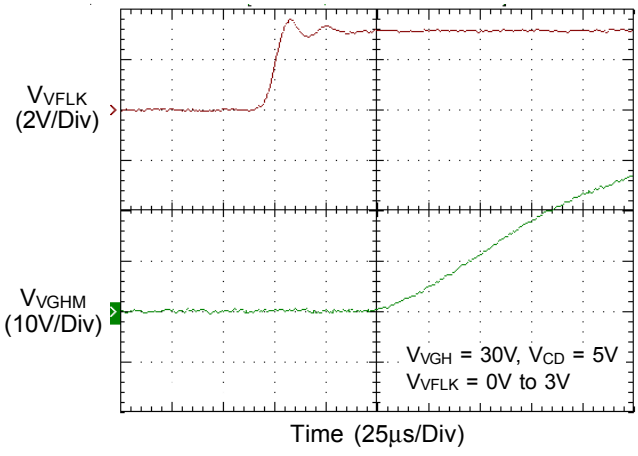
VGHM Start Waveform



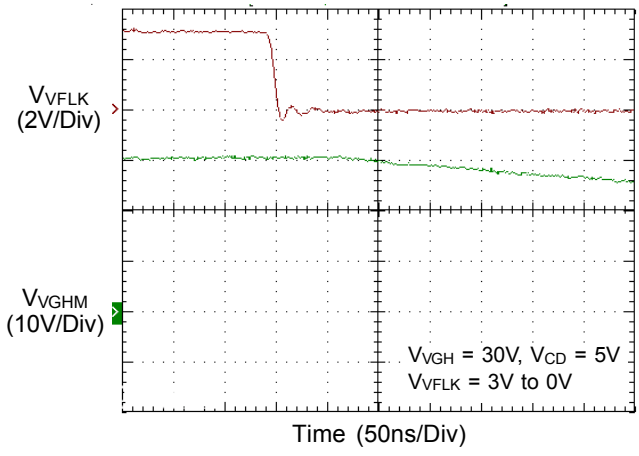
VGHM Falling Regulation Voltage



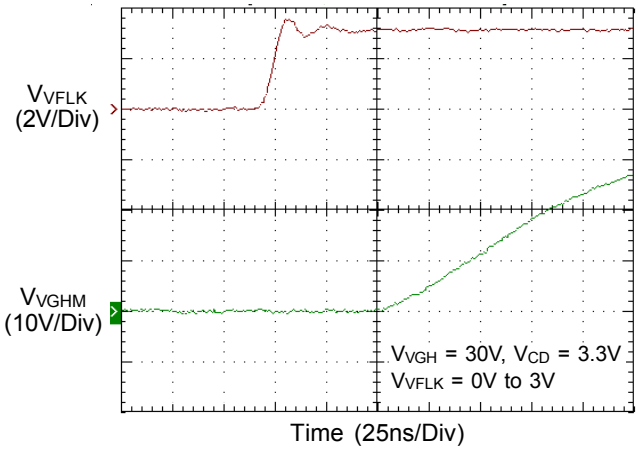
Mode A VGHM Propagation Delay



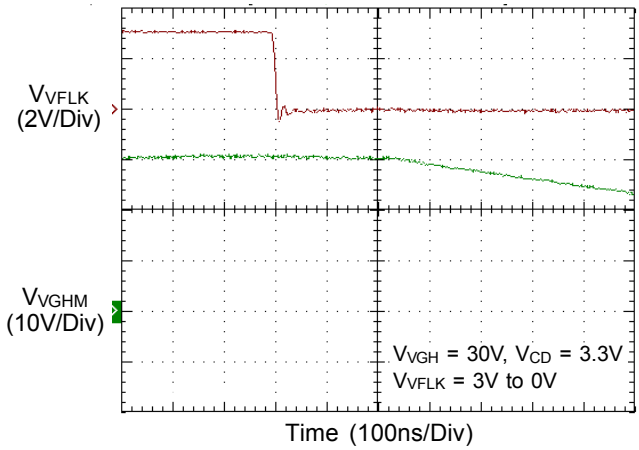
Mode A VGHM Propagation Delay



Mode C VGHM Propagation Delay



Mode C VGHM Propagation Delay



Applications Information

The GPM consists of two high-voltage MOSFETs which include P1 between VGH and VGHM and P2 between VGHM and RE. The switch-control block is enabled when VDPM exceeds V_{REF} and then P1 and P2 are controlled by VFLK and CD. There are three different modes of operation (see the Typical Application Circuit and Timing Diagram).

Activate the Mode A by connecting CD to 5V. When VFLK is logic high, P1 turns on and P2 turns off, VGHM is connected to VGH. When VFLK is logic low, P1 turns off and P2 turns on, VGHM is connected to RE, and VGHM is discharged through the resistor between RE and GND. P2 turns off and stops discharging VGHM when VGHM reaches 10 times the voltage of the VD pin.

When CD is connected with a capacitor, the switch control block works in the Mode B. The rising edge of the VFLK will turns on P1 and turns off P2, connecting VGHM to VGH. An internal N-MOSFET Q3 between CDO and GND is also turned on to discharge the external capacitor between CD and GND. The falling edge of VFLK turns off Q3, and an internal 50μA current source starts charging the CD capacitor. Once V_{CD} exceeds V_{REF}, the switch control circuit turns off P1 and turns on P2, connecting VGHM to RE. VGHM is discharged through the resistor connected between RE and GND. P2 turns off and stops discharging VGHM when VGHM reaches 10 times the voltage of the VD pin.

Activate the Mode C by connecting CD to 3.3V. P1 will be turned on, P2 will be turned off and Q3 will be turned on respectively when VFLK is high. When VFLK is low, Q3 will be turned off and CDO will be pull to the same voltage level as CD through a 1kΩ resistor. P1 and P2 will be turn off and on respectively when comparator detects CDO voltage is greater than 2.5V. VGHM is discharged through the resistor connected between RE and GND. P2 turns off and stops discharging VGHM when VGHM reaches 10 times the voltage of VD pin.

The timing of enabling the switch control block can be adjusted with an external capacitor connected between VDPM and GND. An internal 5μA current source starts charging the VDPM capacitor if all internal power is ready. The voltage on the VDPM linearly rises because of the constant-charging current. When VDPM goes above V_{REF}, the switch control block is enabled.

Output Current Maximum Rating (rms value)

The GPM output current is RMS value and the RMS current boundary depends on ambient temperature with fixed P1 and P2 on-resistance. In figure 6, the test condition is VGH = 30V with R1 = 0Ω and R1 = 43Ω. The boundary is located at 125°C junction temperature for safe operation in SOP-8 package.

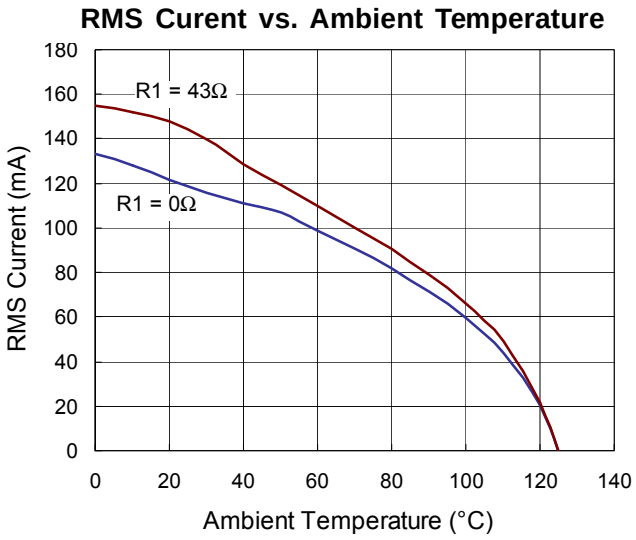


Figure 6. Output Current Maximum Rating vs. Ambient Temperature with R1 = 0Ω and R1 = 43Ω

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOP-8 package, the thermal resistance θ_{JA} is 120°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A =25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C - 25°C) / (120°C/W) = 0.833W for SOP-8 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The Figure 7 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

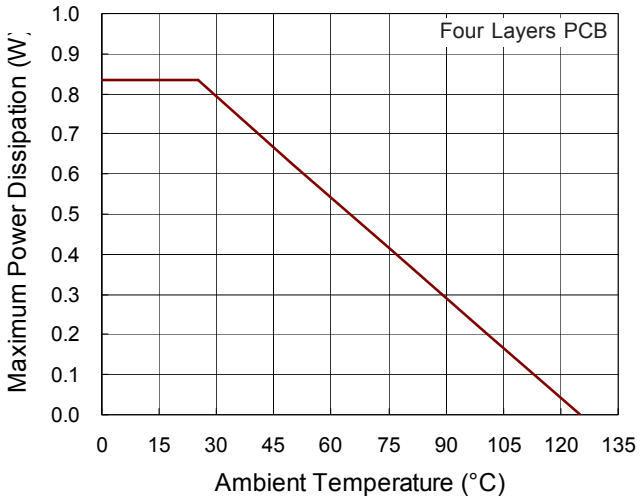
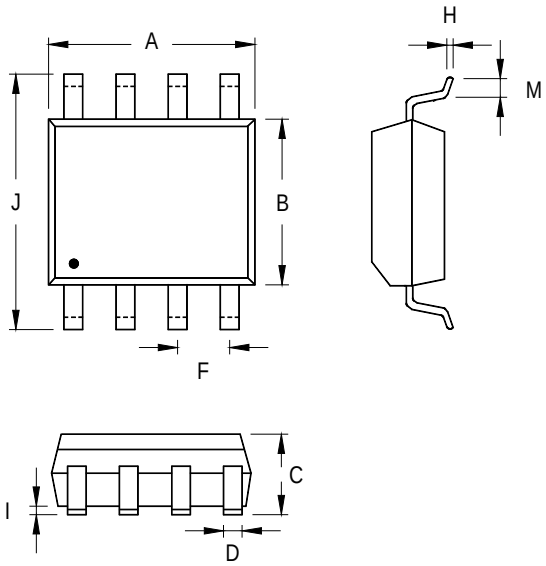


Figure 7. Derating Curve

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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