

2A, Ultra Low Dropout LDO

General Description

The RT9025 is a high performance positive voltage regulator designed for use in applications requiring very low Input voltage and extremely low dropout voltage at up to 2A(Peak). It operates with a VIN as low as 1V and VDD voltage 3V with programmable output voltage as low as 0.8V. The RT9025 features ultra low dropout that is ideal for applications where VOUT is very close to VIN. Additionally, it has an enable pin to further reduce power dissipation while shutdown and provides excellent regulation over variations in line, load and temperature. The RT9025 provides a power good signal to indicate if the voltage level of Vo reaches 90% of its rating value. The RT9025 is available in the SOP-8 and SOP-8 (Exposed Pad) package with 1.05V, 1.2V, 1.5V, 1.8V and 2.5V internally preset outputs that are also adjustable by using external resistors.

Ordering Information

RT9025-□□□□

- Package Type
S : SOP-8
SP : SOP-8 (Exposed Pad-Option 1)
- Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)
Z : ECO (Ecological Element with Halogen Free and Pb free)
- Output Voltage
1K : 1.05V/Adj
12 : 1.2V/Adj
15 : 1.5V/Adj
18 : 1.8V/Adj
25 : 2.5V/Adj

Note :

Richtek products are :

- } RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- } Suitable for use in SnPb or Pb-free soldering processes.

Features

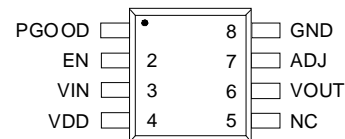
- | Ultra Low Dropout Voltage 230mV at 2A
- | Output Current up to 2A
- | High Accuracy Output Voltage 2%
- | Power Good Output
- | Output Voltage Pull Low Resistor when Disable
- | Over Current Protection
- | Thermal Shutdown Protection
- | RoHS Compliant and 100% Lead (Pb)-Free

Applications

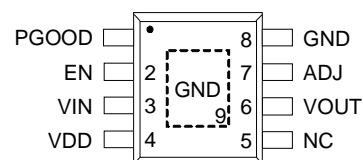
- | Note Book PC Applications
- | Motherboard Applications

Pin Configurations

(TOP VIEW)



SOP-8



SOP-8 (Exposed Pad)

Typical Application Circuit

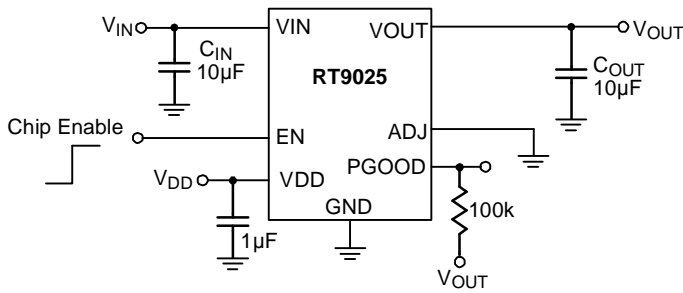


Figure 1. Fixed Voltage Regulator

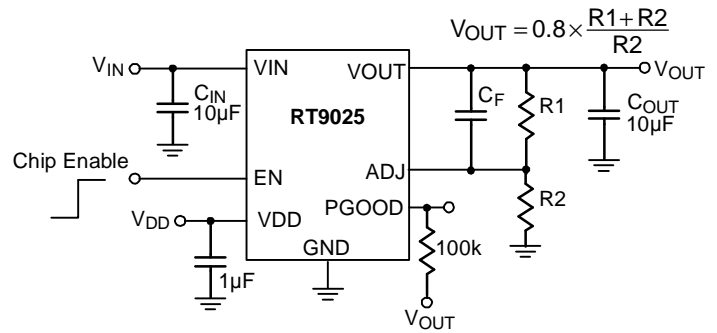
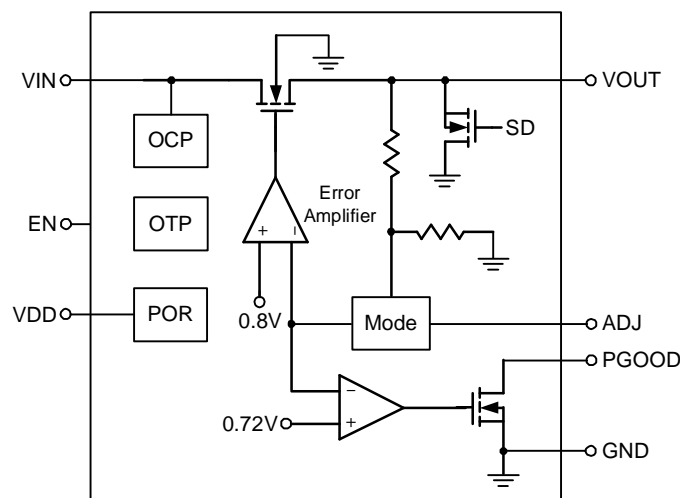


Figure 2. Adjustable Voltage Regulator

Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|--------------------|----------|--|
| 1 | PGOOD | Power Good Open Drain Output. |
| 2 | EN | Chip Enable (Active High). |
| 3 | VIN | Supply Input Voltage. |
| 4 | VDD | Supply Voltage of Control Circuit. |
| 5 | NC | No Internal Connection. |
| 6 | VOUT | Output Voltage. |
| 7 | ADJ | Set the output voltage by the internal feedback resistors when ADJ is grounded. If external feedback resistors is used, $V_{OUT} = 0.8V \times (R2 + R1) / R2$. |
| 8, 9 (Exposed Pad) | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |

Function Block Diagram



Absolute Maximum Ratings (Note 1)

| | |
|---|----------------|
| Supply Input Voltage, V_{IN} ----- | 6V |
| Control Voltage ----- | 6V |
| Output Voltage ----- | 6V |
| Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$ | |
| SOP-8 ----- | 0.833W |
| SOP-8 (Exposed Pad) ----- | 1.333W |
| Package Thermal Resistance (Note 2) | |
| SOP-8, θ_{JA} ----- | 120°C/W |
| SOP-8, θ_{JC} ----- | 60°C/W |
| SOP-8 (Exposed Pad), θ_{JA} ----- | 75°C/W |
| SOP-8 (Exposed Pad), θ_{JC} ----- | 15°C/W |
| Lead Temperature (Soldering, 10 sec.) ----- | 260°C |
| Junction Temperature ----- | 150°C |
| Storage Temperature Range ----- | -65°C to 150°C |
| ESD Susceptibility (Note 3) | |
| HBM (Human Body Mode) ----- | 2kV |
| MM (Machine Mode) ----- | 200V |

Recommended Operating Conditions (Note 4)

| | |
|--------------------------------------|----------------|
| Supply Input Voltage, V_{IN} ----- | 1.4V to 5.5V |
| Control Voltage, V_{DD} ----- | 4.5V to 5.5V |
| Junction Temperature Range ----- | -40°C to 125°C |
| Ambient Temperature Range ----- | -40°C to 85°C |

Electrical Characteristics

($V_{IN} = V_{OUT} + 500\text{mV}$, $V_{EN} = V_{DD} = 5\text{V}$, $C_{IN} = C_{OUT} = 10\mu\text{F}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------------|--|-----|-----|-----|------|
| VIN | | | | | | |
| Quiescent Current (GND Current) (Note 5) | I_Q | $V_{DD} = 5\text{V}$ | -- | 0.6 | 1.2 | mA |
| VDD | | | | | | |
| VDD Operation Range | V_{DD} | V_{DD} Input Range | 4.5 | -- | 5.5 | V |
| VOUT | | | | | | |
| Fixed Output Voltage | | $V_{DD} = 5\text{V}$ | -2 | 0 | 2 | % |
| V_{OUT} Load Regulation (Note 6) | ΔV_{LOAD} | $V_{DD} = 5\text{V}$, $I_{OUT} = 2\text{A}$, $V_{IN} = V_{OUT} + 1\text{V}$ | -- | 0.2 | 1 | % |
| V_{OUT} Line Regulation (V_{IN}) | ΔV_{LINE_IN} | $V_{DD} = 5\text{V}$, $V_{IN} = V_{OUT} + 1\text{V}$ to 5V $I_{OUT} = 1\text{mA}$ | -- | 0.2 | 0.6 | % |
| Dropout Voltage (Note 7) | V_{DROP} | $V_{DD} = 5\text{V}$, $I_{OUT} = 2\text{A}$ | -- | 230 | 300 | mV |
| | | $V_{DD} = 5\text{V}$, $I_{OUT} = 1\text{A}$ | -- | 115 | 150 | |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit | |
|---------------------------------------|------------|---|----------------------------|-----|-------|-------------|---------|
| Current Limit | I_{LIM} | $V_{DD} = 5V, V_{IN} = 3.6V$ | -- | 3.5 | -- | A | |
| Short Circuit Current | | $V_{DD} = 5V, V_{OUT} < 0.2V$ | -- | 1.8 | -- | A | |
| In-rush Current | | $V_{DD} = 5V, C_{OUT} = 10\mu F, \text{Enable Start-up}, I_{LOAD} = 2A$ | -- | 0.5 | -- | A | |
| V_{OUT} Pull Low Resistance | | $V_{EN} = 0V$ | -- | 150 | -- | Ω | |
| V_{OUT} Rising Time | | 10% to 90%, $V_{OUT} = 1.8V$ | -- | 200 | 600 | μs | |
| ADJ | | | | | | | |
| Reference Voltage | V_{REF} | $V_{DD} = 5V, V_{OUT} = 2.5V$ | 0.788 | 0.8 | 0.812 | V | |
| ADJ Pin Threshold | | | -- | 0.2 | -- | V | |
| Power-On Reset | | | | | | | |
| POR Threshold | | | 2.4 | 2.7 | 3.0 | V | |
| POR Falling Hysteresis | | | 0.15 | 0.2 | -- | V | |
| Power Good | | | | | | | |
| Power Good Rising Threshold | | $V_{DD} = 5V$ | -- | 90 | -- | % | |
| Power Good Hysteresis | | $V_{DD} = 5V$ | -- | 10 | -- | % | |
| Power Good Sink Capability | | $V_{DD} = 5V, I_{OUT} = 10mA$ | -- | 0.2 | 0.4 | V | |
| Chip Enable | | | | | | | |
| EN Threshold Voltage | Logic-High | V_{EN_H} | $V_{DD} = 5V$ | 1.2 | -- | -- | V |
| | Logic-Low | V_{EN_L} | $V_{DD} = 5V$ | -- | -- | 0.6 | V |
| EN Pin Bias Current | | I_{EN} | $V_{EN} = 5V$ | -- | 12 | -- | μA |
| V_{DD} Shutdown Current | | I_{SHDN} | $V_{DD} = 5V, V_{EN} = 0V$ | -- | -- | 1 | μA |
| Over Temperature Protection | | | | | | | |
| Thermal Shutdown Temperature | | T_{SD} | -- | 160 | -- | $^{\circ}C$ | |
| Thermal Shutdown Returned Temperature | | | -- | 90 | -- | $^{\circ}C$ | |

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}C$ on a 4-layers high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for SOP-8 (Exposed Pad) package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

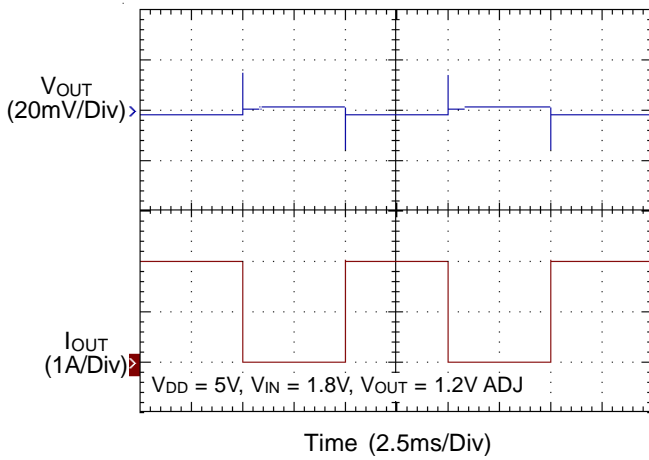
Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition ($I_{OUT} = 0mA$).

Note 6. Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 1mA to 2A.

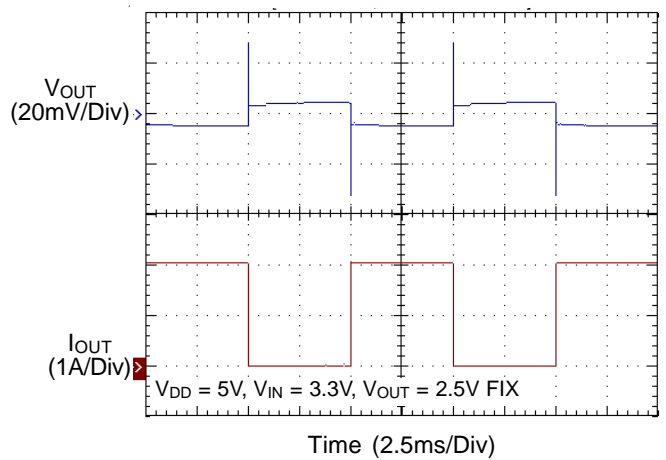
Note 7. The dropout voltage is defined as $V_{IN} - V_{OUT}$, which is measured when V_{OUT} is $V_{OUT(NORMAL)} - 100mV$.

Typical Operating Characteristics

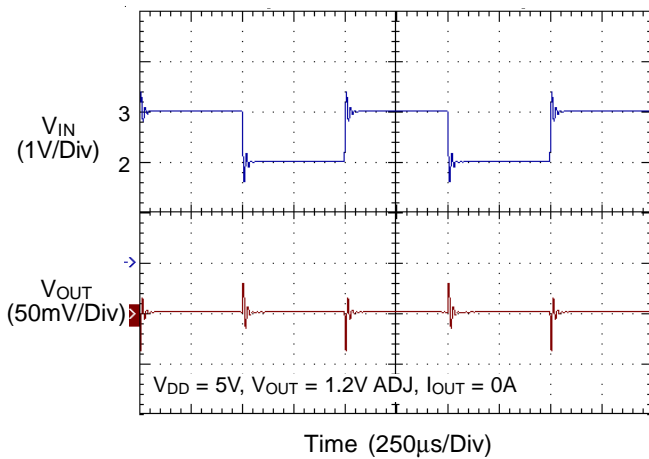
Load Transient Response



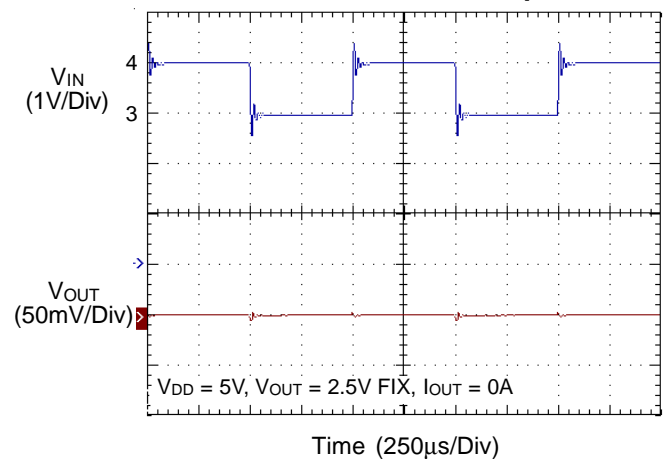
Load Transient Response



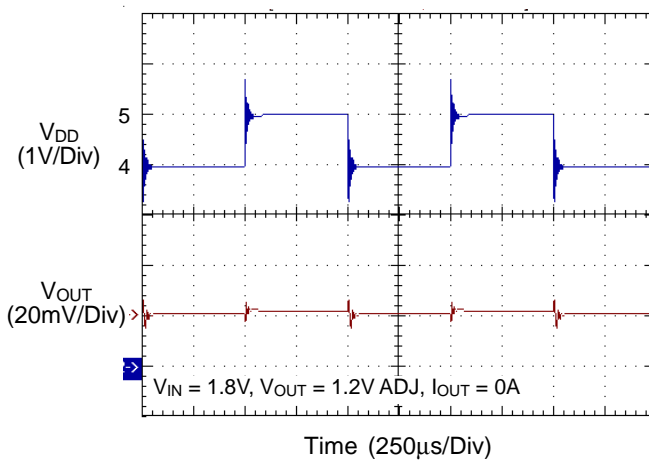
V_{IN} Line Transient Response



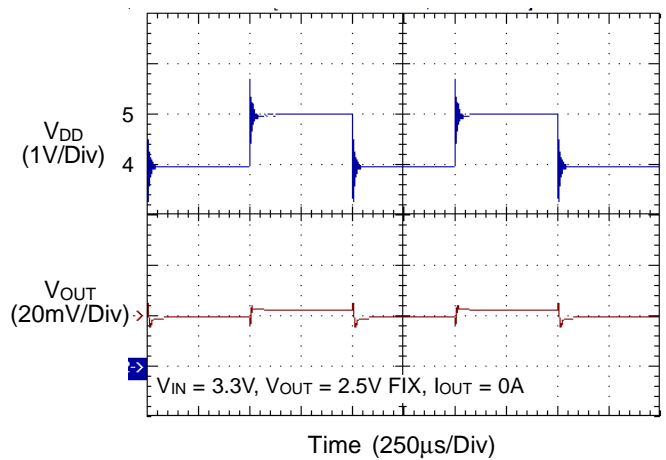
V_{IN} Line Transient Response



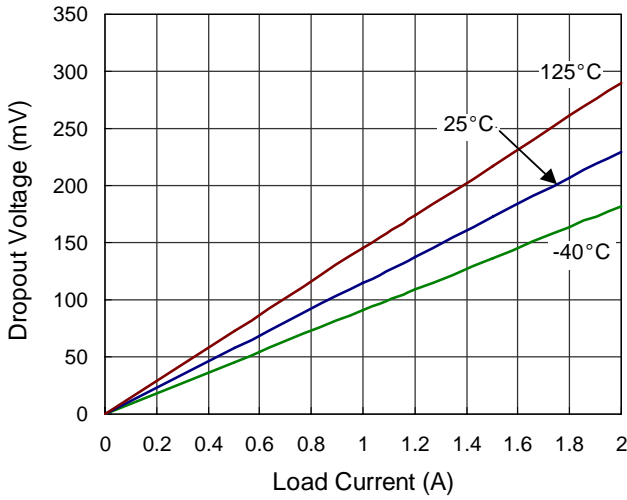
V_{DD} Line Transient Response



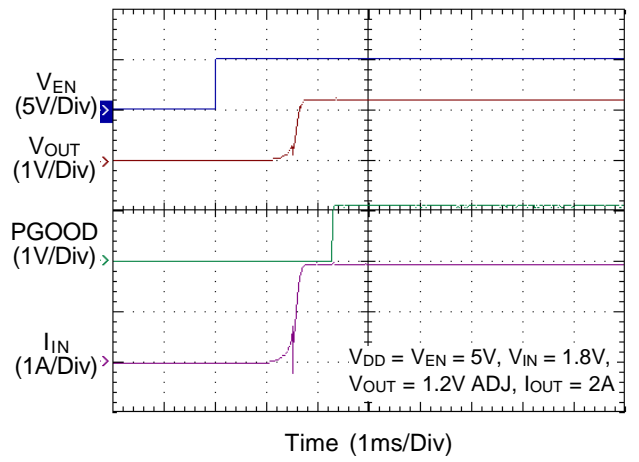
V_{DD} Line Transient Response



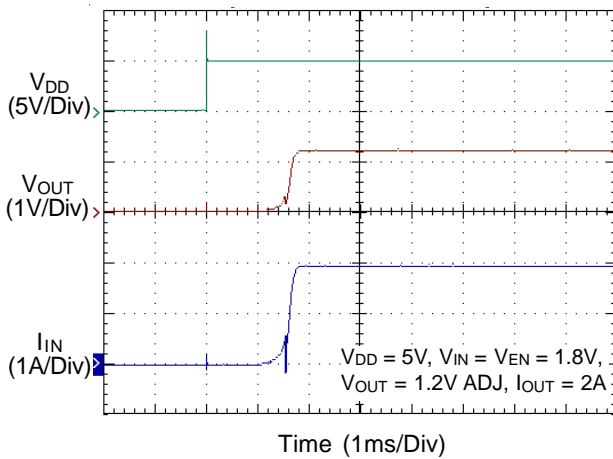
Dropout Voltage vs. Load Current



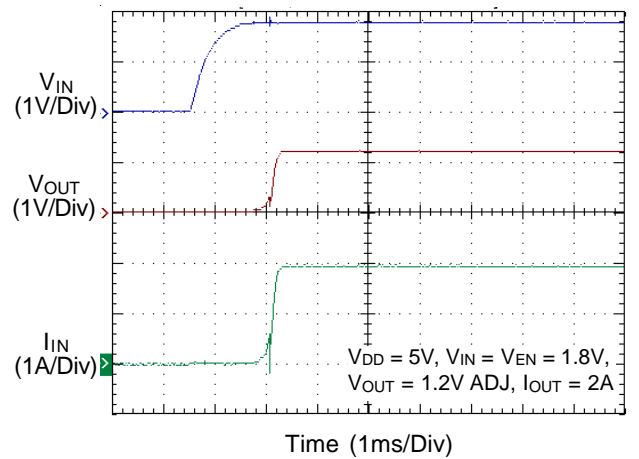
Start Up from Enable and PGOOD Delay



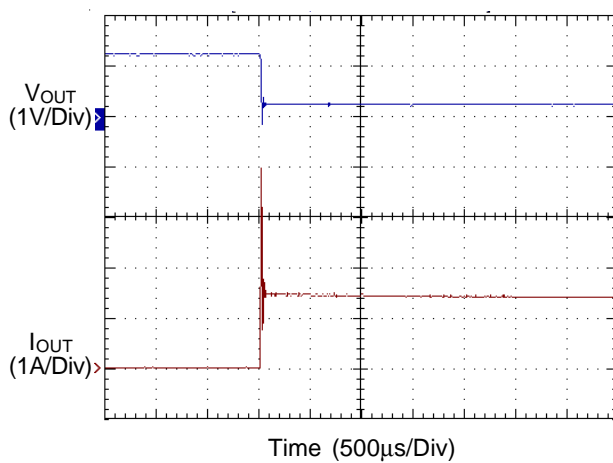
Start Up from V_{DD}



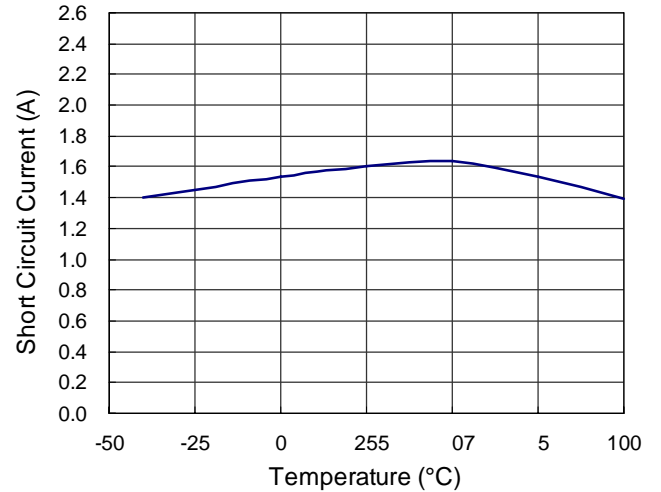
Start Up from V_{IN}



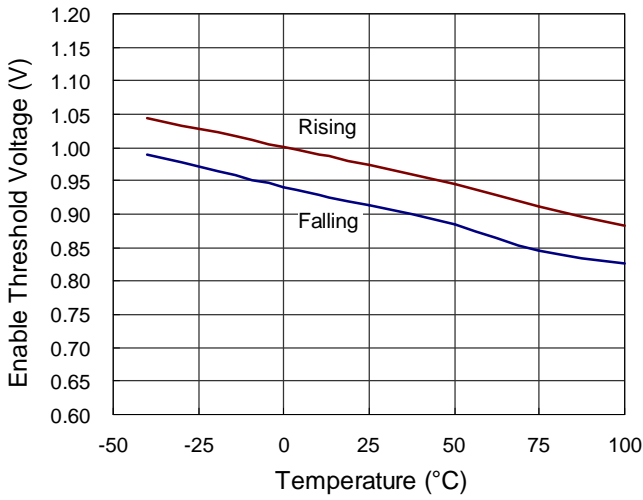
Short Circuit Protection



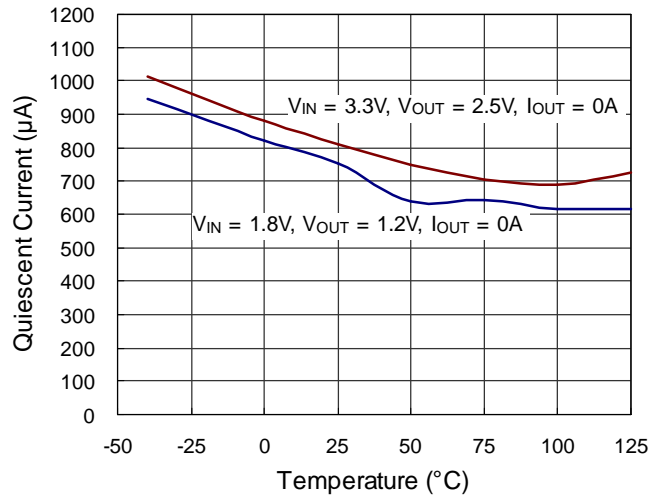
Short Circuit Current vs. Temperature



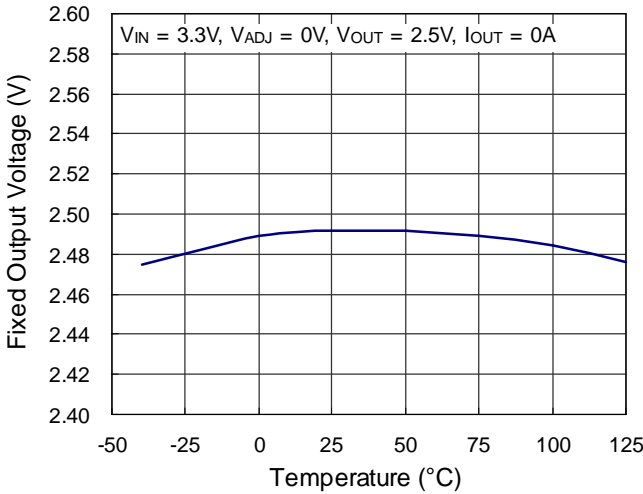
Enable Threshold Voltage vs. Temperature



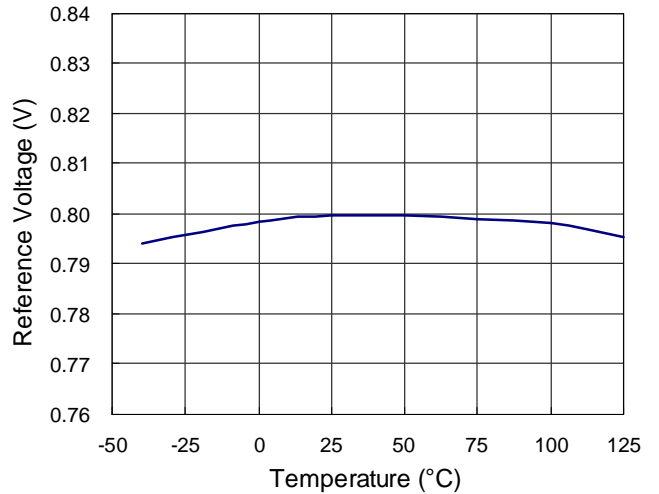
Quiescent Current vs. Temperature



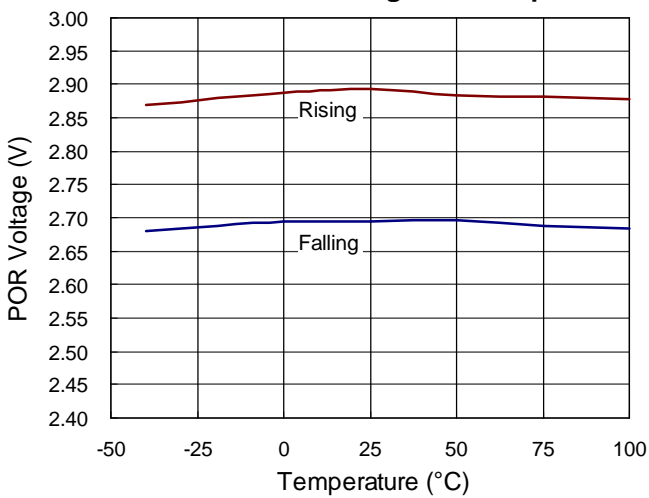
Fixed Output Voltage Range vs. Temperature



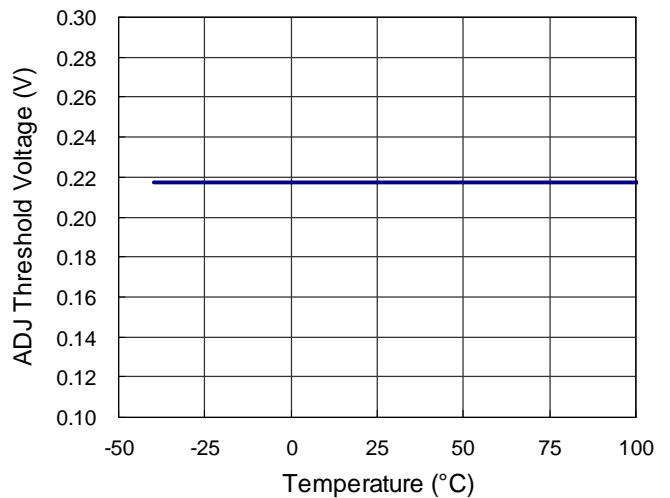
Reference Voltage vs. Temperature



VDD POR Threshold Voltage vs. Temperature



ADJ Threshold Voltage Range vs. Temperature



Application information

Adjustable Mode Operation

The output voltage of RT9025 is adjustable from 0.8V to V_{IN} by external voltage divider resistors as shown in Typical Application Circuit (Figure 2). The value of resistors R1 and R2 should be more than 10kΩ to reduce the power loss. The output voltage can be calculated by the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the reference voltage (0.8V typical).

Enable

The RT9025 goes into shutdown mode when the EN pin is in the logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to 10μA typical. The RT9025 goes into operation mode when the EN pin is in the logic high condition. If the EN pin is floating, please notice the RT9025 internal initial logic level. For RT9025, the EN pin function pulls low level internally. So the regulator will be turn off when EN pin is floating.

Input Capacitor

Good bypassing is recommended from input to ground to improve AC performance. A 10μF input capacitor or greater located as close as possible to the IC is recommended.

Output Capacitor

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9025 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor which value is at least 10μF with ESR is > 15mΩ on the RT9025 output ensures stability. The RT9025 still works well with output capacitor of other types due to the wide stable ESR range. Figure 3 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9025 and returned to a clean analog ground.

Region of Stable C_{OUT} ESR vs. Output Current

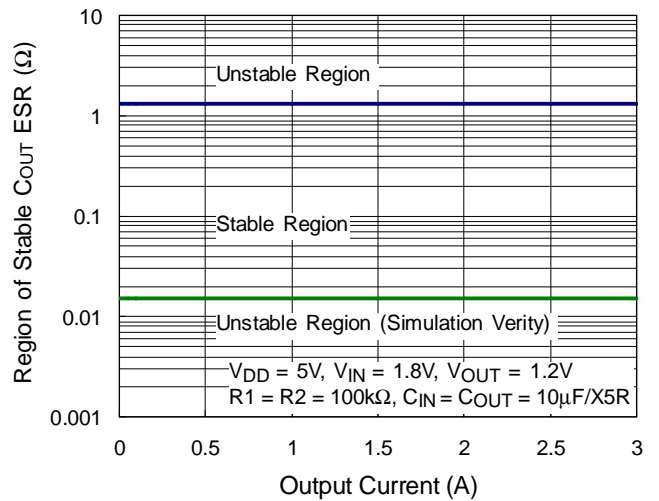


Figure 3. Region of Stable C_{OUT} ESR vs. Output Current

Current Limit

The RT9025 contains an independent current limit and the short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor's gate voltage, limiting the output current to higher than 3.5A typical. When the output voltage is less than 0.2V, the short circuit current protection starts the current fold back function and maintains the loading current 1.8A. The output can be shorted to ground indefinitely without damaging the part.

Power Good

The power good function is an open-drain output. Connects 100kΩ pull up resistor to V_{OUT} to obtain an output voltage. The PGOOD pin will output high immediately after the output voltage arrives 90% of normal output voltage.

Thermal Shutdown Protection

Thermal protection limits power dissipation to prevent IC over temperature in RT9025. When the operation junction temperature exceeds 160°C, the over temperature protection circuit starts the thermal shutdown function and turns the pass transistor off. The pass transistor turns on again after the junction temperature cools by 30°C. RT9025 lowers its OTP trip level from 160°C to 90°C when output short circuit occurs ($V_{OUT} < 0.2V$). It limits

IC case temperature under 100°C and provides maximum safety to customer while output short circuit occurring.

Power Dissipation

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junctions to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

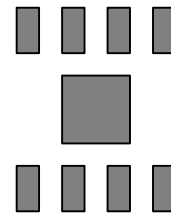
For recommended operating conditions specification of RT9025, the maximum junction temperature is 125°C. The junction to ambient thermal resistance for SOP-8 (Exposed Pad) package is 75°C/W on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The copper thickness is 2oz. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (75^\circ\text{C}/\text{W}) = 1.33\text{W} \text{ (SOP-8 Exposed Pad on the minimum layout)}$$

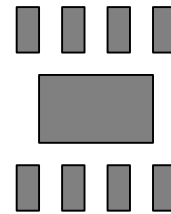
Layout Considerations

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design had been designed. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance θ_{JA} can be decreased by adding a copper under the exposed pad of SOP-8 (Exposed Pad) package.

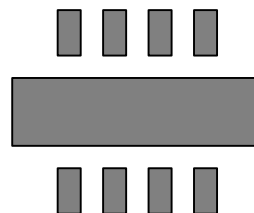
As shown in Figure 4, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 4.a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 4.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm² (Figure 4.e) reduces the θ_{JA} to 49°C/W.



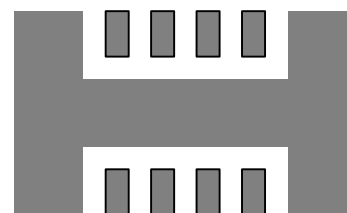
(a) Copper Area = (2.3 x 2.3) mm², $\theta_{JA} = 75^\circ\text{C}/\text{W}$



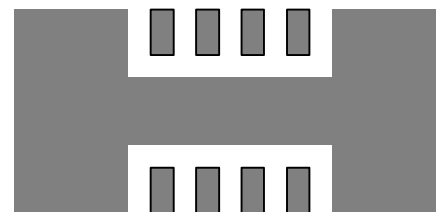
(b) Copper Area = 10mm², $\theta_{JA} = 64^\circ\text{C}/\text{W}$



(c) Copper Area = 30mm², $\theta_{JA} = 54^\circ\text{C}/\text{W}$



(d) Copper Area = 50mm², $\theta_{JA} = 51^\circ\text{C}/\text{W}$



(e) Copper Area = 70mm², $\theta_{JA} = 49^\circ\text{C}/\text{W}$

Figure 4. Thermal Resistance vs. Copper Area Layout Thermal Design

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} . For RT9025 packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

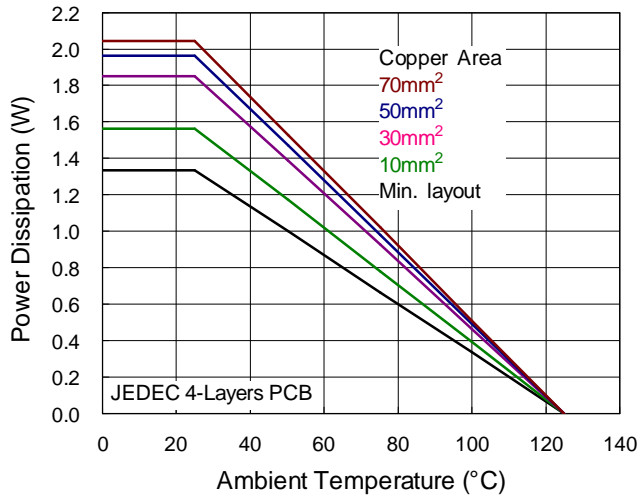
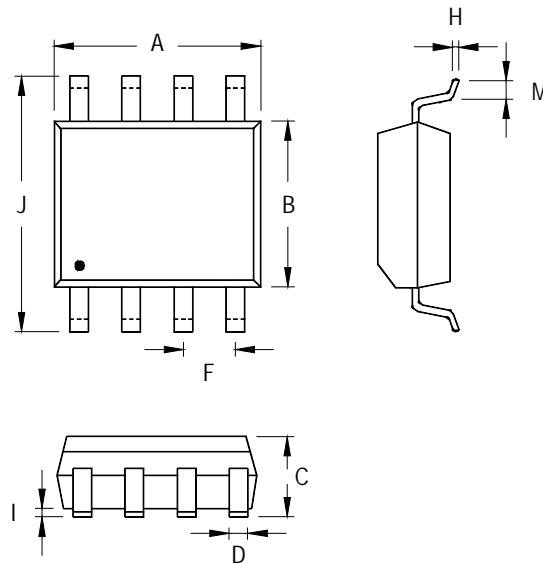


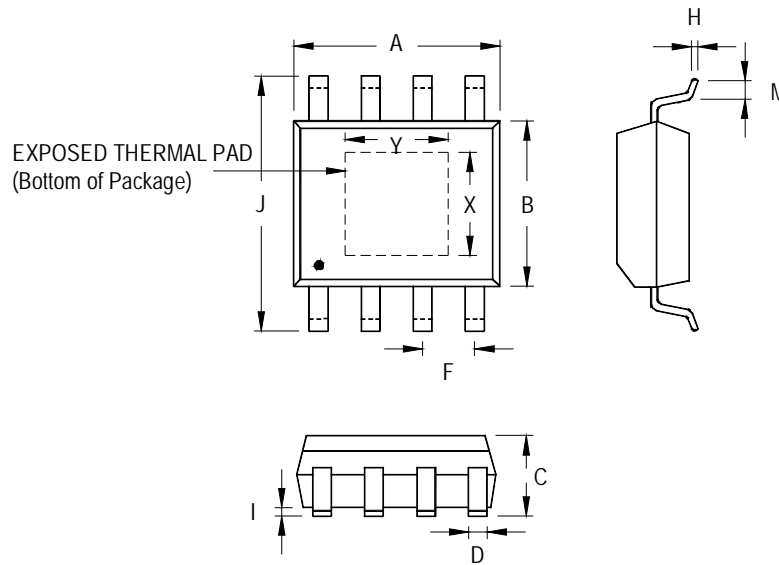
Figure 5. Derating Curve for Package

Outline Dimension



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.170 | 0.254 | 0.007 | 0.010 |
| I | 0.050 | 0.254 | 0.002 | 0.010 |
| J | 5.791 | 6.200 | 0.228 | 0.244 |
| M | 0.400 | 1.270 | 0.016 | 0.050 |

8-Lead SOP Plastic Package



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | | |
|----------|---------------------------|-------|----------------------|-------|-------|
| | Min | Max | Min | Max | |
| A | 4.801 | 5.004 | 0.189 | 0.197 | |
| B | 3.810 | 4.000 | 0.150 | 0.157 | |
| C | 1.346 | 1.753 | 0.053 | 0.069 | |
| D | 0.330 | 0.510 | 0.013 | 0.020 | |
| F | 1.194 | 1.346 | 0.047 | 0.053 | |
| H | 0.170 | 0.254 | 0.007 | 0.010 | |
| I | 0.000 | 0.152 | 0.000 | 0.006 | |
| J | 5.791 | 6.200 | 0.228 | 0.244 | |
| M | 0.406 | 1.270 | 0.016 | 0.050 | |
| Option 1 | X | 2.000 | 2.300 | 0.079 | 0.091 |
| | Y | 2.000 | 2.300 | 0.079 | 0.091 |
| Option 2 | X | 2.100 | 2.500 | 0.083 | 0.098 |
| | Y | 3.000 | 3.500 | 0.118 | 0.138 |

8-Lead SOP (Exposed Pad) Plastic Package

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