SAB3013
Hex 6-Bit DAC

Product Specification

Linear Products

DESCRIPTION

The SAB3013 is a MOS N-channel integrated circuit which provides 6 analog memories controlled by a microcomputer.

FEATURES

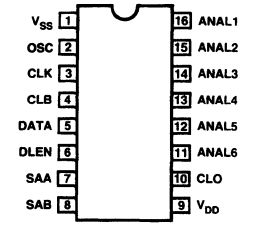
- **Replacement for 6 μP-controlled potentiometers**
- **6-function analog memory; D/A converter with 6-bit resolution**
- **The output of the analog values is pulse-width modulated with adjustable repetition rate (max. 21.8kHz)**
- **Microcomputer-adapted asynchronous serial interface for data input (CBUS)**
- **Parallel operation of up to four SAB3013 circuits is possible**
- **Serial CBUS-controlled**

APPLICATIONS

- **Television receivers**
- **Radio receivers**
- **Computer-controlled TV/radio**
- **Industrial**
- **Instrumentation**

PIN CONFIGURATION

N Package



CD11930S

PIN NO.	SYMBOL	DESCRIPTION	
1	V_{SS}	Ground (0V)	
2	OSC	Oscillator output	
3	CLK	Oscillator input (Schmitt-trigger)	
4	CLB	Asynchronous clock pulse	CBUS
5	DATA	Data input	CBUS
6	DLEN	Data line enable input	CBUS
7	SAA	Address inputs	
8	SAB	Address inputs	
9	V_{DD}	Positive supply	
10	CLO	Buffered oscillator output	
11	ANAL6	Analog outputs	
12	ANAL5	Analog outputs	
13	ANAL4	Analog outputs	
14	ANAL3	Analog outputs	
15	ANAL2	Analog outputs	
16	ANAL1	Analog outputs	

ORDERING INFORMATION

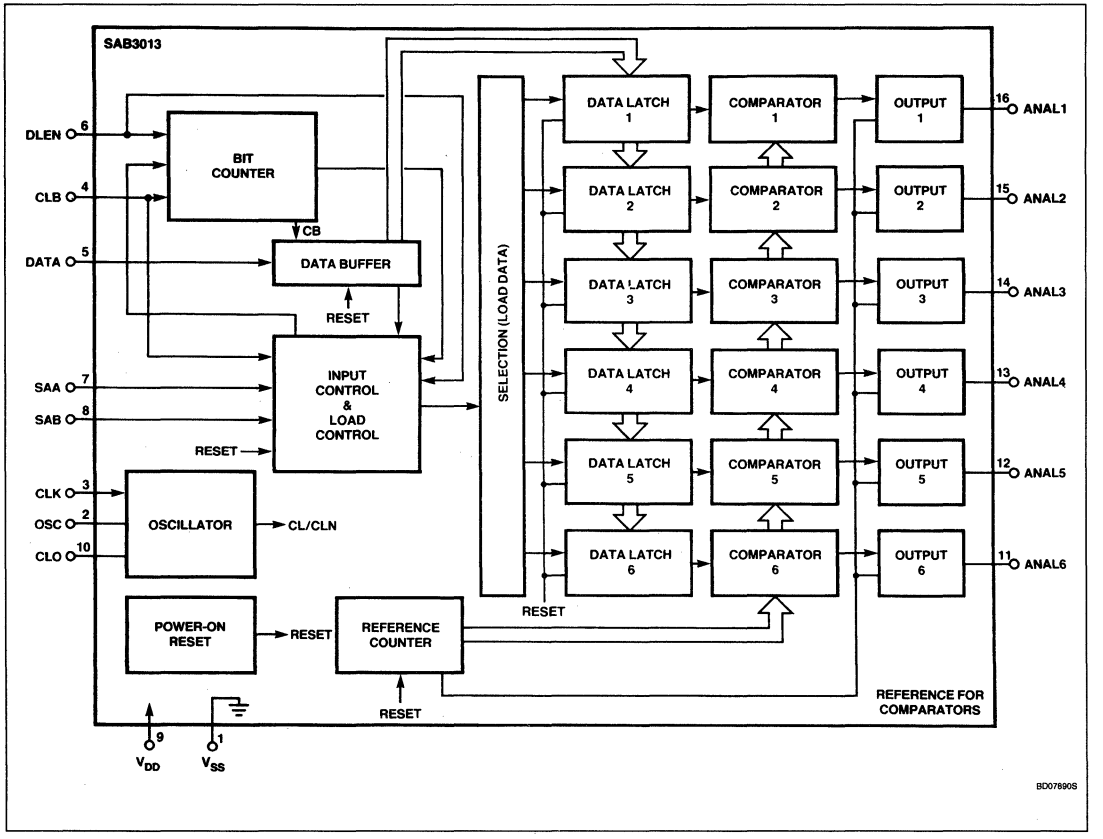
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	0 to 70°C	SAB3013N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.3 to +7.5	V
V_I	Input voltage range	−0.3 to +15	V
$\pm I_I$	Input current	100	μA
V_O	Output voltage (open drain outputs)	V_{SS} to 15	V
$\pm I_O$	Output current (open drain/push-pull outputs)	10	mA
P_O	Power dissipation per output	25	mW
P_{TOT}	Total power dissipation per package	250	mW
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

Hex 6-Bit DAC SAB3013

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS

V_{SS}=0; T_A = 0°C to +70°C; V_{DD} = 4.5 to 5.5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5	5.5	V
I_{DD}	Supply current	V_{DD} = 5.5V			35	mA
Inputs DATA, CLB, DLEN, SAA, SAB						
V_{IL}	Input voltage LOW		−0.3		0.8	V
V_{IH}	Input voltage HIGH		2.0		12	V
I_{IR}	Input leakage current	V_I = −0.3 to +12V			1	μA
Outputs ANAL1 to ANAL6 (open-drain)						
V_{OL}	Output voltage LOW	I_O = 6mA			0.7	V
I_{OR}	Output leakage current	V_{OH} = 15V			20	μA
C_L	Load capacitance				1000	pF
Input CLK						
V_{IL}	Input voltage LOW		−0.3		0.8	V
V_{IH}	Input voltage HIGH		3.5		12	V
I_{IR}	Input leakage current	V_I = −0.3 to 12V			1	μA
t_{WH}	Pulse duration HIGH		355			ns
t_{WL}	Pulse duration LOW		355			ns
Output CLO						
V_{OL}	Output voltage LOW	I_O 500μA			0.8	V
V_{OH}	Output voltage HIGH	$-I_O$ = 100μA	3.5			V
Inputs DATA, CLB						
t_{WH}	Pulse duration HIGH	see Figure 1	450			ns
t_{WL}	Pulse duration LOW	see Figure 1	450			ns
f_{CLB}	Input frequency CLB		0		1	MHz
Internal oscillator CLK/OSC						
R	External resistor		27		1000	kΩ
C	External capacitor		27		1000	pF
f_{CLK}	Clock frequency	R = 27kΩ; C = 27pF	0.7	1.0	1.4	MHz
f_{CLK}	Frequency for external oscillator		0.03		1.4	MHz
Timing (see Figure 1)						
t_{SUDA}	Data setup time DATA → CLB		800			ns
t_{HDDA}	Data hold time DATA → CLB		300			ns
t_{SUEN}	Enable setup time DLEN → CLB	Measured with a voltage swing of minimum $V_{IH} - V_{IL}$	400			ns
t_{SUDI}	Disable setup time CLB → DLEN		400			ns
t_{SULD}	Setup time DLEN → CLB (load pulse)		1000			ns

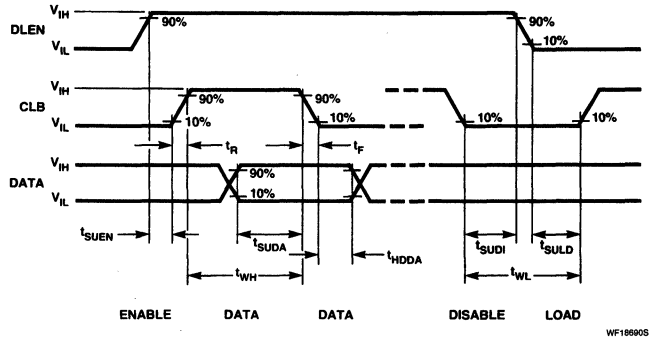


Figure 1. CBUS Timing

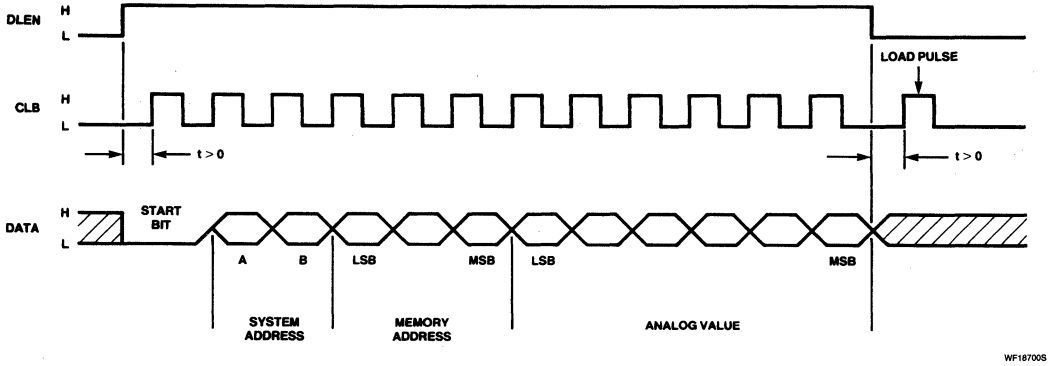


Figure 2. Waveforms Showing a CBUS Transmission

FUNCTIONAL DESCRIPTION

The SAB3013 is designed to deliver analog values in microcomputer-controlled television receivers and radio receivers. The circuit comprises an analog memory and D/A converter for six analog functions with a 6-bit resolution for each. The information for the analog memory is transferred by the microcomputer via an asynchronous serial data bus.

The SAB3013 accomplishes a word format recognition, so it is able to operate one common data bus together with circuits having different word formats.

The data word of the microcomputer used for the SAB3013 consists of information for addressing the appropriate SAB3013 circuit (2 bits), for addressing the analog memories concerned (3 bits) and processing of the wanted analog value (6 bits). The address of the circuit is externally programmable via two inputs. It is possible to address up to four SAB3013 circuits via one common bus.

The built-in oscillator can be used for a frequency between 30kHz and 1.4MHz. The analog values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ (maximum 21.8kHz at f_{CLK} = 1.4MHz), and the analog values are determined by the ratio of the HIGH-time and the cycle time. A DC voltage proportional to the analog value is obtained by means of an external integration network (low-pass filter).

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

OPERATION DESCRIPTION

The data input is achieved serially via the inputs DATA, DLEN and CLB. Clock pulses have to be applied at input CLB for data processing at input DATA. Data processing is only possible when DLEN = HIGH. The data from the data buffer is loaded directly into the output latch on receipt of a load pulse at input CLB (DLEN = LOW), provided the following conditions are met:

- 12 clock pulses must be received at input CLB (word format control) during transmission (DLEN = HIGH)
- The start-bit must be LOW
- The system address bits must be A = SAA and B = SAB
- The analog address must be valid

The data word for the SAB3013 consists of the following bits (see Figure 2):

1 start-bit
2 system address bits (A and B)
3 address bits for selection of the required analog memory
6 data bits for processing the analog value

ADDRESS INPUTS (SAA, SAB)

The address of the SAB3013 is programmed at the inputs SAA and SAB. These inputs must be defined and not left open-circuit.

Reset

The circuit internally generates a reset cycle with a duration of one clock cycle after switching on the supply. If a spike on the supply is likely to destroy data, a reset signal will be generated. All analog memories are set to 50% (analog value 32/64) after the reset cycle. The supply voltage rise dV_{DD}/dt must be maximum 0.5V/μs and minimum 0.2V/μs.

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