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Always order by complete part number: **SLA7042M**



# SLA7042M AND SLA7044M

## MICROSTEPPING, UNIPOLAR PWM, HIGH-CURRENT MOTOR CONTROLLER/DRIVERS

**DC ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$  unless otherwise noted.**

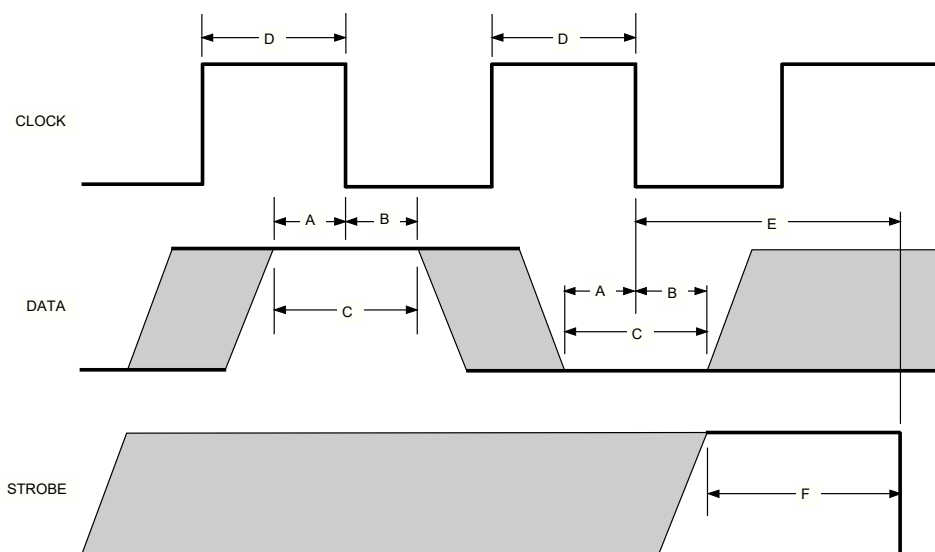
Characteristic	Symbol	Test Conditions	Limits			
			Min	Typ	Max	Units
FET Leakage Current	$I_{DSS}$	$V_{DS} = 100\text{ V}$	—	—	4.0	mA
FET ON Voltage	$V_{DS(ON)}$	SLA7042M, $I_{OUT} = 1.2\text{ A}$	—	—	800	mV
		SLA7044M, $I_{OUT} = 3\text{ A}$	—	—	855	mV
FET ON Resistance	$r_{DS(on)}$	SLA7042M, $I_{OUT} = 1.2\text{ A}$	—	—	0.67	$\Omega$
		SLA7044M, $I_{OUT} = 3\text{ A}$	—	—	0.285	$\Omega$
Body Diode Forward Voltage	$V_{SD}$	SLA7042M, $I_{OUT} = -1.2\text{ A}$	—	—	1.2	V
		SLA7044M, $I_{OUT} = -3\text{ A}$	—	—	1.6	V
Control Supply Voltage	$V_{DD}$	Operating	4.5	5.0	5.5	V
Control Supply Current	$I_{DD}$	Each controller, $V_{DD} = 5.5\text{ V}$	—	—	7.0	mA
Logic Input Voltage	$V_{IN(1)}$		3.5	—	—	V
	$V_{IN(0)}$		—	—	1.5	V
Logic Input Current	$I_{IN(1)}$	$V_{IN(1)} = V_{DD}$	—	—	1.0	$\mu\text{A}$
	$I_{IN(0)}$	$V_{IN(0)} = 0$	—	—	-1.0	$\mu\text{A}$
REF/ENABLE Input Voltage	$V_{REF/EN}$	DATA, CLOCK, STROBE, and OUT Enabled	0.4	—	2.5	V
		DATA, CLOCK, STROBE, and OUT Disabled	$V_{DD} - 1$	—	—	V
REF/ENABLE Input Current	$I_{REF/EN}$	$0\text{ V} \leq V_{REF/EN} \leq 5\text{ V}$	—	—	$\pm 1.0$	$\mu\text{A}$
Step Reference Current Ratio  First Bit Entered (X) = Phase Second Bit Entered = LSB Last Bit Entered = MSB	SRCR	DATA Input = 000X	—	0	—	%
		DATA Input = 001X	—	20	—	%
		DATA Input = 010X	—	40	—	%
		DATA Input = 011X	—	55.5	—	%
		DATA Input = 100X	—	71.4	—	%
		DATA Input = 101X	—	83	—	%
		DATA Input = 110X	—	91	—	%
		DATA Input = 111X	—	100	—	%

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

## TYPICAL AC CHARACTERISTICS at $T_A = +25^\circ\text{C}$ , $V_{DD} = 5\text{ V}$ , $I_{OUT} = 1\text{ A}$ , Logic Levels are $V_{DD}$ and Ground

PWM OFF Time		DATA Input = 001X	7 $\mu\text{s}$
		DATA Input = 010X	7 $\mu\text{s}$
		DATA Input = 011X	9 $\mu\text{s}$
		DATA Input = 100X	9 $\mu\text{s}$
		DATA Input = 101X	9 $\mu\text{s}$
		DATA Input = 110X	11 $\mu\text{s}$
		DATA Input = 101X	11 $\mu\text{s}$
Output RiseTime	$t_r$	10% to 90%	0.5 $\mu\text{s}$
Output Fall Time	$t_f$	90% to 10%	0.1 $\mu\text{s}$
Strobe-to-Output Switching Time	$t_{pd}$	50% to 50%	0.7 $\mu\text{s}$

# SLA7042M AND SLA7044M MICROSTEPPING, UNIPOLAR PWM, HIGH-CURRENT MOTOR CONTROLLER/DRIVERS



Dwg. WK-002

## SERIAL PORT TIMING CONDITIONS

( $T_A = +25^\circ\text{C}$ , Logic Levels are  $V_{DD}$  and Ground)

A. Minimum Data Active Time Before Clock Falling Edge (Data Set-Up Time) .....	150 ns
B. Minimum Data Active Time After Clock Falling Edge (Data Hold Time) .....	150 ns
C. Minimum Data Pulse Width .....	350 ns
D. Minimum Clock Pulse Width .....	350 ns
E. Minimum Time Between Clock and Strobe Falling Edges .....	650 ns
F. Minimum Strobe Pulse Width .....	500 ns

## APPLICATIONS INFORMATION

The SLA7042M and SLA7044M modules integrate two CMOS controller ICs and four NMOS FETs. Each half of the device operates independently, although the CLOCK inputs may be connected together and the STROBE inputs may be connected together. Pulling  $V_{REF/EN}$  low (<2.5 V) allows the 4-bit shift registers to be serially loaded with motor phase and output current ratioing data.

The first bit selects the motor phase (logic high = Output A or B, logic low = Output A or B); the next three bits determine the motor current ratio (eight steps, 0% to 100%). The internal D/A converter, in conjunction with a current-sensing resistor and input reference voltage, completes the microstepping current control.

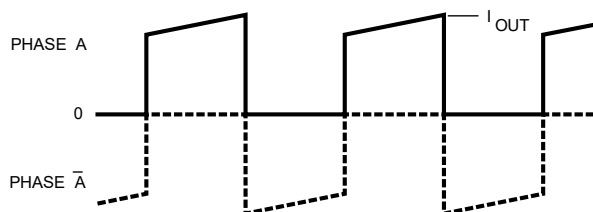
Pulling  $V_{REF/EN}$  high (within 1 V of  $V_{DD}$ ) resets the shift register and latches to turn the MOS drivers OFF and inhibits the serial DATA input.

# SLA7042M AND SLA7044M MICROSTEPPING, UNIPOLAR PWM, HIGH-CURRENT MOTOR CONTROLLER/DRIVERS

## REGULATING THE PWM OUTPUT CURRENT

The output current (and motor coil current) waveform is illustrated in Figure 1. Setting the maximum PWM current trip point to meet the specified full-step running current for the motor,  $I_{OUT\ max}$  (DATA input = 111X = 100% ratio), requires only a current-sensing resistor,  $R_S$ , and an input reference voltage,  $V_{REF/EN}$ , between 0.4 V and 2.5 V.

$$I_{OUT\ max} \approx \frac{V_{REF/EN}}{3 \cdot R_S}$$



Dwg. WK-001

FIGURE 1. PHASE A COIL CURRENT WAVEFORM

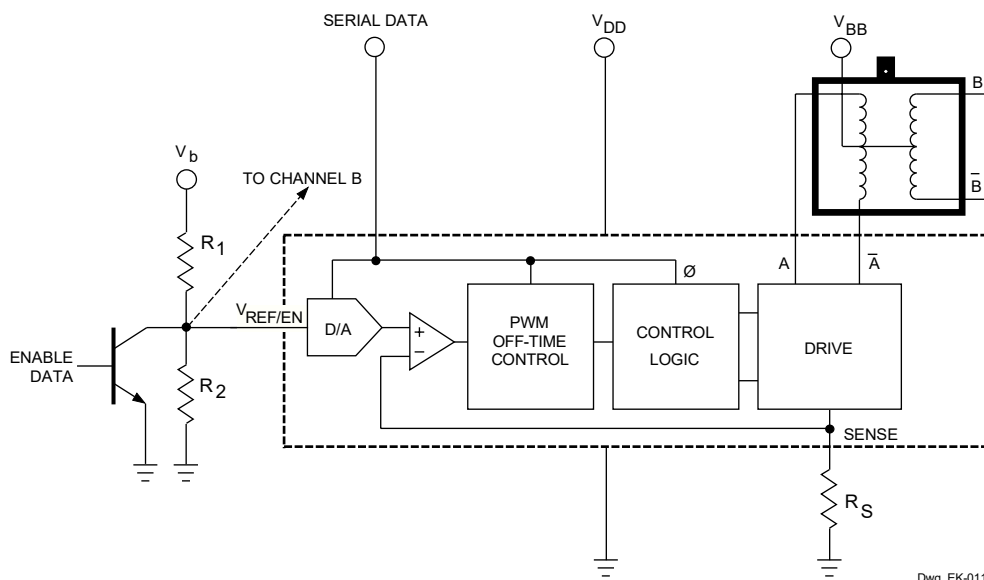
## SERIAL DATA INPUT ENABLE

In a minimum-component application, a voltage divider provides  $V_{REF/EN}$  and an npn transistor provides the required pull-down to enable the serial data input as shown in Figure 2.

$$I_{OUT\ max} \approx \frac{R_2}{R_1 + R_2} \cdot \frac{V_b}{3 \cdot R_S}$$

## μP STEPPER MOTOR CONTROL

Alternative REFERENCE/ENABLE input configurations provide for more complete motor control. A tri-state logic element and a voltage divider allows a fixed reference voltage, with both output disable and data enable functions. Complete μP control is usually accomplished with a D/A converter as shown in Figure 3. Here, digital control provides an output disable ( $>V_{DD} - 1\ V$ ),  $V_{REF}$ , and  $V_{EN}$  ( $<2.5\ V$ ).



Dwg. EK-011

FIGURE 2. PWM CONTROL (RUN MODE)

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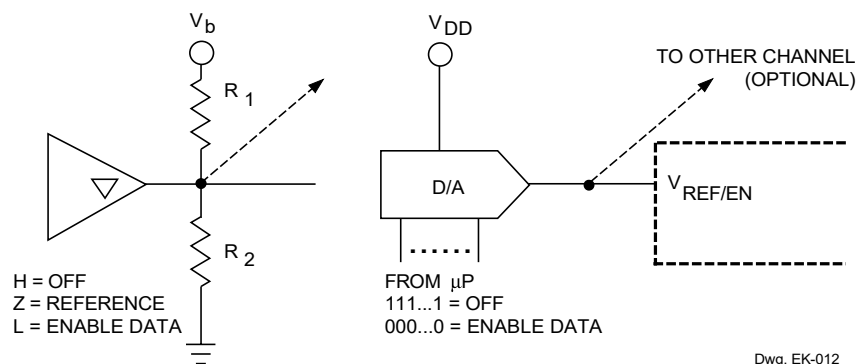


FIGURE 3. COMPLETE CONTROL

## SERIAL DATA INPUT

The serial DATA input port is enabled (active low) by the REFERENCE/ENABLE input. When  $V_{REF/EN}$  is between 0.4 V and 2.5 V, information on the DATA input is read into the shift register on each high-to-low transition of the CLOCK.

There are four bits: the first bit entered controls the

motor phase — a high level enables  $OUT_A$  or  $OUT_B$ , a low level enables  $OUT_{\bar{A}}$  or  $OUT_{\bar{B}}$ . The next three bits set the step reference voltage ratio and PWM OFF time as shown in the Characteristics Tables — the least-significant bit first and the most-significant bit last.

Data written into the serial data port is latched and becomes active on a high-to-low transition at STROBE.

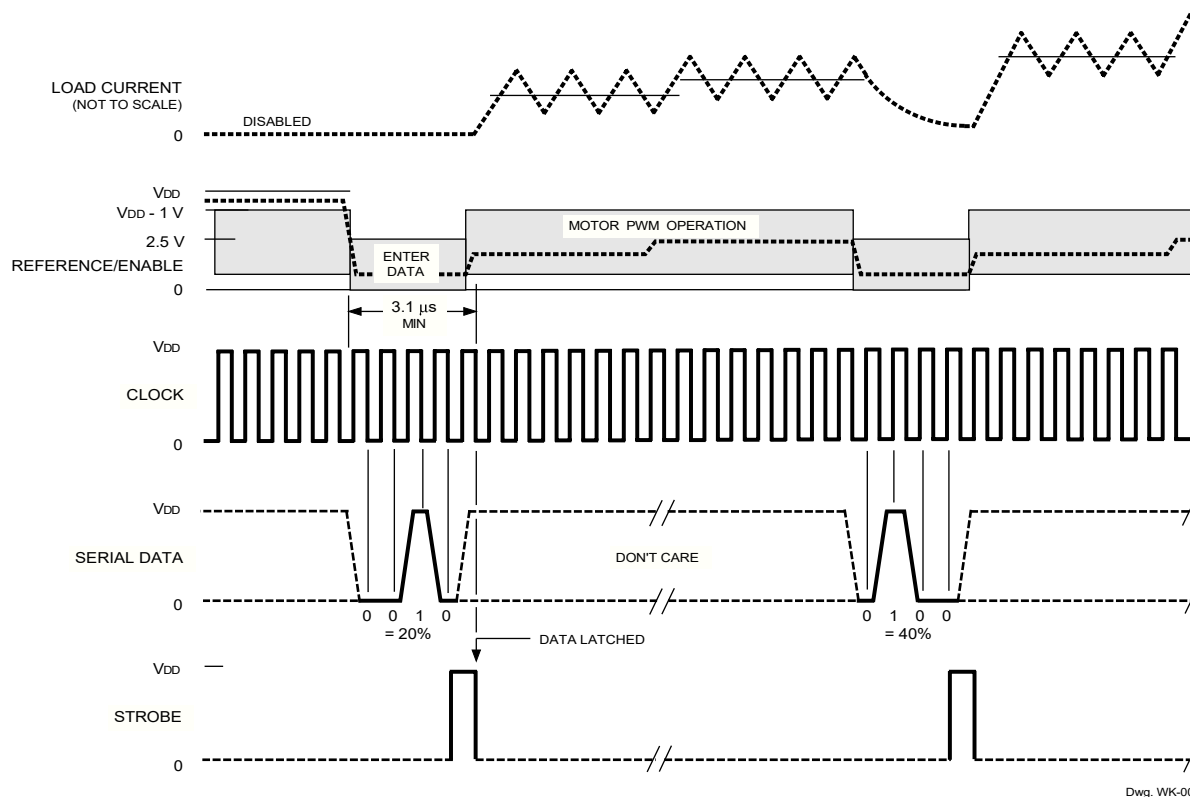


FIGURE 4. TIMING RELATIONSHIPS

# SLA7042M AND SLA7044M MICROSTEPPING, UNIPOLAR PWM, HIGH-CURRENT MOTOR CONTROLLER/DRIVERS

## REFERENCE/ENABLE INPUT

The serial DATA input port is enabled (active low) by the REFERENCE/ENABLE input when  $V_{REF/EN}$  is between 0.4 V and 2.5 V. With  $V_{REF/EN}$  greater than  $V_{DD} - 1$  V, the serial DATA input port is disabled, the outputs are OFF, and the controller/driver will not be affected by changes at the DATA, CLOCK, or STROBE inputs.

With  $V_{REF/EN}$  between 0.4 V and 2.5 V, the output current limit is a linear function of  $V_{REF}$  and the step reference current ratio.

$$I_{OUT} \approx \frac{V_{REF}}{3 \cdot R_S} \cdot SRCR$$

In a typical (SLA7042M) application where  $V_{DD} = 5$  V, a  $V_{REF/EN}$  between 0.4 V and 2.5 V, and a maximum allowable load current of 1.2 A, the maximum value of  $R_S$  is  $0.69 \Omega$  and  $I_{OUT\_min}$  is 0.11 A when SRSCR is 100% (DATA input = 111X).

## POWER DISSIPATION CALCULATIONS

The SLA7042/44M normally do not require special heat sinking except under unusual circumstances (two phases operating near maximum output current and  $T_A > 65^\circ\text{C}$ ). However, as with all power drivers, the basic constituents of power dissipation should be evaluated. Conduction losses (internal power dissipation) include:

- (a) FET output power dissipation ( $I_{OUT}^2 \cdot r_{DS(on)}$  or  $I_{OUT} \cdot V_{DS(ON)}$ ),
- (b) FET body diode power dissipation ( $V_{SD} \cdot I_{OUT}$ ), and
- (c) control circuit power dissipation ( $V_{DD} \cdot I_{DD}$ ).

## PACKAGE RATINGS/DERATING FACTORS

Thermal calculations must also consider the temperature effects on the output FET ON resistance. The applicable thermal ratings for the 18-lead power-tab SIP PMCM package are:

$R_{\theta JA} = 28^\circ\text{C/W}$  (junction to ambient with no heat sink)  
or 4.5 W at  $+25^\circ\text{C}$  and a derating factor of  $-36 \text{ mW}/^\circ\text{C}$   
for operation above  $+25^\circ\text{C}$ .

$R_{\theta JM} = 5^\circ\text{C/W}$  (junction to mounting surface).

## TEMPERATURE EFFECTS ON FET $r_{DS(on)}$

Analyzing safe, reliable operation includes a concern for the relationship of NMOS ON resistance to junction temperature. Device package power calculations must include the increase in ON resistance (producing higher output ON voltages) caused by higher operating junction temperatures. Figure 5 provides a normalized ON resistance curve, and all thermal calculations should consider increases from the given  $+25^\circ\text{C}$  limits, which may be caused by internal heating during normal operation.

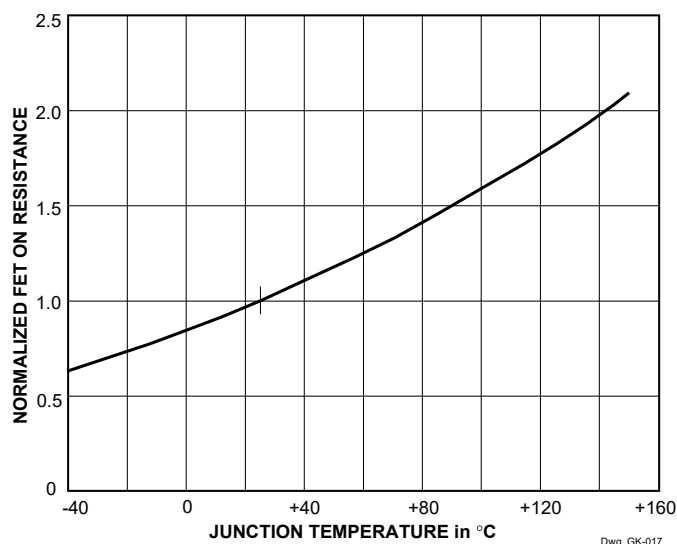
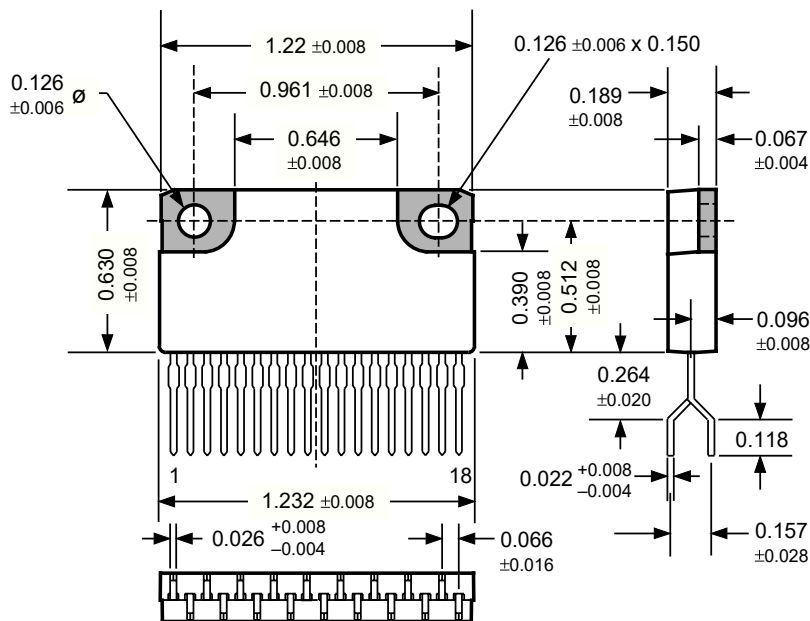


FIGURE 5. NORMALIZED ON RESISTANCE  
vs TEMPERATURE

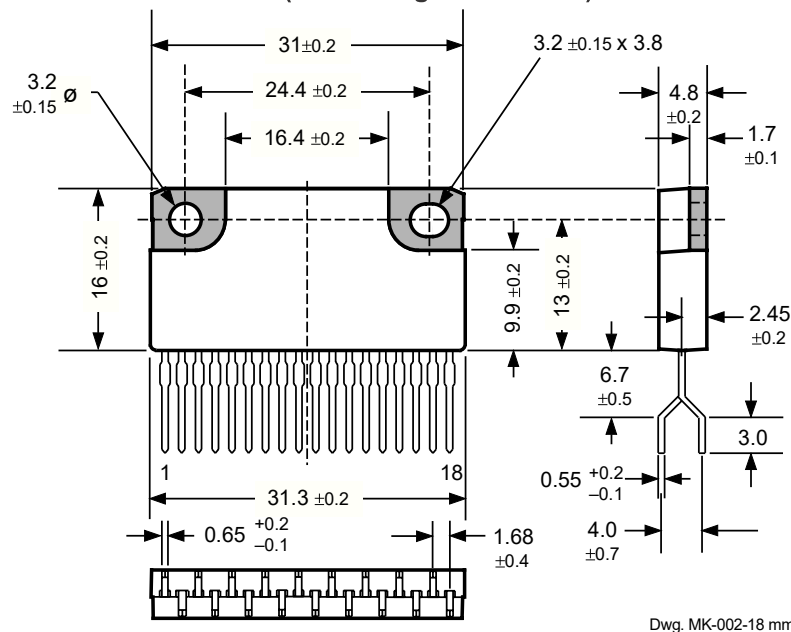
The power MOSFET outputs of these devices are similar to the International Rectifier type IRL510 (SLA7042M) and IRL520 (SLA7044M). These devices feature an excellent combination of fast switching, ruggedized device design, low on-resistance, and cost effectiveness.

# SLA7042M AND SLA7044M MICROSTEPPING, UNIPOLAR PWM, HIGH-CURRENT MOTOR CONTROLLER/DRIVERS

Dimensions in Inches  
(for reference only)



Dimensions in Millimeters  
(controlling dimensions)



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NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.

2. Recommended mounting hardware torque: 4.34 – 5.79 lbf•ft (6 – 8 kgf•cm or 0.588 – 0.784 Nm).

3. The shaded area is exposed (electrically isolated) heat spreader.

4. Recommend use of metal-oxide-filled, alkyl-degenerated oil base, silicone grease (Dow Corning 340 or equivalent).