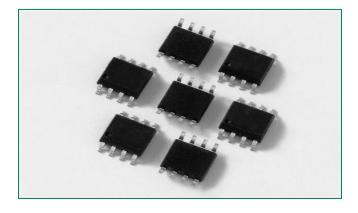


Po

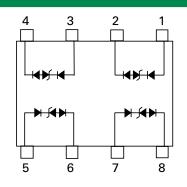
GREEN

RoHS

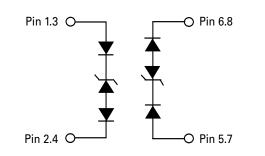
# SLVU2.8-4 Series 2.8V 40A TVS Array



### Pinout



### **Functional Block Diagram**



### Additional Information







# Description

The SLVU2.8-4 was designed to protect low voltage, CMOS devices from ESD and lightning induced transients. There is a compensating diode in series with each low voltage TVS to present a low loading capacitance to the line being protected. These robust structures can safely absorb repetitive ESD strikes at  $\pm 30$ kV (contact discharge) per IEC 61000-4-2 standard and each structure can safely dissipate up to 40A (IEC 61000-4-5 2nd edition, t<sub>P</sub>=8/20µs) with very low clamping voltages.

### Features

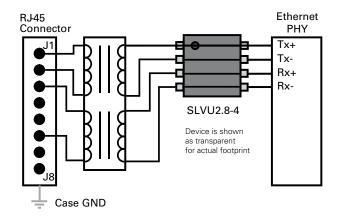
- ESD, IEC 61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC 61000-4-4, 40A (5/50ns)
- Lightning, IEC 61000-4-5 2nd edition, 40A (8/20µs)
- Low capacitance of 2pF per line
- Low leakage current of 1µA (MAX) at 2.8V
- SOIC-8 (JEDEC MO-012) pin configuration allows for simple flow-through layout
- RoHS Compliant and Lead Free
- Moisture Sensitivity Level
  (MSL-1)

# Applications

- 10/100/1000 Ethernet
- WAN/LAN Equipment
- Switching Systems
- Desktops, Servers, and Notebooks
- Base Stations

Analog Inputs

### Application Example



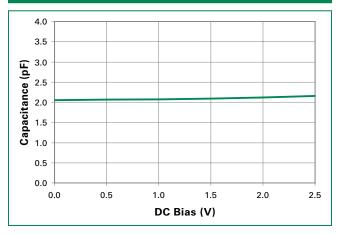
Electrical Characteristics (T <sub>OP</sub> = 25°C)						
Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Reverse Standoff Voltage	V <sub>RWM</sub>	I <sub>R</sub> ≤1μA			2.8	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>τ</sub> =2μA	3.0			V
Snap Back Voltage	V <sub>SB</sub>	I <sub>T</sub> =50mA	2.8			V
Reverse Leakage Current	I <sub>LEAK</sub>	V <sub>R</sub> =2.8V (Each Line)			1	μA
Clamping Voltage <sup>1</sup>	V <sub>c</sub>	I <sub>PP</sub> =5A, t <sub>P</sub> =8/20μs (Each Line)		7.0	8.5	V
Clamping Voltage <sup>1</sup>	V <sub>c</sub>	I <sub>PP</sub> =24A, t <sub>P</sub> =8/20μs (Each Line)		13.9	15.0	V
ESD Withstand Voltage <sup>1</sup>		IEC61000-4-2 (Contact)	±30			kV
	V <sub>ESD</sub>	IEC61000-4-2 (Air)	±30			kV
Dynamic Resistance	R <sub>DYN</sub>	(V <sub>C2</sub> - V <sub>C1</sub> ) / (I <sub>PP2</sub> - I <sub>PP1</sub> ) (Each Line)		0.4		Ω
Diode Capacitance <sup>1</sup>	CD	V <sub>R</sub> =0V, f=1MHz (Each Line)		2.0	2.5	pF

Note: 1Parameter is guaranteed by design and/or device characterization.

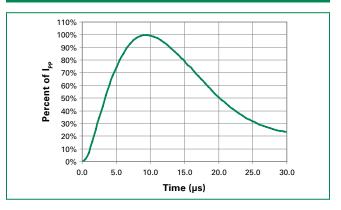
Absolute Maximum Ratings					
Parameter	Rating	Units			
Peak Pulse Power (t <sub>P</sub> =8/20µs)	600	W			
Peak Pulse Current (t <sub>P</sub> =8/20µs)	40	А			
Operating Temperature	–40 to 125	°C			
Storage Temperature	–55 to 150	°C			

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

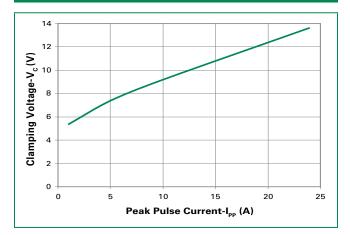
# Figure 1: Capacitance vs. Reverse Voltage



# Figure 3: 8/20 µs Pulse Waveform



# Figure 2: Clamping Voltage vs. I<sub>PP</sub>





Product Characteristics			
Lead Plating	Matte Tin		
Lead Material	Copper Alloy		
Lead Coplanarity	0.0004 inches (0.102mm)		
Substitute Material	Silicon		
Body Material	V-0 per UL 94 Molded Epoxy		

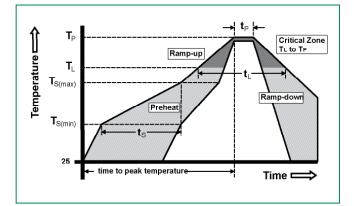
Notes

- All dimensions are in millimeters
  Dimensions include solder plating.

- Dimensions include solder plating.
  Dimensions are exclusive of mold flash & metal burr.
  All specifications comply to JEDEC SPEC MO-203 Issue A
  Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
  Package surface matte finish VDI 11-13.

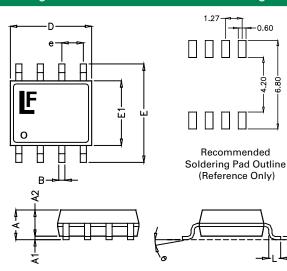
# **Soldering Parameters**

Reflow Condition		Pb – Free assembly	
	-Temperature Min (T <sub>s(min)</sub> )	150°C	
Pre Heat	-Temperature Max (T <sub>s(max)</sub> )	200°C	
	-Time (min to max) (t <sub>s</sub> )	60 – 180 secs	
Average ramp up rate (Liquidus) Temp (T <sub>L</sub> ) to peak		5°C/second max	
T <sub>S(max)</sub> to T	- Ramp-up Rate	5°C/second max	
Reflow	-Temperature $(T_L)$ (Liquidus)	217°C	
nellow	-Temperature (t <sub>L</sub> )	60 – 150 seconds	
PeakTemp	erature (T <sub>P</sub> )	260 <sup>+0/-5</sup> °C	
Time within 5°C of actual peak Temperature (t <sub>p</sub> )		20 – 40 seconds	
Ramp-down Rate		5°C/second max	
Time 25°C to peak Temperature (T <sub>P</sub> )		8 minutes Max.	
Do not exceed		260°C	



# Package Dimensions – Mechanical Drawings and Recommended Solder Pad Outline

oluce PLANE

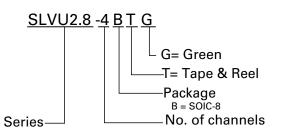


Package	SOIC-8			
Pins	8			
JEDEC	MS-012			
	Millin	netres	Inc	hes
	Min	Max	Min	Max
Α	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.050	0.065
В	0.31	0.51	0.012	0.020
C	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
Е	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
е	1.27	BSC	0.050	BSC
L	0.40	1.27	0.016	0.050

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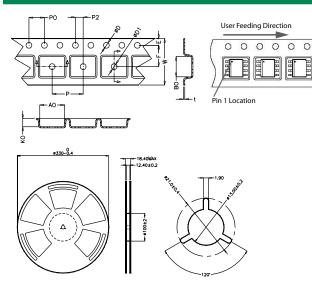


# Part Numbering System



Ordering Information					
Part Number	Package	Marking	Min. Order Qty.		
SLVU2.8-4BTG	SOIC-8	U2.8-4	2500		

### Embossed Carrier Tape & Reel Specification - SOIC Package



Symbol	Millimetres		Inches		
	Min	Max	Min	Max	
E	1.65	1.85	0.065	0.073	
F	5.4	5.6	0.213	0.22	
P2	1.9	2.1	0.075	0.083	
D	1.5	1.6	0.059	0.063	
D1	1.50 Min		0.059 Min		
P0	3.9	4.1	0.154	0.161	
10P0	40.0 ± 0.20		1.574 ± 0.008		
W	11.9	12.1	0.468	0.476	
Р	7.9	8.1	0.311	0.319	
A0	6.3	6.5	0.248	0.256	
B0	5.1	5.3	0.2	0.209	
К0	2	2.2	0.079	0.087	
t	0.30 ± 0.05		0.012 ±	± 0.002	

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# Part Marking System

