

# SN5485, SN54LS85, SN54S85 SN7485, SN74LS85, SN74S85 4-BIT MAGNITUDE COMPARATORS

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TYPE	TYPICAL POWER DISSIPATION	TYPICAL DELAY (4-BIT WORDS)
'85	275 mW	23 ns
'LS85	52 mW	24 ns
'S85	365 mW	11 ns

SN5485, SN54LS85, SN54S85 . . . J OR W PACKAGE  
SN7485 . . . N PACKAGE  
SN74LS85, SN74S85 . . . D OR N PACKAGE  
(TOP VIEW)



## description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

SN54LS85, SN54S85 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A2 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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logic diagrams (positive logic)



logic symbol †



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for D, J, N, and W packages.



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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54' SN54S'	SN54LS'	SN74' SN74S'	SN74LS'	UNIT
Supply voltage, $V_{CC}$ (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Interemitter voltage (see Note 2)	5.5		5.5		V
Operating free-air temperature range	-55 to 125		-0 to 70		°C
Storage temperature range	-65 to 150		-65 to 150		°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
 2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A input in conjunction with its respective B input of the '85 and 'S85.

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**recommended operating conditions**

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	-400			-400			$\mu A$
Low-level output current, $I_{OL}$	16			16			mA
Operating free-air temperature, $T_A$	-55			125			$^{\circ}C$

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{IH}$	High-level input voltage		2			V
$V_{IL}$	Low-level input voltage				0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu A$	2.4	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2	0.4		V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	High-level input current	A < B, A > B inputs			40	$\mu A$
		all other inputs			120	
$I_{IL}$	Low-level input current	A < B, A > B inputs			-1.6	mA
		all other inputs			-4.8	
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX}, V_O = 0$	SN5485	-20	-55	mA
			SN7485	-18	-55	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX},$ See Note 4		55	88	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$ .

§ Not more than one output should be shorted at a time.

NOTE 4:  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$**

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any A or B data input	A < B, A > B	1	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Note 5		7		ns
			2		12			
		3	17		26			
		4	23		35			
$t_{PHL}$	Any A or B data input	A < B, A > B	1		11			ns
			2		15			
		3	20		30			
		A = B	4		20	30		
$t_{PLH}$	A < B or A = B	A > B	1		7	11	ns	
$t_{PHL}$	A < B or A = B	A > B	1		11	17	ns	
$t_{PLH}$	A = B	A = B	2		13	20	ns	
$t_{PHL}$	A = B	A = B	2		11	17	ns	
$t_{PLH}$	A > B or A = B	A < B	1		7	11	ns	
$t_{PHL}$	A > B or A = B	A < B	1		11	17	ns	

¶  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.



**recommended operating conditions**

	SN54LS85			SN74LS85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS <sup>†</sup>	SN54LS85		SN74LS85		UNIT
			MIN	TYP <sup>‡</sup>	MAX	MIN	
$V_{IH}$	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage			0.7		0.7	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5		-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4	2.7	3.4	V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4	V
		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$			0.35	0.5	
$I_I$	Input current at maximum input voltage	A < B, A > B inputs	0.1		0.1		mA
		all other inputs	0.3		0.3		
$I_{IH}$	High-level input current	A < B, A > B inputs	20		20		$\mu$ A
		all other inputs	60		60		
$I_{IL}$	Low-level input current	A < B, A > B inputs	-0.4		-0.4		mA
		all other inputs	-1.2		-1.2		
$I_{OS}$	Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20	-100	-20	-100	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 4}$	10.4	20	10.4	20	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4:  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$**

PARAMETER <sup>†</sup>	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any A or B data input	A < B, A > B	1	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Note 5}$		14		ns
			2			19		
			3			24	36	
			4			27	45	
$t_{PHL}$	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
			4			23	45	
$t_{PLH}$	A < B or A = B	A > B	1			14	22	ns
$t_{PHL}$	A < B or A = B	A > B	1			11	17	ns
$t_{PLH}$	A = B	A = B	2			13	20	ns
$t_{PHL}$	A = B	A = B	2			13	26	ns
$t_{PLH}$	A > B or A = B	A < B	1		14	22	ns	
$t_{PHL}$	A > B or A = B	A < B	1		11	17	ns	

<sup>†</sup> $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

**SN5485, SN54LS85, SN54S85  
SN7485, SN74LS85, SN74S85  
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**recommended operating conditions**

	SN54S85			SN74S85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-1			-1	mA
Low-level output current, $I_{OL}$			20			20	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{IH}$	High-level input voltage		2			V
$V_{IL}$	Low-level input voltage				0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S85 2.5	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	High-level input current	A < B, A > B inputs	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		50	$\mu\text{A}$
		all other inputs			150	
$I_{IL}$	Low-level input current	A < B, A > B inputs	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-2	mA
		all other inputs			-6	
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ , See Note 4		73	115	mA
		$V_{CC} = \text{MAX}, T_A = 125^\circ\text{C}$ , See Note 4	SN54S85W			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4:  $I_{CC}$  is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$**

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any A or B data input	A < B, A > B	1	$C_L = 15 \text{ pF}, R_L = 280 \Omega,$ See Note 5		5		ns
			2		7.5			
		3	10.5		16			
		4	12		18			
$t_{PHL}$	Any A or B data input	A < B, A > B	1		5.5		ns	
			2		7			
		3	11		16.5			
		4	11		16.5			
$t_{PLH}$	A < B or A = B	A > B	1			5	7.5	ns
$t_{PHL}$	A < B or A = B	A > B	1			5.5	8.5	ns
$t_{PLH}$	A = B	A = B	2		7	10.5	ns	
$t_{PHL}$	A = B	A = B	2		5	7.5	ns	
$t_{PLH}$	A > B or A = B	A < B	1		5	7.5	ns	
$t_{PHL}$	A > B or A = B	A < B	1		5.5	8.5	ns	

¶  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.





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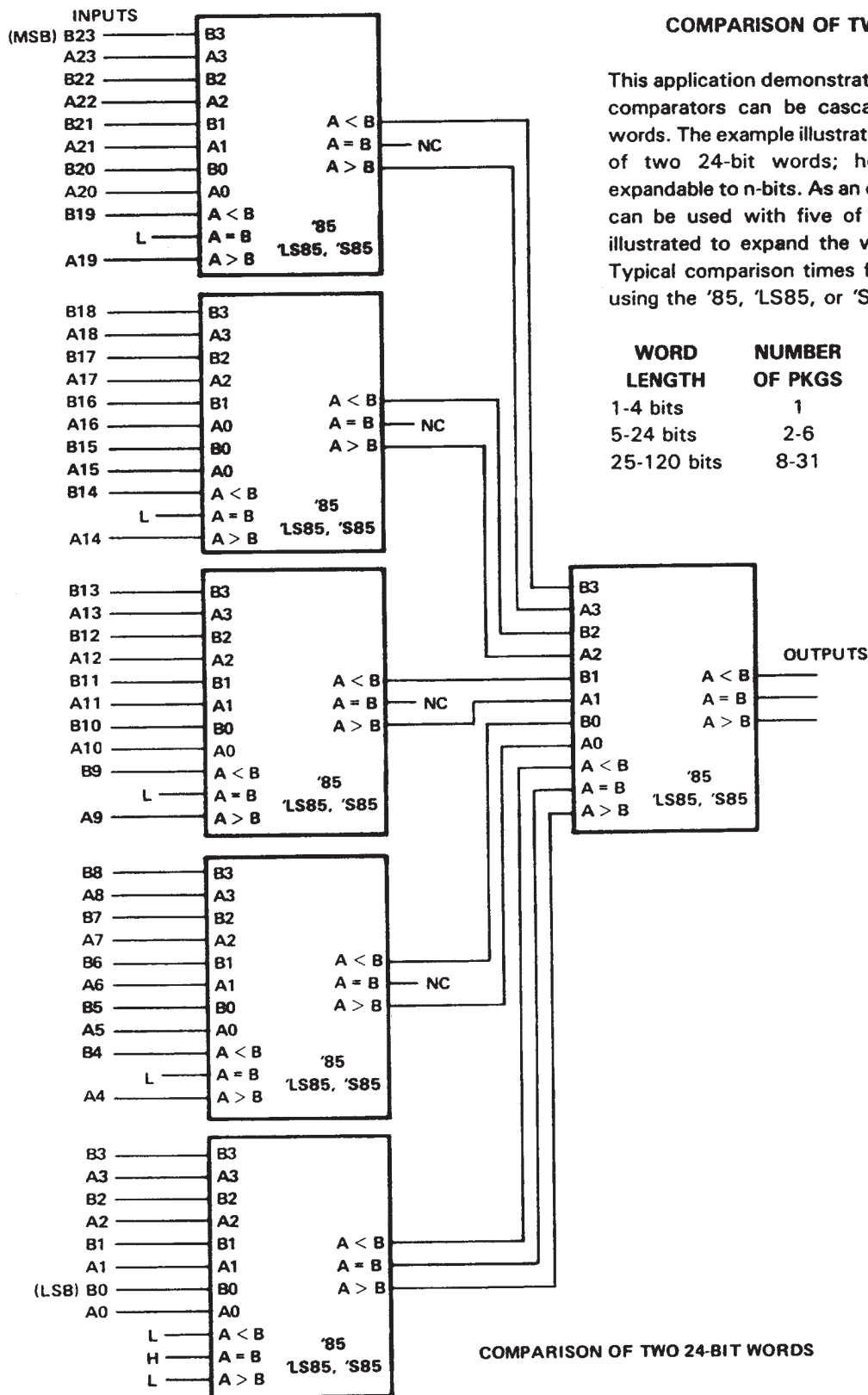
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**TYPICAL APPLICATION DATA**

**COMPARISON OF TWO N-BIT WORDS**

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the '85, 'LS85, or 'S85 are:

WORD LENGTH	NUMBER OF PKGS	'85	'LS85	'S85
1-4 bits	1	23 ns	24 ns	11 ns
5-24 bits	2-6	46 ns	48 ns	22 ns
25-120 bits	8-31	69 ns	72 ns	33 ns



**COMPARISON OF TWO 24-BIT WORDS**



**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS85DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS85NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS85DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS85NSR	SO	NS	16	2000	367.0	367.0	38.0

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