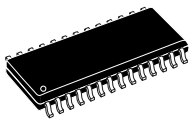
ST8004

SMARTCARD INTERFACE

- 3 OR 5 V SUPPLY FOR THE IC
- STEP-UP CONVERTER FOR V_{CC} GENERATION
- 3 SPECIFIC PROTECTED HALF DUPLEX BI-DIRECTIONAL BUFFERED I/O LINES
- AUTOMATIC ACTIVATION AND DEACTIVATION SEQUENCES
- THERMAL AND SHORT-CIRCUIT PROTECTIONS ON ALL CARD CONTACTS
- 26 MHz INTEGRATED CRYSTAL OSCILLATOR
- CLOCK GENERATION FOR THE CARD UP TO 20MHz WITH SYNCHRONOUS FREQUENCY CHANGES
- ISO7816-3 COMPATIBLE
- ENHANCED ESD PROTECTION ON CARD SIDE
- SO-28 PACKAGE
- UNDER VOLTAGE LOCKOUT PROTECTION SELECTABLE TO 3V OR 2.2V
- SUPPLY SUPERVISOR INTEGRATED



SOP

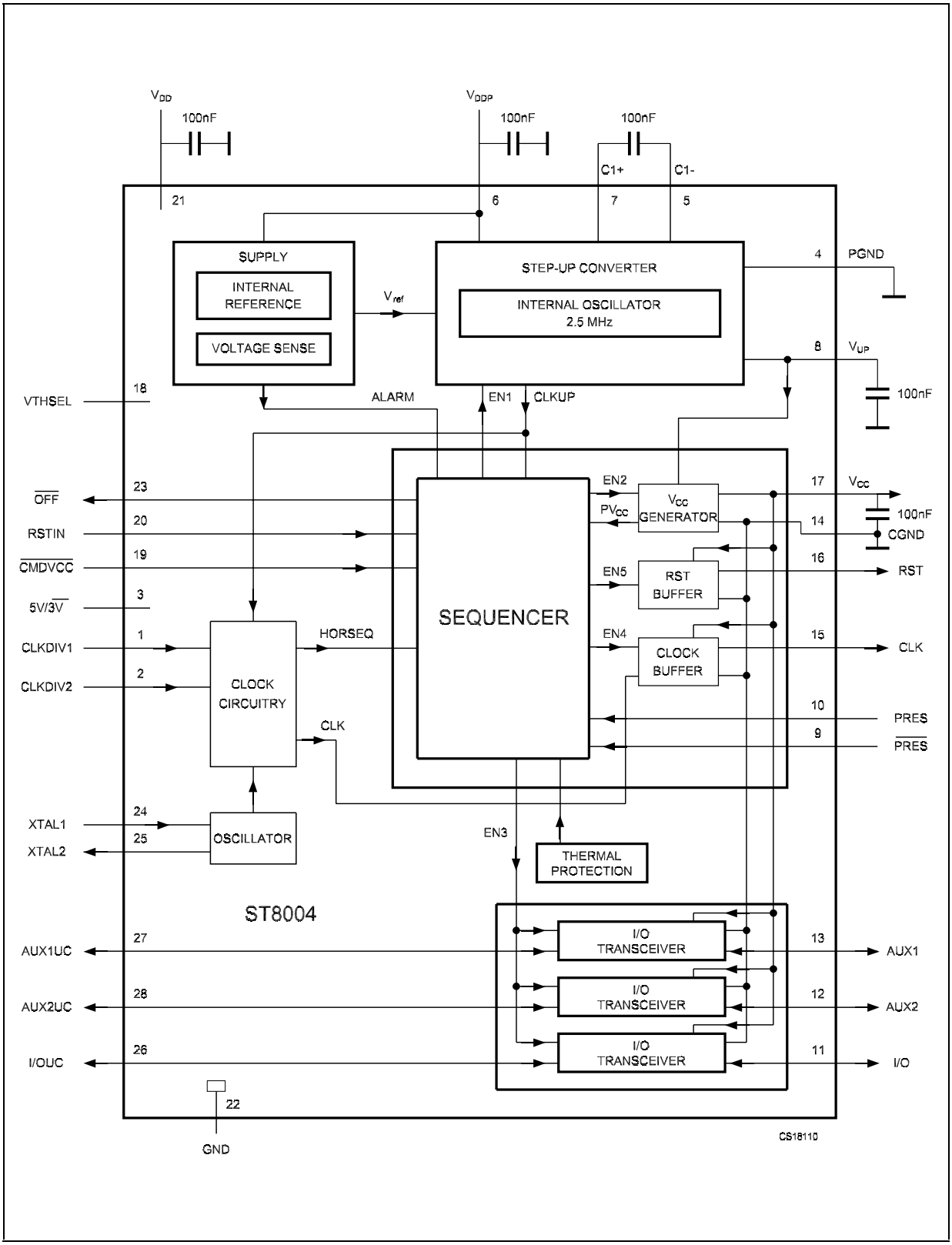
DESCRIPTION

The ST8004 is a complete low cost analog interface for asynchronous 3V and 5V smart cards. It can be placed between the card and the microcontroller with few external components to perform all supply protection and control functions. Main applications are: smartcard readers for Set Top Box, IC card readers for banking, identification.

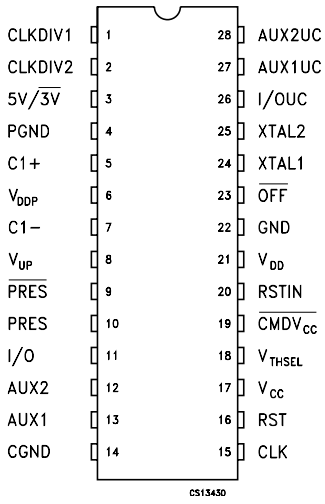
ORDERING CODES

Type	Temperature Range	Package	Comments
ST8004CD	0 to 85 °C	SO-28 (Tube)	27 parts per tube / 12 tube per box
ST8004CDR	0 to 85 °C	SO-28 (Tape & Reel)	1000 parts per reel

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN N°	SYMBOL	NAME AND FUNCTION
1	CLKDIV1	Control of CLK Frequency
2	CLKDIV2	Control of CLK Frequency
3	5V/$\overline{3V}$	V_{CC} selection pin.
4	PGND	Power Ground for Step-Up converter
5	C1+	External Cap. for Step-Up converter
6	V_{DDP}	Power Supply for Step-Up converter
7	C1-	External Cap. Step-Up converter
8	V_{UP}	Output of Step-Up converter
9	$\overline{PRES}$	Card Presence Input (Active Low)
10	PRES	Card Presence Input (Active High)
11	I/O	Data Line to and from card (C7) (internal 10kΩ pull-up resistor connected to V_{CC})
12	AUX2	Auxiliary line to and from card (C8) (internal 10kΩ pull-up resistor connected to V_{CC})
13	AUX1	Auxiliary line to and from card (C4) (internal 10kΩ pull-up resistor connected to V_{CC})
14	CGND	Ground for card signal (C5)
15	CLK	Clock to card (C3)
16	RST	Card Reset (C2)
17	V_{CC}	Supply Voltage for the card (C1)
18	V_{THSEL}	Deactivation threshold selector pin (under voltage lock-out)
19	$\overline{CMDV_{CC}}$	Start activation sequence input (Active Low)
20	RSTIN	Card Reset Input from MCU
21	V_{DD}	Supply Voltage
22	GND	Ground
23	$\overline{OFF}$	Interrupt to MCU (active Low)
24	XTAL1	Crystal or external clock input
25	XTAL2	Crystal connection (leave this pin open if external clock is used)
26	I/OUC	Data Line to and from MCU (internal 10kΩ pull-up resistor connected to V_{DD})
27	AUX1UC	Auxiliary line to and from MCU (internal 10kΩ pull-up resistor connected to V_{DD})
28	AUX2UC	Auxiliary line to and from MCU (internal 10kΩ pull-up resistor connected to V_{DD})

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}, V_{DDP}	Supply Voltage	-0.3	7	V
V_{n1}	Voltage on pins XTAL1, XTAL2, 5V/$\overline{3V}$, RSTIN, AUX2UC, AUX1UC, I/$\overline{OUC}$, CLKDIV1, CLKDIV2, V_{THSEL}, $CMDV_{CC}$, PRES, PRES and $\overline{OFF}$	-0.3	V_{DD} + 0.3	V
V_{n2}	Voltage on card contact pins I/O, RST, AUX1, AUX2 and CLK	-0.3	V_{CC} + 0.3	V
V_{n3}	Voltage on pins V_{UP}, S1 and S2		9	V
ESD1	MIL-STD-883 class 3 on card contact pins, $\overline{PRES}$ and PRES (Note 1, 2)	-6	6	KV
ESD2	MIL-STD-883 class 2 on µC contact pins and RSTIN (Note 1, 2)	-2	2	KV

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Note 1: All card contacts are protected against any short with any other card contact.

Note 2: Method 3015 (HBM, 1500 Ω, 100 pF) 3 positive pulses and 3 negative pulses on each pin referenced to ground.

THERMAL DATA

Symbol	Parameter	Condition	Value	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient Temperature	In free air	70	°K/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_A	Temperature Range		-25		85	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	V_{THSEL} = V_{DD} or floating		2.7		6.5	V
		V_{THSEL} = GND		3.150		6.5	
V_{DDP}	Supply Voltage for the voltage doubler			4.5	5	6.5	V
		To comply with $V_{I(RIPPLE)(P\text{-}P)}$ specifications		4.75		5.25	
$V_{O(VUP)}$	Output Voltage on pin V_{UP} from step-up converter				5.5		V
$V_{I(VUP)}$	Input Voltage to be applied on VUP in order to block the step-up converter			7		9	V
I_{DD}	Supply Current	Inactive mode				1.2	mA
		Active mode; f_{CLK} = f_{XTAL}; C_L = 30pF				1.5	
I_P	Supply Current for Step-Up converter	Inactive mode				0.1	mA
		Active mode; f_{CLK} = f_{XTAL}; C_L = 30pF	I_{CC} = 0			18	
			I_{CC} = 65 mA			150	
V_{th2}	Threshold Voltage on V_{DD}	V_{THSEL} = V_{DD} or floating		2.2		2.4	V
V_{th3}	Threshold Voltage on V_{DD}	V_{THSEL} = GND		2.95		3.05	V
$V_{HYS(th2)}$	Hysteresis on V_{th2}	V_{THSEL} = V_{DD} or floating		50		150	mV
$V_{HYS(th3)}$	Hysteresis on V_{th3}	V_{THSEL} = GND			0		mV
t_W	Pulse width of the internal Alarm pulse			6		20	ms
ΔT_{HFIL}	Delay of Internal filter	V_{THSEL} = GND		5		50	µs

CARD SUPPLY VOLTAGE CHARACTERISTICS (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C) (Note 1)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{CC}	Output Voltage including ripple	Inactive Mode		-0.1		0.1	V
		Inactive Mode; I_{CC} = 1 mA		-0.1		0.4	
		Active Mode; V_{DDP} = 5V ± 5% $\lvert I_{CC}\rvert$ < 65 mA DC	5 V card	4.75		5.25	
			3 V card	2.85		3.15	
		Active Mode; single current pulse of 100 mA; 2 µs	5 V card	4.65		5.25	
			3 V card	2.85		3.15	
		Active Mode; current pulse of 40 nAs with $\lvert I_{CC}\rvert$<200mA t < 400 ns	5 V card	4.65		5.25	
			3 V card	2.76		3.15	
$V_{I(RIPPLE)}$ (P-P)	Peak to Peak ripple voltage on V_{CC}	20 KHz to 200 MHz V_{DDP} = 5V ± 5%				350	mV
$\lvert I_{CC}\rvert$	Output Current	From 0 to 5V or to 3V				65	mA
		V_{CC} short circuit to GND				150	
S_R	Slew Rate	Up to down		0.11		0.22	V/µs

CRYSTAL CONNECTION (PINS XTAL1 AND XTAL2) (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{EXT}	External capacitors on pins XTAIL1, XTAIL2	Depending on specification of crystal or resonator used			15	pF
$f_{I(XTAL)}$	Crystal Input Frequency		2		26	MHz
$V_{IH(XTAL)}$	High level input voltage on XTAIL1		0.7 V_{DD}		V_{DD}	V
$V_{IL(XTAL)}$	Low level input voltage on XTAIL1		0		0.3 V_{DD}	V

DATA LINES (PINS I/O, AUX1, AUX2, AUX1UC AND AUX2UC) (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{D(EDGE)}$	Delay between falling edge on pin I/O and I/OUC and width of active pull-up pulse			200		ns
$f_{I/O(MAX)}$	Maximum frequency of data lines				1	MHz
C_I	Input capacitance on data lines				10	pF

DATA LINES (PINS I/O, AUX1 AND AUX2 WITH 10 kΩ PULL-UP RESISTOR CONNECTED TO V_{CC} INTERNALLY (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	High Level Output Voltage on data lines	I_{OH} = - 40µA	0.75 V_{CC}		V_{CC}	V
		No Load	0.9 V_{CC}		V_{CC}+0.3	
V_{OL}	Low Level Output Voltage on data lines	I_{OL} = 1 mA			300	mV
V_{IH}	High Level Input Voltage on data lines		1.8		V_{CC}	V
V_{IL}	Low Level Input Voltage on data lines		-0.3		0.8	V
$V_{INACTIVE}$	Voltage on data lines when inactive	No Load			0.1	V
		$I_{I/O}$ = 1 mA			0.3	
I_{EDGE}	Current from data lines when active pull-up is active	V_{OH} = 0.7 x V_{CC}; C_O = 80 pF	-1			mA
$\|I_{IH}\|$	Input Leakage Current when high	V_{IH} = V_{CC}			10	µA
I_{IL}	Low Level Input Current	V_{IL} = 0			600	µA
$R_{PU(INT)}$	Internal pull-up resistance to V_{CC}		9		13	KΩ
$t_{T(DI)}$	Input transition times	From V_{IL} max to V_{IH} min			1	µs
$t_{T(DO)}$	Output transition times	C_O = 80 pF, no DC load; 0.4 V to 70% from 0 to V_{CC}			0.1	µs
C_I	Input capacitance				10	pF

DATA LINES (PINS I/OUC, AUX1UC AND AUX2UC WITH 10 kΩ PULL-UP RESISTOR CONNECTED TO V_{DD} INTERNALLY (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	High Level Output Voltage	I_{OH} = - 40µA	0.75 V_{DD}		V_{DD}	V
		No Load	0.9 V_{DD}			
V_{OL}	Low Level Output Voltage	I_{OL} = 1 mA	0		300	mV
V_{IH}	High Level Input Voltage		0.7 V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage		0		0.3 V_{DD}	V
$\|I_{LIH}\|$	Input Leakage Current when high	V_{IH} = V_{DD}			10	µA
I_{IL}	Input Leakage Current when low	V_{IL} = 0			600	µA
$R_{PU(INT)}$	Internal pull-up resistance to V_{DD}		9	11	13	KΩ
$t_{T(DI)}$	Input transition times	From V_{IL} max to V_{IH} min			1	µs
$t_{T(DO)}$	Output transition times	C_O = 30 pF, no DC load; 10% to 90% from 0 to V_{DD}			0.1	µs
C_I	Input capacitance				10	pF

INTERNAL OSCILLATOR (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$f_{OSC(INT)}$	Frequency of internal oscillator		2.2		3.2	MHz

RESET OUTPUT TO THE CARD (PIN RST) (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{O(INACTIVE)}$	Output Voltage in Inactive Mode	I_O = 1 mA	0		0.3	V
		No Load	0		0.1	
$t_{D(RSTIN-RST)}$	Delay between pins RSTN and RST	RST Enable			2	µs
V_{OL}	Low Level Output Voltage	I_{OL} = 200 µA	0		0.2	V
V_{OH}	High Level Output Voltage	I_{OH} = -200 µA	0.9 V_{CC}		V_{CC}	V
t_R, t_F	Rise and fall time (10% to 90% of V_{CC})	C_O = 250 pF			0.1	µs

CLOCK OUTPUT TO THE CARD (PIN CLK) (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{O(INACTIVE)}$	Output Voltage in Inactive Mode	I_O = 1 mA	0		0.3	V
		No Load	0		0.1	
V_{OL}	Low Level Output Voltage	I_{OL} = 200 µA	0		0.3	V
V_{OH}	High Level Output Voltage	I_{OH} = -200 µA	0.9 V_{CC}		V_{CC}	V
t_R, t_F	Rise and fall time (10% to 90% of V_{CC})	C_O = 35 pF (Note 2)			8	ns
δ	Duty cycle factor (except for f_{XTALS}) (See Note 4)	C_O = 35 pF (Note 2)	45		55	%
S_R	Slew Rate (rise and fall edge)	C_O = 35 pF	0.2			V/ns

LOGIC INPUTS (PINS CLKDIV1, CLKDIV2, PRES, $\overline{\text{PRES}}$, $CMDV_{CC}$, RSTIN AND 5V/3V, VTHSEL (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C) (Note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage		0		0.3 V_{DD}	V
V_{IH}	High Level Input Voltage		0.7 V_{DD}		V_{DD}	V
$\|I_{LIH}\|$	Input Leakage Current when high	V_{IL} = 0 to V_{DD}			5	µA
$\|I_{LIL}\|$	Input Leakage Current when low	V_{IH} = 0 to V_{DD}			5	µA

$\overline{\text{OFF}}$ OUTPUTS (PIN $\overline{\text{OFF}}$ IS AN OPEN DRAIN WITH AN INTERNAL 20 kΩ PULL-UP RESISTOR TO V_{DD}); (see note 5) (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.4	V
V_{OH}	High Level Output Voltage	I_{OH} = -15 µA	0.75 V_{DD}			V

PROTECTION (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{SD}	Shut down temperature			135		°C
$I_{CC(SD)}$	Shut down current at V_{CC}				150	mA

TIMING (V_{DD} = 3.3V, V_{DDP} = 5V, f_{XTAL} = 10MHz, unless otherwise noted. Typical values are to T_a = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{ACT}	Activation sequence duration	(See Fig. 3)		180	220	µs
t_{DE}	Deactivation sequence duration	(See Fig. 4)	60	80	100	µs
t_3	Start of the windows to send CLK to card	(See Fig. 3)			130	µs
t_5	End of the windows to send CLK to card	(See Fig. 3)	140			µs

Note 1: To meet these specifications V_{CC} should be decoupled to CGND using two ceramic multiplier capacitors of low ESR with values of 100nF.

Note 2: The transition time and duty cycle factor are shown in figure 7; d = t1/(t1+t2).

Note 3: $\overline{\text{PRES}}$ and CMDVCC are active Low; RSTIN and PRES are active High

Note 4: Referred to the paragraph "CLOCK CIRCUITRY"

Note 5: See paragraph "FAULT DETECTION".

Figure 1 : Alarm as a function of V_{DD} (t_W = 10 ms), V_{THSEL} = V_{DD} or floating

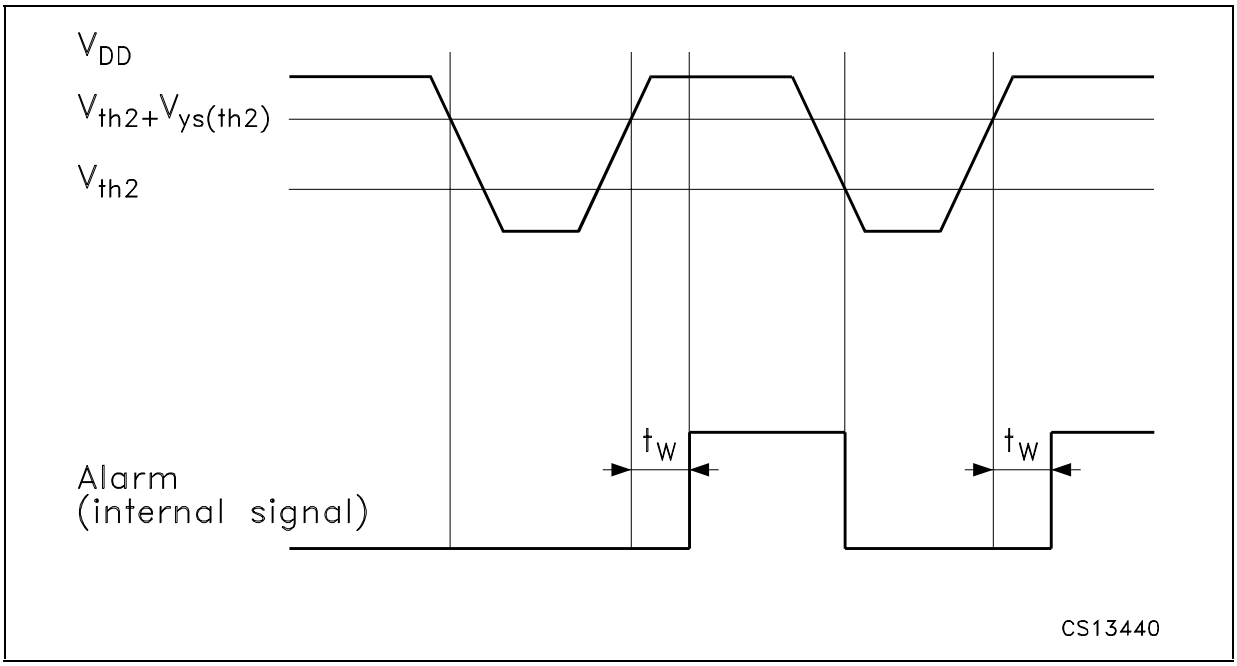


Figure 2 : Alarm as a function of V_{DD} (t_W = 10 ms), V_{THSEL} = GND

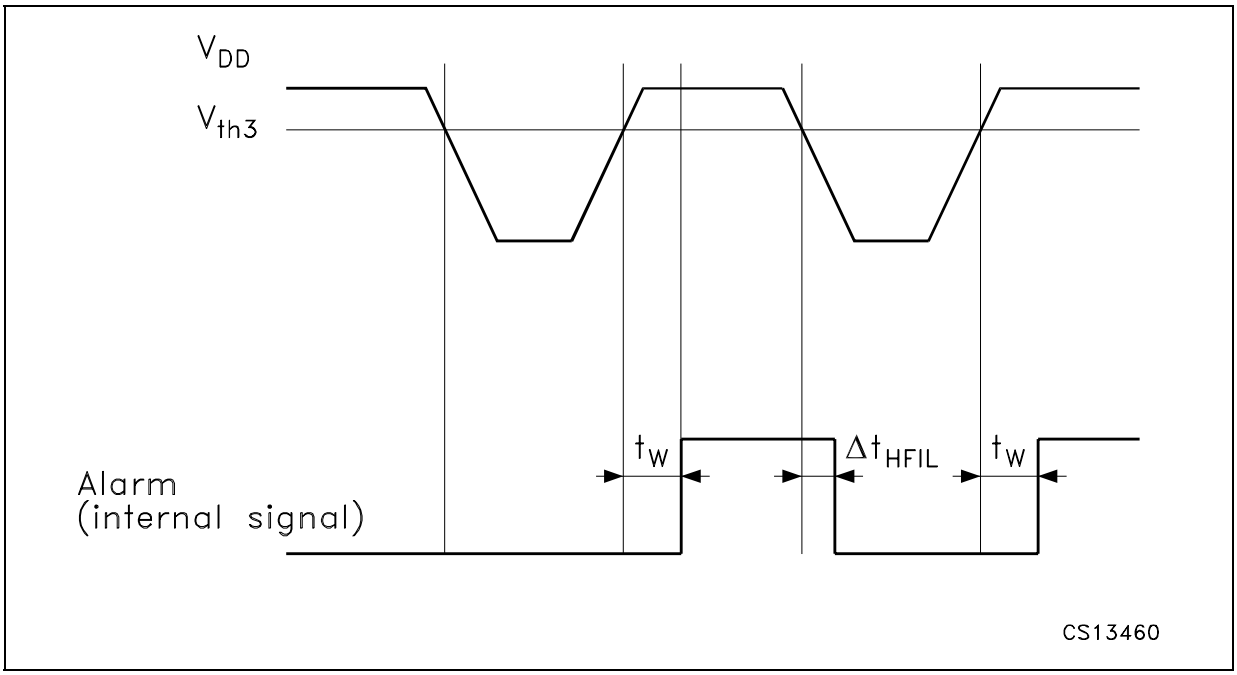


Figure 3 : Activation sequence

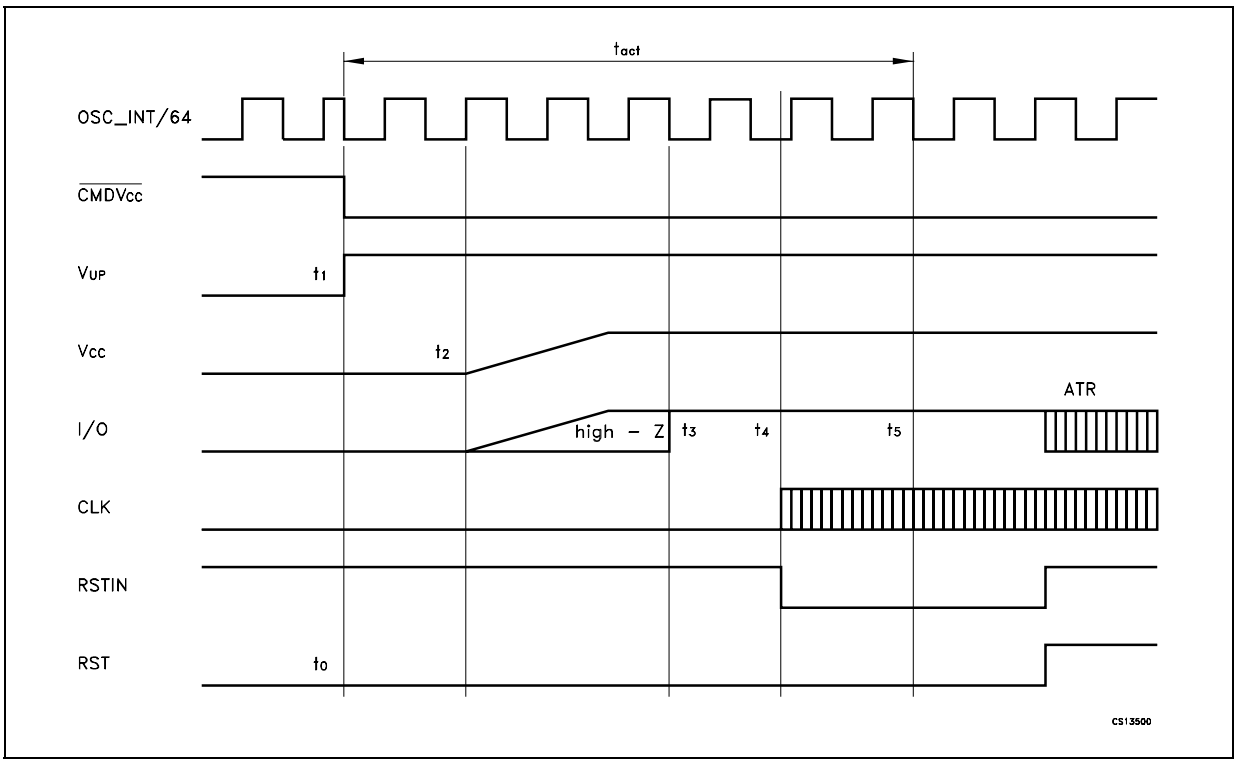


Figure 4 : Deactivation sequence

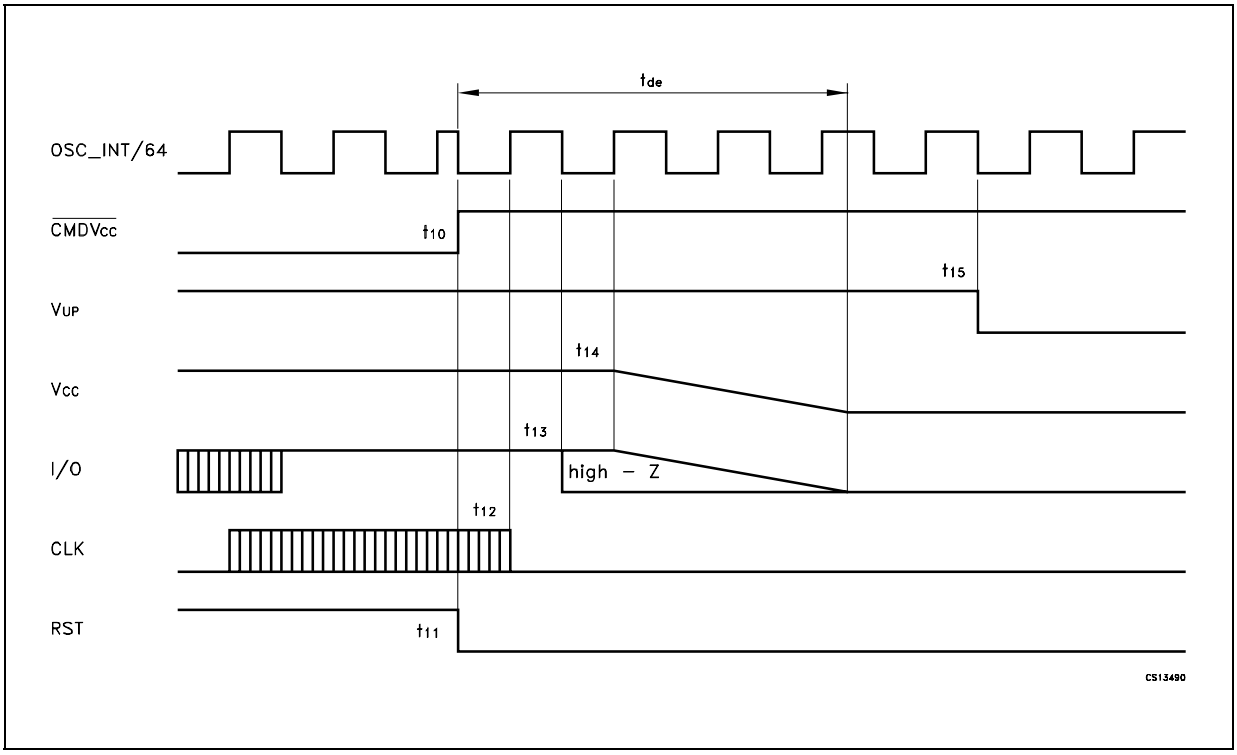


Figure 5 : Behavior of $\overline{OFF}$, $\overline{CMDV}_{CC}$, PRES and V_{CC}

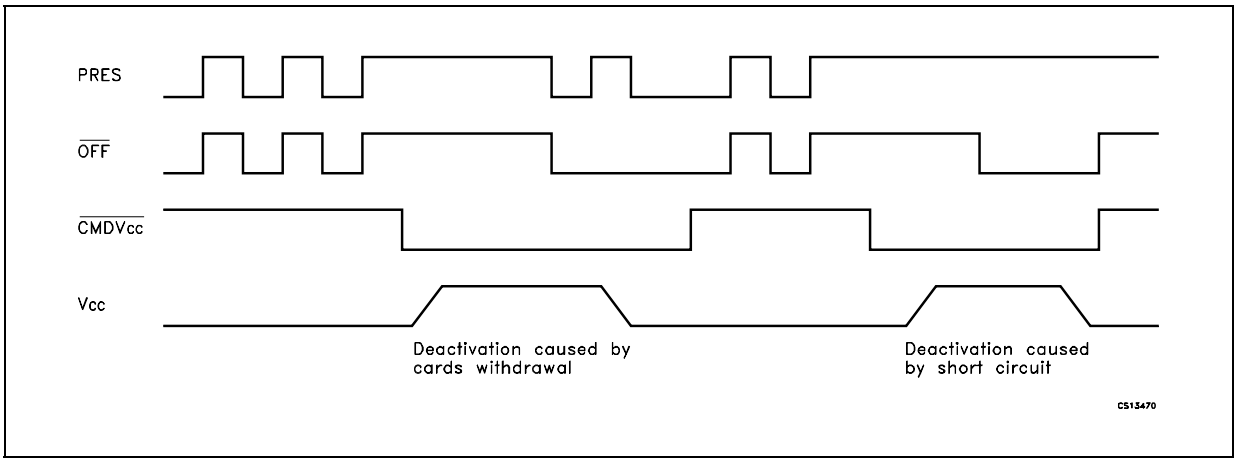


Figure 6 : Emergency deactivation sequence

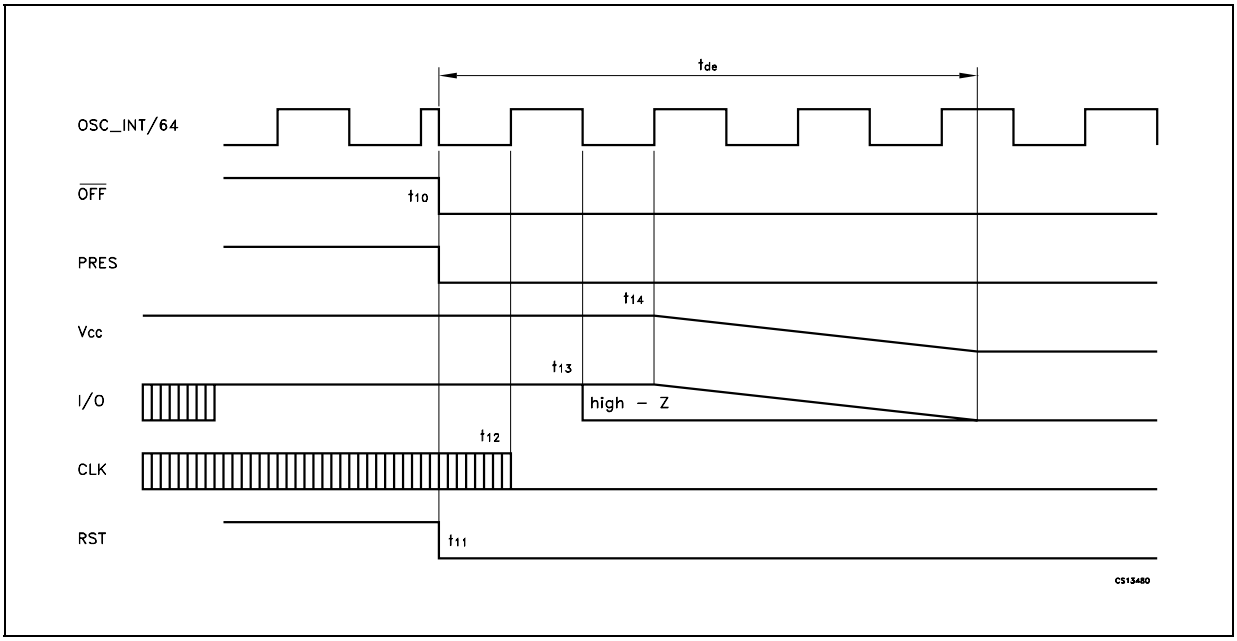
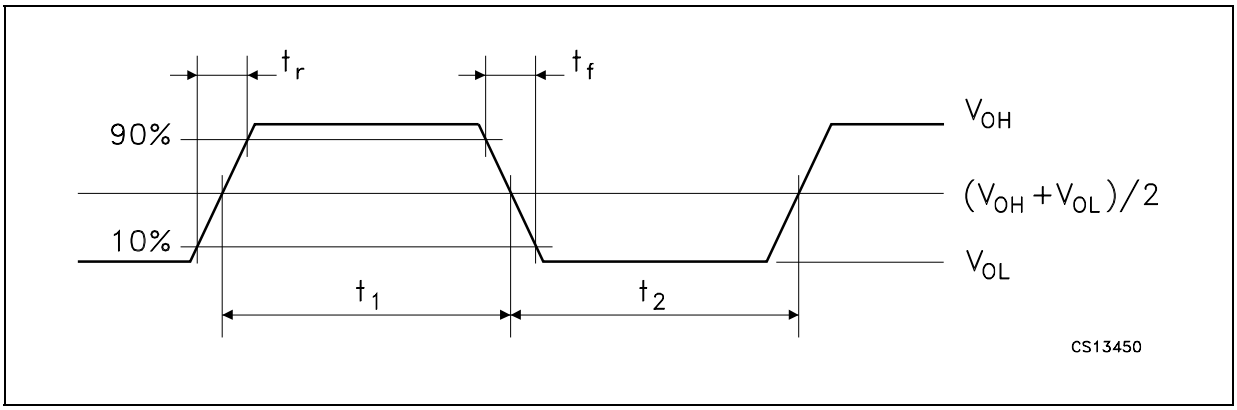


Figure 7 : Definition of output transition times



FUNCTIONAL DESCRIPTION

Throughout this document it is assumed that the reader is familiar with iso7816 norm terminology

POWER SUPPLY

The supply pins for the IC are V_{DD} and GND. V_{DD} should be in the range of 2.7 to 6.5 V. All interface signals with the microcontroller are referenced to V_{DD}; therefore be sure the supply voltage of the microcontroller is also at V_{DD}. All card contacts remain inactive during powering up or powering down. The sequencer is not activated until V_{DD} reaches V_{th2} +$V_{hys(th2)}$ or V_{th3} + $V_{hys(th3)}$ when V_{THSEL} = GND. When V_{DD} falls below V_{th2} or V_{th3}, an automatic deactivation of the contacts is performed. To generate a 5 V ±5% V_{CC} supply to the card, an integrated voltage doubler is incorporated. This step-up converter should be separately supplied by V_{DDP} and PGND (from 4.5 to 6.5 V). In order to satisfy the $V_{I(RIPPLE)(P-P)}$ specifications, V_{DDP} should be from 4.75V to 5.25V. Due to large transient currents, the 2x100 nF capacitors of the step-up converter should have an ESR of less than 100 mΩ, and be located as near as possible to the IC. The supply voltages V_{DD} and V_{DDP} may be applied to the IC in any time sequence. To get the correct deactivation of the card V_{DDP} is allowed to turn-off only when V_{DD} is below the undervoltage threshold. If a voltage between 7 and 9 V is available within the application, this voltage may

be tied to pin V_{UP}, thus blocking the step-up converter. In this case, V_{DDP} must be tied to V_{DD} and the capacitor between pins S1 and S2 may be omitted.

VOLTAGE SUPERVISOR (FOR V_{THSEL} = V_{DD} OR FLOATING)

This block surveys the V_{DD} supply. A defined reset pulse of approximately 10 ms (t_W) is used internally for maintaining the IC in the inactive mode during powering up or powering down of V_{DD} (see Fig.1). As long as V_{DD} is less than V_{th2} +$V_{hys(th2)}$, the IC will remain inactive whatever the levels on the command lines. This also lasts for the duration of t_W after V_{DD} has reached a level higher than V_{th2} +$V_{hys(th2)}$.The system controller should not attempt to start an activation sequence during this time. When V_{DD} falls below V_{th2}, a deactivation sequence of the contacts is performed.

VOLTAGE SUPERVISOR (FOR V_{THSEL} = GND)

This block surveys the V_{DD} supply. A defined reset pulse of approximately 10 ms (t_W) is used internally for maintaining the IC in the inactive mode during powering up or powering down of V_{DD} (see Fig.2). If V_{DD} is less than V_{th3} during a time, longer than ΔT_{HFIL} (max 150µs), the IC will remain inactive whatever the levels on the command lines. The IC remain inactive also for the duration of tw after V_{DD} has reached a level higher than V_{th3}. The system controller should not attempt to start an activation sequence during this time. When V_{DD} falls below V_{th3} during time more than ΔT_{HFIL}, a deactivation sequence of the contacts is performed.

CLOCK CIRCUITRY

The clock signal (CLK) to the card is either derived from a clock signal input on the pin XTAL1 or from a crystal up to 26 MHz connected between pins XTAL1 and XTAL2.

The frequency may be chosen at f_{XTAL},1/2 f_{XTAL},1/4 f_{XTAL} or 1/8 f_{XTAL} via pins CLKDIV1 and CLKDIV2 (see Table 1). The frequency change is synchronous, which means that during transition, no pulse is shorter than 45% of the smallest period and that the first and last clock pulse around the change has the correct width.

In the case of f_{XTAL}, the duty factors depend on the signal at XTAL1.

In order to reach a 45% to 55% duty factor on the pin CLK the input signal on XTAL1 should have a duty factor of 48% to 52% and transition times of less than 5% of the input signal period.If a crystal is used with f_{XTAL}, the duty factor on pin CLK may be 45% to 55% depending on the layout and on the crystal characteristics and frequency. In the other cases, it is guaranteed between 45% and 55% of the period. The crystal oscillator runs as soon as the IC is powered-up. If the crystal oscillator is used, or if the clock pulse on XTAL1 is permanent, then the clock pulse will be applied to the card according to the timing diagram of the activation sequence. If the signal applied to XTAL1 is controlled by the micro-controller, then the clock pulse will be applied to the card by the microcontroller after completion of the activation sequence.

TABLE 1

CLKDIV1	CLKDIV2	CLK
0	0	1/8 f_{XTAL}
0	1	1/4 f_{XTAL}
1	1	1/2 f_{XTAL}
1	0	f_{XTAL}

I/O CIRCUITRY

The three data lines I/O, AUX1 and AUX2 are identical. The Idle state is realized by data lines I/O and I/OUC being pulled HIGH via a 10k resistor (I/O to V_{CC} and I/OUC to V_{DD}). I/O is referenced to V_{CC}, and I/OUC to V_{DD}, thus allowing operation with $V_{CC} \neq V_{DD}$. The first line on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other line, which then becomes the slave. After a time delay td (edge) (approximately 200 ns), the N transistor on the slave line is turned on, thus transmitting the logic 0 present on the master line.When the master line returns to logic 1, the P transistor on the slave line is turned on during the time delay td (edge) and then both lines return to their idle state. This active pull-up feature ensures fast LOW-to-HIGH transitions; it is able to deliver more than 1 mA up to an output voltage of 0.9 V_{CC} on a 80pF load. At the end of the active pull-up

pulse, the output voltage only depends on the internal pull-up resistor, and on the load current. The maximum frequency on these lines is 1MHz.

INACTIVE STATE

After power-on reset, the circuit enters the inactive state.
A minimum number of circuits are active while
waiting for the microcontroller to start a session.

- All card contacts are inactive (approximately 200Ω to GND); I/OUC, AUX1UC and AUX2UC are high impedance (10 kΩ pull-up resistor connected to V_{DD})
- Voltage generators are stopped
- XTAL oscillator is running
- Voltage supervisor is active.

ACTIVATION SEQUENCE

After power-on and, after the internal pulse width delay, the microcontroller may check the presence of the card with the signal $\overline{OFF}$ ($\overline{OFF}$ = HIGH while $\overline{CMDV_{CC}}$ is High means that the card is present; $\overline{OFF}$ = LOW while $\overline{CMDV_{CC}}$ is HIGH means that no card is present).
If the card is in the reader (which is the case if $\overline{PRES}$ or PRES is true), the microcontroller may start a card session by pulling $\overline{CMDV_{CC}}$ LOW. The following sequence then occurs (see Fig.3):

- $\overline{CMDV_{CC}}$ is pulled LOW (t0)
- The voltage doubler is started (t1~t0)
- V_{CC} rises from 0 to 5 or 3V with a controlled slope (t2 = t1 +½3T)(I/O, AUX1 and AUX2 follow V_{CC} with a slight delay); T is 64 times the period of the internal oscillator, approximately 25µs
- I/O, AUX1 and AUX2 are enabled (t3 = t1 +4T)
- CLK is applied to the C3 contact (t4)
- RST is enabled (t5 = t1 +7T).

The clock may be applied to the card in the following way: set RSTIN High before setting $\overline{CMDV_{CC}}$ Low, and reset it Low between t3 and t5; CLK will start at this moment. RST will remain LOW until t5, where RST is enabled to be the copy of RSTIN. After t5, RSTIN has no further action on CLK. This is to allow a precise count of CLK pulses before toggling RST. If this feature is not needed, then $\overline{CMDV_{CC}}$ may be set LOW with RSTIN Low. In this case, CLK will start at t3, and after t5, RSTIN may be set High in order to get the Answer To Request (ATR) from the card.

ACTIVE STATE

When the activation sequence is completed, the ST8004 will be in the active state. Data are exchanged between the card and the microcontroller via the I/O lines. The ST8004 is designed for cards without V_{PP} (this is the voltage required to program or erase the internal non-volatile memory).
Depending on the layout and on the application test conditions (for example with an additional 1pF cross capacitance between C2/C3 and C2/C7) it is possible that C2 is polluted with high frequency noise from C3. In this case, it will be necessary to connect a 220pF capacitor between C2 and CGND.
It is recommended to:

1. Keep track C3 as far as possible from other tracks
2. Have straight connection between CGND and C5 (the 2 capacitors on C1 should be connected to this ground track)
3. Avoid ground loops between CGND,PGND and GND
4. Decoupled V_{DDP} and V_{DD} separately; if the 2 supplies are the same in the application, then they should be connected in star on the main track.

With all these layout precautions, noise should be at an acceptable level, and jitter on C3 should be less than 100ps.

DEACTIVATION SEQUENCE

When a session is completed, the microcontroller sets the $\overline{CMDV_{CC}}$ line to the HIGH state. The circuit then executes an automatic deactivation sequence by counting the sequencer back and ends in the inactive state (see Fig.4):

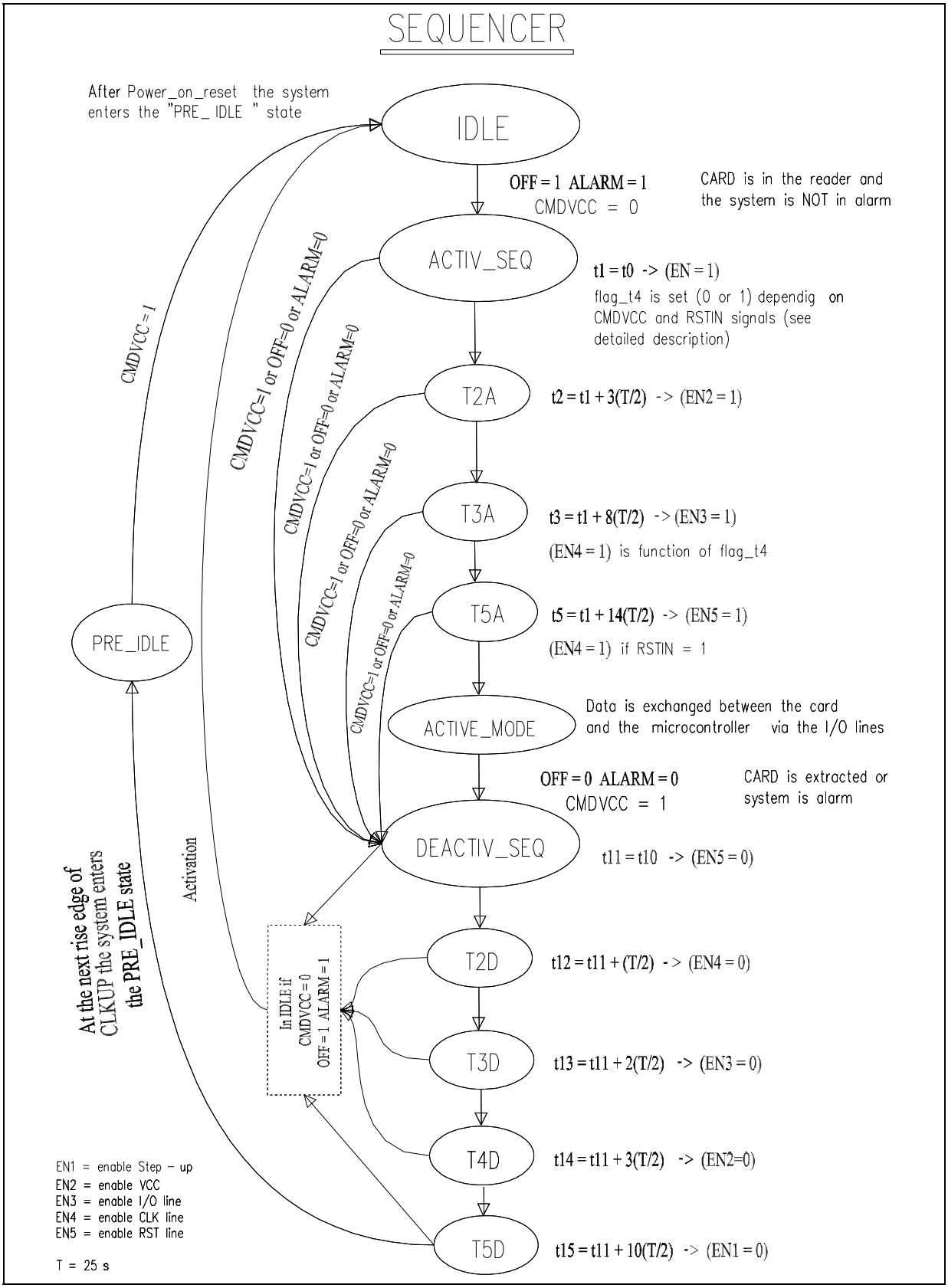
- RST goes LOW → (t11 = t10)
- CLK is stopped LOW → (t12 = t11 +½T) where T is approximately 25 µs
- I/O, AUX1 and AUX2 are output into high-impedance state → (t13 = t11 +T)(10 kΩ pull-up resistor connected to V_{CC})

• V_{CC} falls to zero → (t14 = t11 +½3T); the deactivation sequence is completed when V_{CC} reaches its inactive state
• V_{UP} falls to zero → (t15 = t11 +5T) and all card contacts become low-impedance to GND;
• I/OUC, AUX1UC and AUX2UC remain pulled up to V_{DD} via a 10 kΩ resistor.

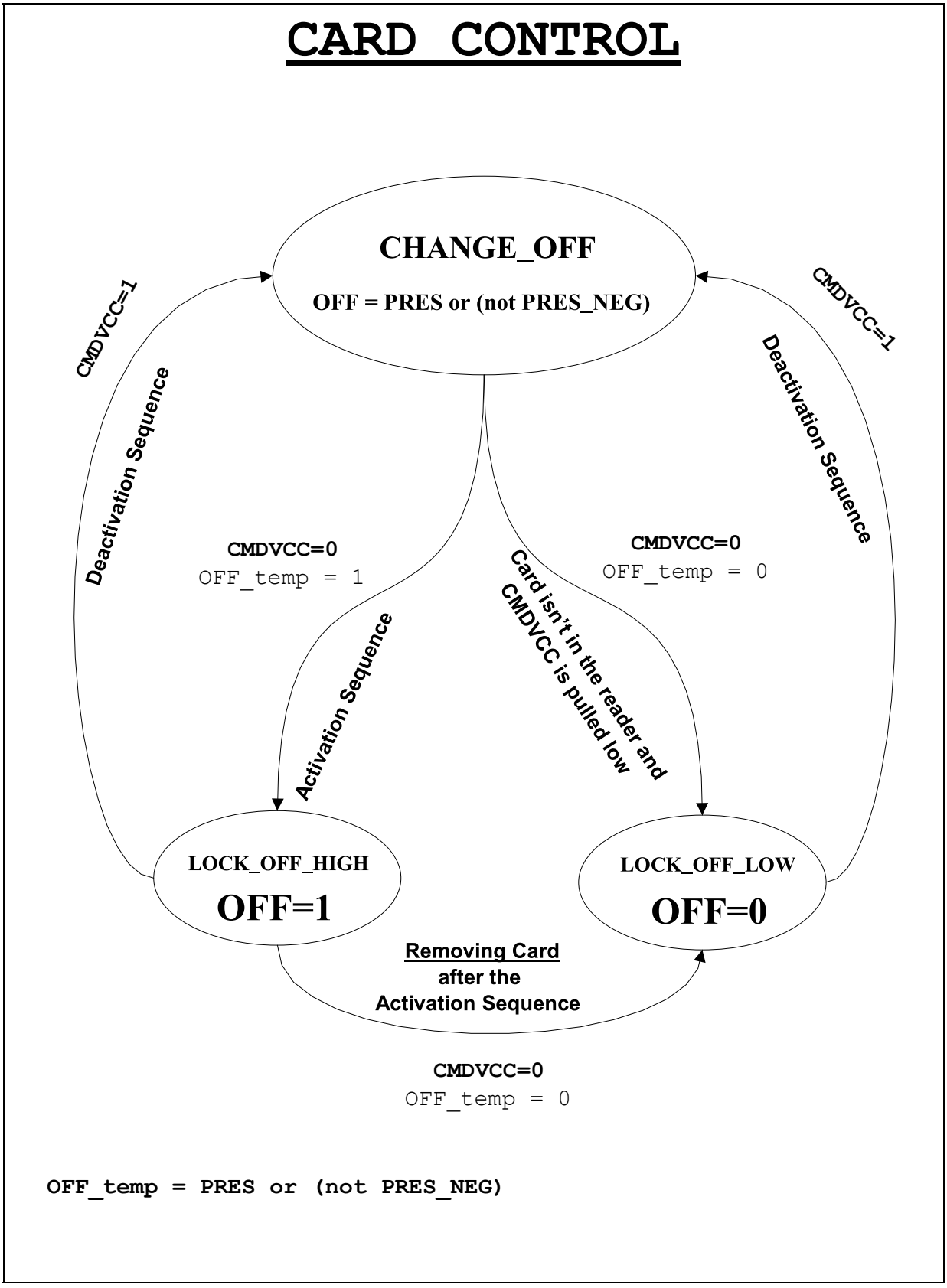
FAULT DETECTION

The following fault conditions are monitored by the circuit:
Short-circuit or high current on V_{CC}
Removing card during transaction
V_{DD} dropping
Overheating.
There are two different cases (Fig. 5)
1. $\overline{CMDV_{CC}}$ HIGH: (outside a card session) then, $\overline{OFF}$ is LOW if the card is not in the reader, and HIGH if the card is in the reader. A supply voltage drop on V_{DD} is detected by the supply supervisor, which generates an internal power-on reset pulse, but does not act upon $\overline{OFF}$. The card is not powered-up, so no short-circuit or overheating is detected.
2. $\overline{CMDV_{CC}}$ LOW: (within a card session) then, $\overline{OFF}$ falls LOW if the card is extracted, or if a short-circuit has occurred on V_{CC}, or if the temperature on the IC has become too high. As soon as the fault is detected, an emergency deactivation is automatically performed (see Fig.6). When the system controller sets $\overline{CMDV_{CC}}$ back to HIGH, it may sense $\overline{OFF}$ again in order to distinguish between a hardware problem or a card extraction. If a supply voltage drop on V_{DD} is detected while the card is activated, then an emergency deactivation will be performed and $\overline{OFF}$ goes LOW.
When $\overline{OFF}$ level falls low, the system controller must wait not less than 160µs before setting high again the $\overline{CMDV_{CC}}$ command.
Depending on the type of card presence switch within the connector (normally closed or normal open), and on the mechanical characteristics of the switch, a bouncing may occur on presence signals at card insertion or withdrawal. There is no debounce feature in the device, so the software has to take it into account; however, the detection of card take off during active phase, which initiates an automatic deactivation sequence is done on the first True/False transition on $\overline{PRES}$ or PRES, and is memorized until the system controller sets $\overline{CMDV_{CC}}$ High. So, the software may take some time waiting for presence switches to be stabilized without causing any delay on the necessary fast and normalized deactivation sequence.

ST8004 SEQUENCER

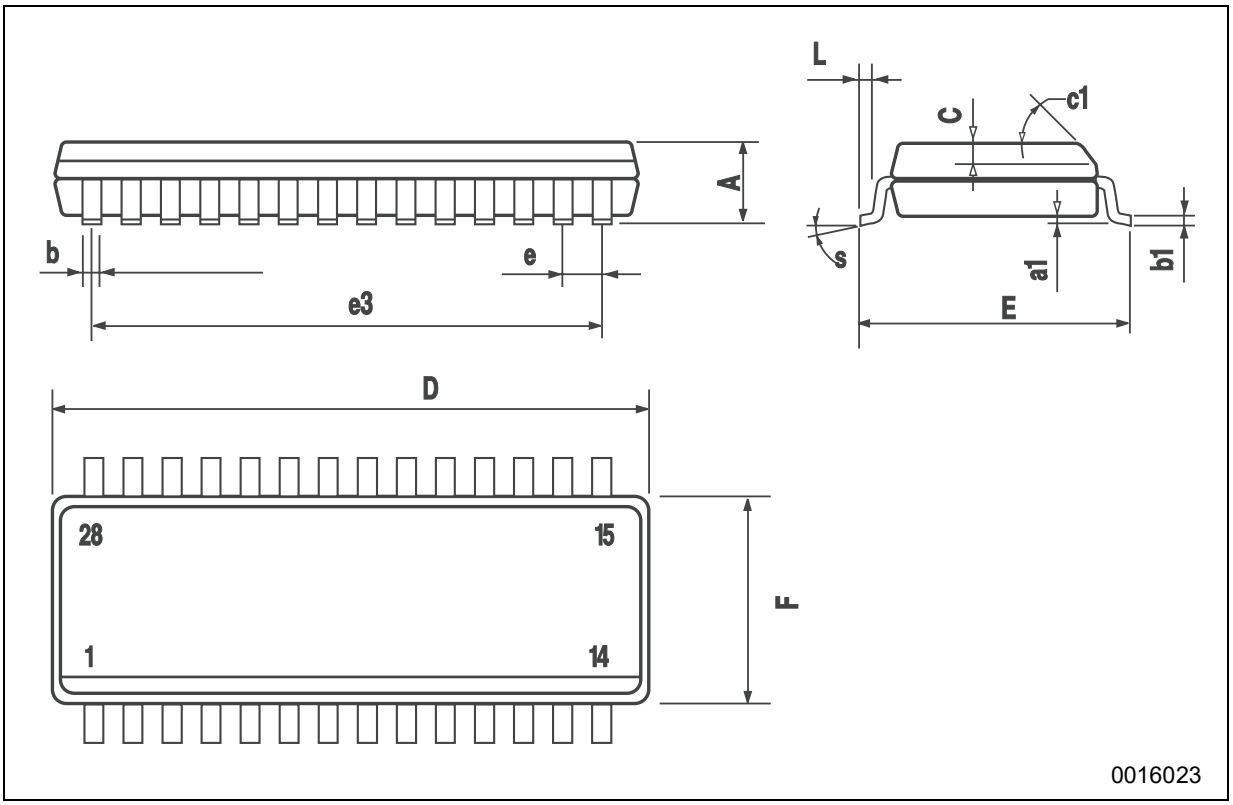


CARD CONTROL SEQUENCER



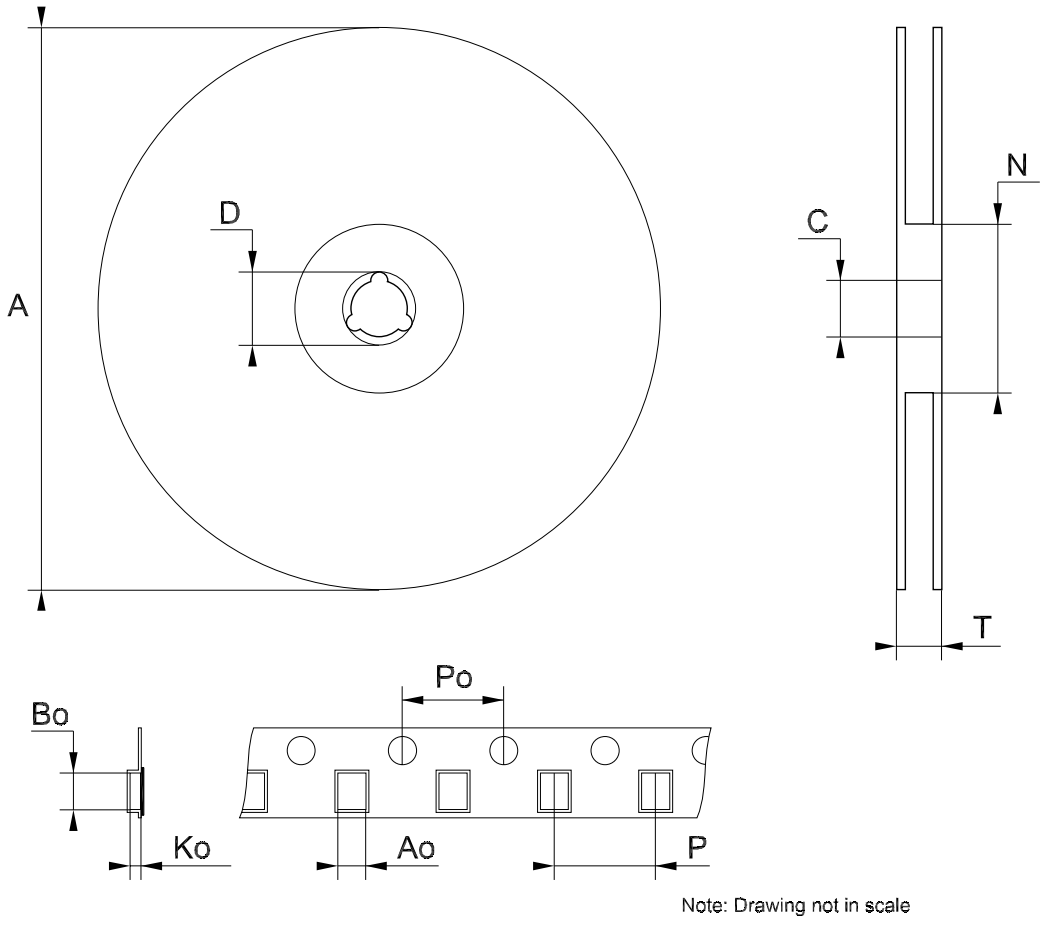
SO-28 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45˚ (typ.)					
D	17.70		18.10	0.697		0.713
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8˚ (max.)					



Tape & Reel SO-28 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11.0	0.425		0.433
Bo	18.2		18.4	0.716		0.724
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

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