

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

# TA8227P

## LOW FREQUENCY POWER AMPLIFIER

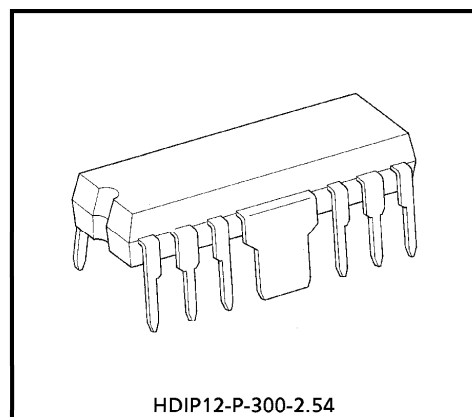
TA8227P is an audio power IC with built-in two channels developed for portable radio cassette tape recorder with power ON/OFF switch.

Because of the parts reduction and DIP (Dual Inline Package), space merit is remarkable.

Thermal shut down protection circuit is built in.

### FEATURES

- High Power
  - :  $P_{out} = 2.5 \text{ W/CH (Typ.)}$   
( $V_{CC} = 9 \text{ V}$ ,  $R_L = 4 \Omega$ ,  $f = 1 \text{ kHz}$ ,  $\text{THD} = 10\%$ )
  - :  $P_{out} = 3.0 \text{ W/CH (Typ.)}$   
( $V_{CC} = 9 \text{ V}$ ,  $R_L = 3 \Omega$ ,  $f = 1 \text{ kHz}$ ,  $\text{THD} = 10\%$ )
- Voltage Gain
  - :  $G_V = 45.0 \text{ dB (Typ.)}$   
( $R_f = 120 \Omega$ ,  $f = 1 \text{ kHz}$ )
  - :  $G_V = 56.5 \text{ dB (Typ.)}$   
( $R_f = 0 \Omega$ ,  $f = 1 \text{ kHz}$ )
- Small Quiescent Current
  - :  $I_{CCQ} = 21 \text{ mA (Typ.)}$   
( $V_{CC} = 9 \text{ V}$ ,  $V_{IN} = 0$ )
- Ripple Rejection Ratio
  - :  $\text{R.R.} = -52 \text{ dB (Typ.)}$   
( $V_{CC} = 9 \text{ V}$ ,  $\text{fripple} = 100 \text{ Hz}$ ,  $R_g = 600 \Omega$ )
- Cross Talk
  - :  $\text{C.T.} = -50 \text{ dB (Typ.)}$   
( $V_{CC} = 9 \text{ V}$ ,  $f = 1 \text{ kHz}$ ,  $R_g = 600 \Omega$ )
- Output Noise Voltage
  - :  $V_{no} = 0.3 \text{ mV}_{rms} \text{ (Typ.)}$   
( $V_{CC} = 9 \text{ V}$ ,  $R_g = 10 \text{ k}\Omega$ ,  $\text{BW} = 20 \text{ Hz} \sim 20 \text{ kHz}$ )
- Stand-By Switch
- Soft Clip
- Built-in Thermal Shut Down Protection Circuit
- Operation Supply Voltage Range :  $V_{CC}(\text{opr}) = 5 \sim 12 \text{ V}$  ( $T_a = 25^\circ\text{C}$ )
- Low Popping Noise at Power ON
- Best for Supply Voltage 9 V



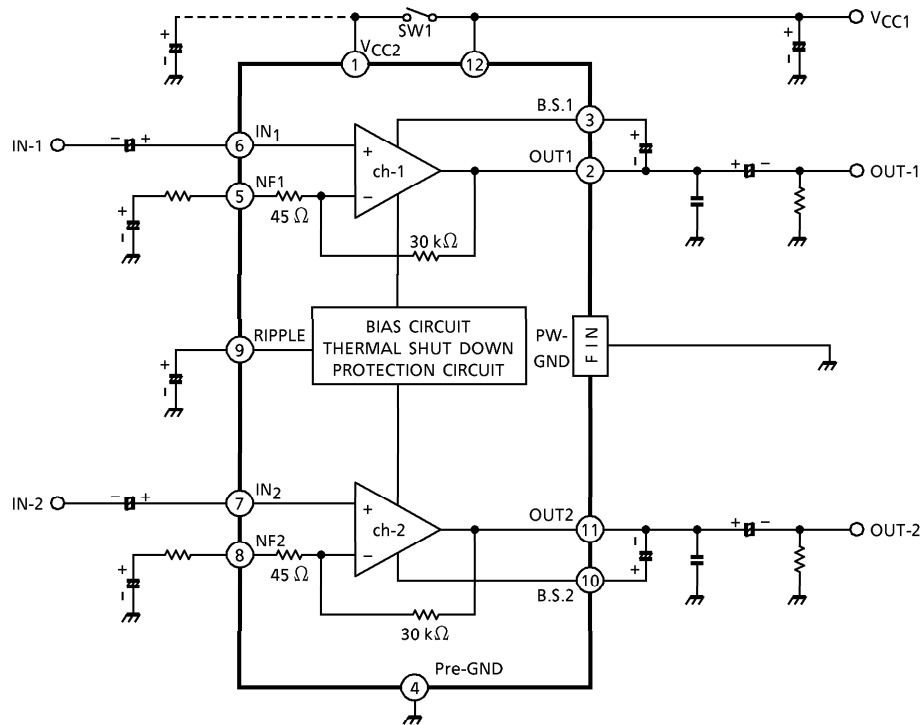
HDIP12-P-300-2.54

Weight : 1.4 g (Typ.)

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BLOCK DIAGRAM



APPLICATION INFORMATION AND APPLICATION METHOD

1. Adjustment of voltage gain

The voltage gain  $G_V$  is obtained as follows by  $R_1$ ,  $R_2$  and  $R_f$  in Fig.1

$$G_V = 20 \log \frac{R_f + R_1 + R_2}{R_f + R_1}$$

When  $R_f = 0 \Omega$   $G_V = 56.5 \text{ dB (Typ.)}$

When  $R_f = 120 \Omega$   $G_V = 45 \text{ dB (Typ.)}$

By increasing  $R_f$ , reduction of  $G_V$  is possible. However, since the feedback increase is liable to produce oscillation, it is recommended to use this at 40 dB or over.

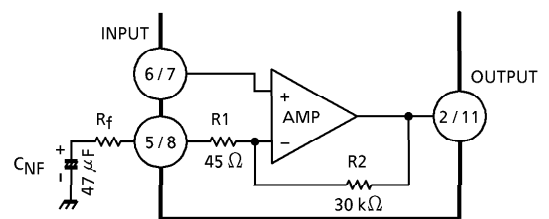


Fig.1

2. Thermal shut-down circuit

The thermal shut-down circuit is built in for the purpose of preventing the destruction of IC due to the abnormal temperature rise when the heat radiation is insufficient.

The operation temperature is set at radiation  $F_{in}$  temperature  $175^\circ\text{C}$  (Typ.).

At this temperature or over the bias is interrupted to prevent the destruction of IC.

### 3. Input stage

The input circuit of this IC is as shown in Fig.2. PNP  $T_r$  : Q1 is provided in the input circuit so as to make its usage possible without the input coupling capacitor.

However, at pin⑥ and ⑦, max 60mV offset voltage is produced.

Application after checking volume slide noise is recommended.

For cutting the volume slide noise, insert the input capacitor :  $C_{IN}$  in series to interrupt the DC component.

### 4. Oscillation preventive measures

For oscillation preventive capacitor  $C_6$  and  $C_7$  between the output terminal and GND, it is recommended to use polyester film capacitor having good characteristics for temperature and for high frequency.

Since the characteristics of the capacitor is liable to be influenced by the temperature, use this capacitor after the temperature test to check the oscillation allowance.

In addition, as the position of the electrolytic capacitor has a remarkable influence on the oscillation, connect  $C_{10}$  to  $V_{CC}$  at the nearest possible position from power GND.

At using this application with the voltage gain reduced, oscillation is liable to be produced. Apply the capacitor after checking enough for its capacity, type and mounting position.

(\*) As the oscillation allowance varies according to the printed pattern layout the standard printed board of TOSHIBA is recommended to be referred to design it.

### 5. Power ON/OFF switch

There is power ON/OFF switch at Pin①. However, output power is changed by Pin① supply voltage when Pin① supply voltage is not same Pin⑫ supply voltage, after referring to attached date, select Pin① supply voltage.

### 6. Input voltage

When the excessive signal is input, turning-up is produced in the clip waveform. The turning-up point is  $V_{in} = 300 \text{ mV}_{rms}$  (Typ.) :  $V_{CC} = 9 \text{ V}$ ,  $R_L = 4 \Omega$ ,  $f = 1 \text{ kHz}$  : Enough care must be taken for this phenomenon.

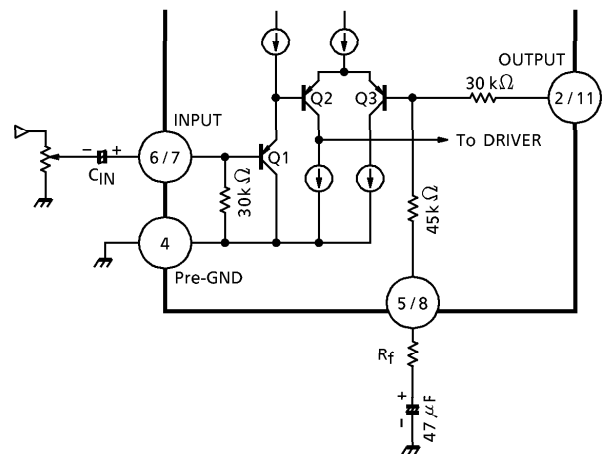


Fig.2

## MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V <sub>CC</sub>	20	V
Output Current (Peak / CH)	I <sub>O</sub> (peak)	2.5	A
Power Dissipation	P <sub>D</sub> (Note)	4.0	W
Operating Temperature	T <sub>opr</sub>	-25~75	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

(Note) Value for mounting on PC board (Refer to P<sub>D</sub>-Ta curve)

## ELECTRICAL CHARACTERISTICS

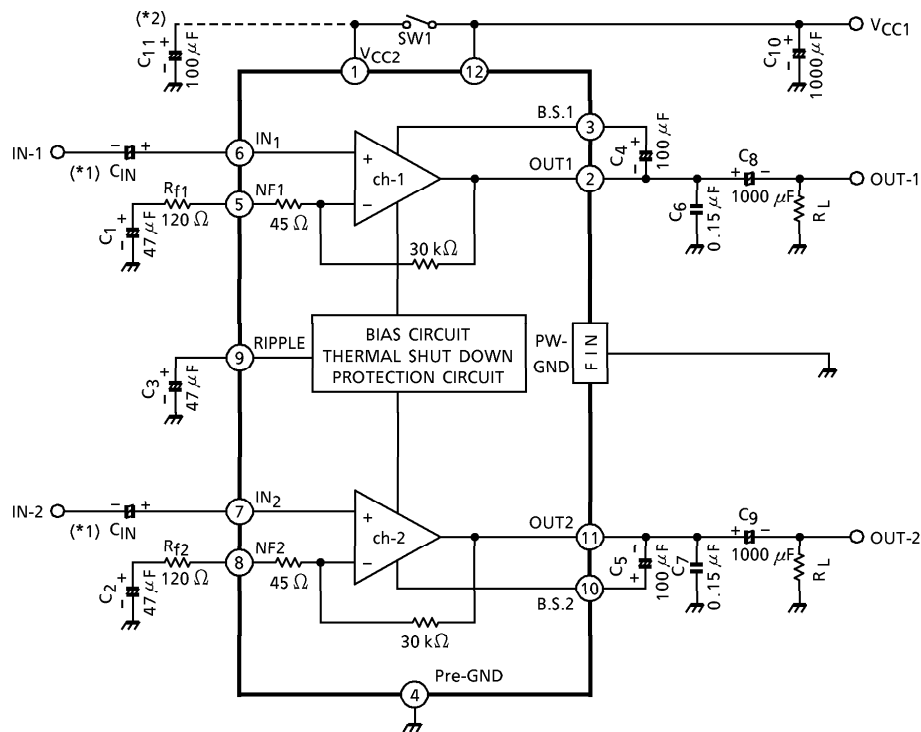
(Unless otherwise specified, V<sub>CC</sub> = 9 V, R<sub>L</sub> = 4 Ω, R<sub>g</sub> = 600 Ω, f = 1 kHz, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	I <sub>CCQ</sub>	—	V <sub>in</sub> = 0	—	21	45	mA
Output Power	P <sub>out</sub> (1)	—	THD = 10%	2.0	2.5	—	W
	P <sub>out</sub> (2)	—	THD = 10%, R <sub>L</sub> = 3 Ω	—	3.0	—	
Total Harmonic Distortion	THD	—	P <sub>out</sub> = 0.4 W / CH	—	0.2	1.0	%
Voltage Gain	G <sub>v</sub> (1)	—	R <sub>f</sub> = 120 Ω V <sub>out</sub> = 0.775 V <sub>rms</sub> (0 dBm)	43	45	47	dB
	G <sub>v</sub> (2)	—	R <sub>f</sub> = 0 Ω V <sub>out</sub> = 0.775 V <sub>rms</sub> (0 dBm)	—	56.5	—	
Input Resistance	R <sub>IN</sub>	—	—	—	30	—	kΩ
Output Noise Voltage	V <sub>no</sub>	—	R <sub>g</sub> = 10 kΩ, BW = 20 Hz~20 kHz	—	0.3	1.0	mV <sub>rms</sub>
Ripple Rejection Ratio	R.R.	—	R <sub>g</sub> = 600 Ω, fripple = 100 Hz	—	-52	—	dB
Cross Talk	C.T.	—	R <sub>g</sub> = 600 Ω V <sub>out</sub> = 0.775 V <sub>rms</sub> (0 dBm)	—	-50	—	dB
Input Offset Voltage	V <sub>6</sub> , V <sub>7</sub>	—	—	—	30	60	mV
Stand-by Current	I <sub>stb</sub>	—	SW1 → OFF	—	1	—	μA

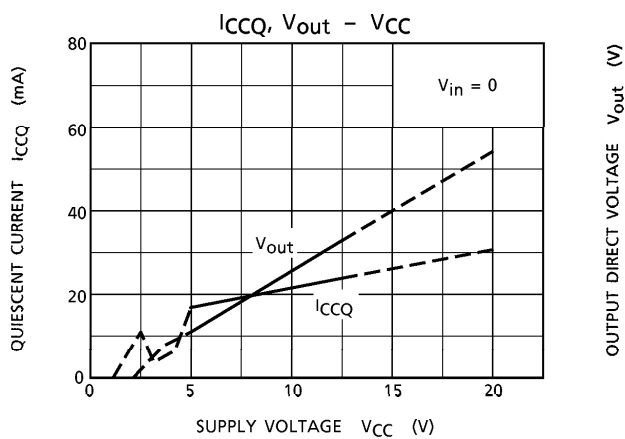
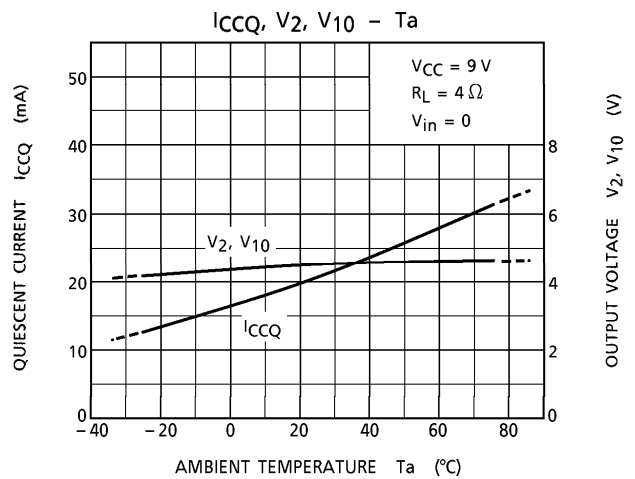
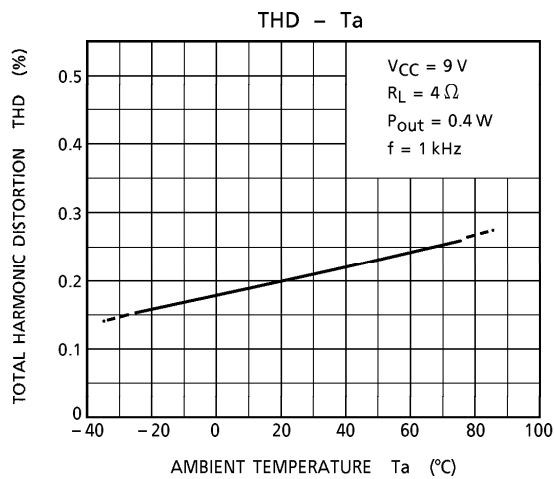
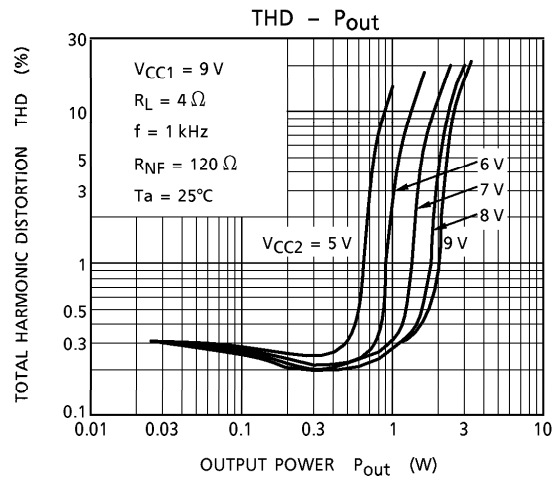
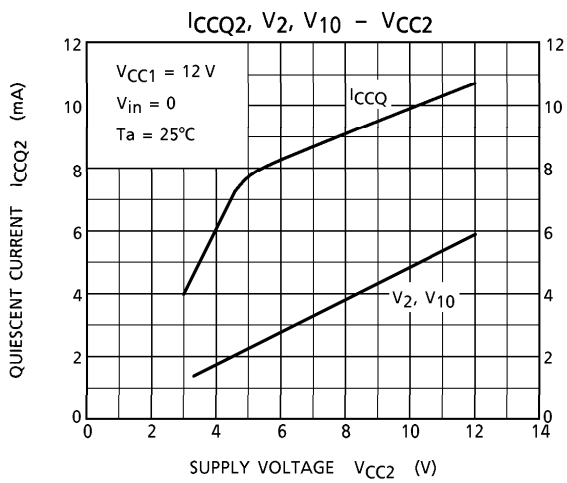
TYP. DC VOLTAGE OF EACH TERMINAL (V<sub>CC</sub> = 9 V, Ta = 25°C)

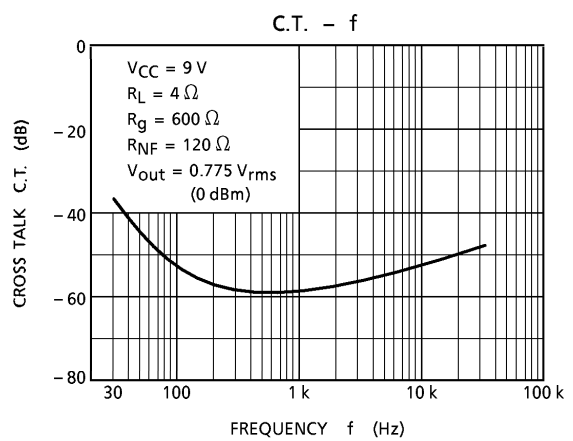
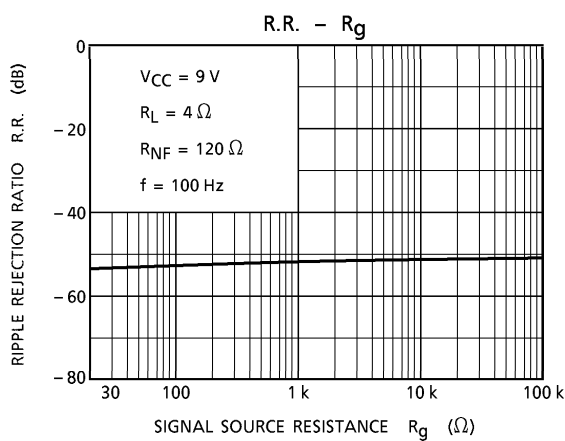
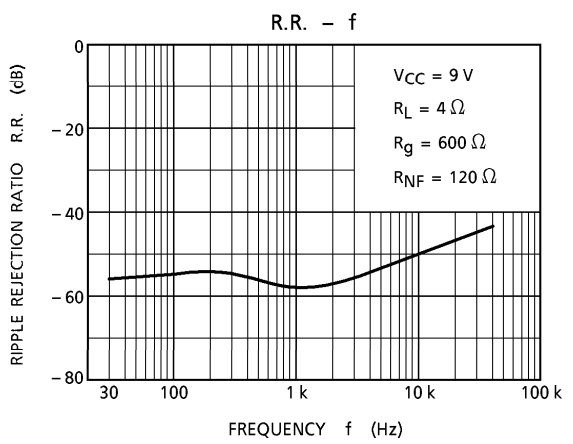
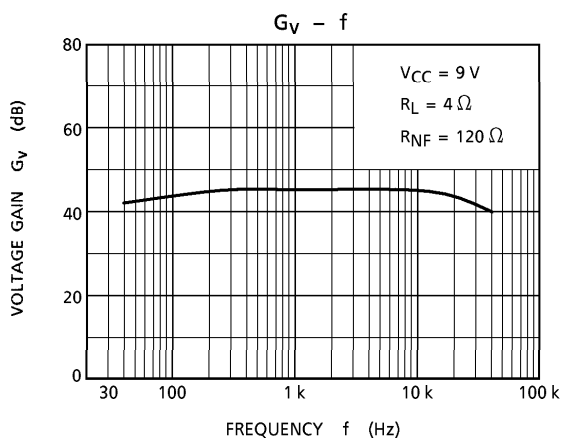
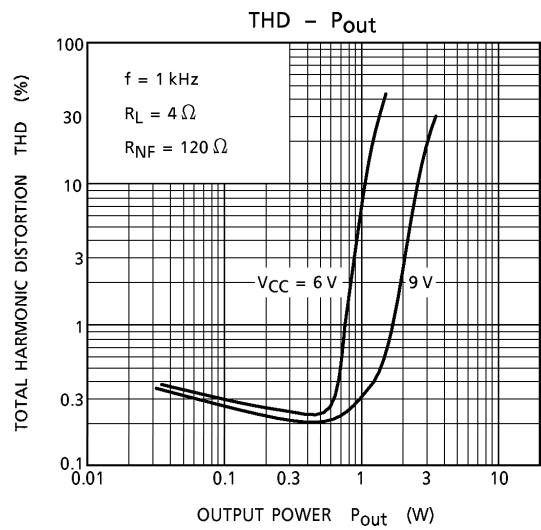
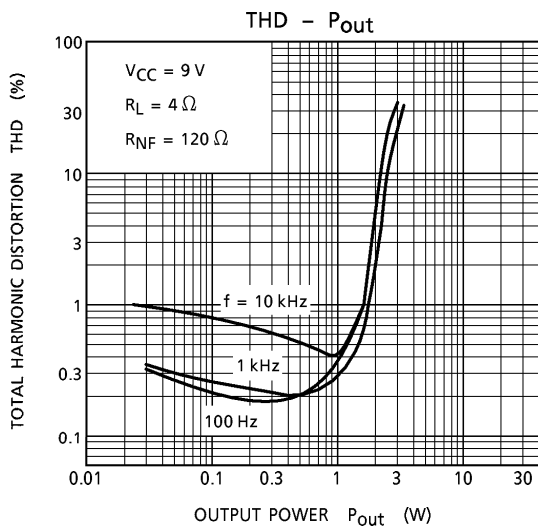
TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
DC Voltage (V)	V <sub>CC</sub>	4.5	8.7	GND	0.7	0.03	0.03	0.7	5.0	8.7	4.5	V <sub>CC</sub>

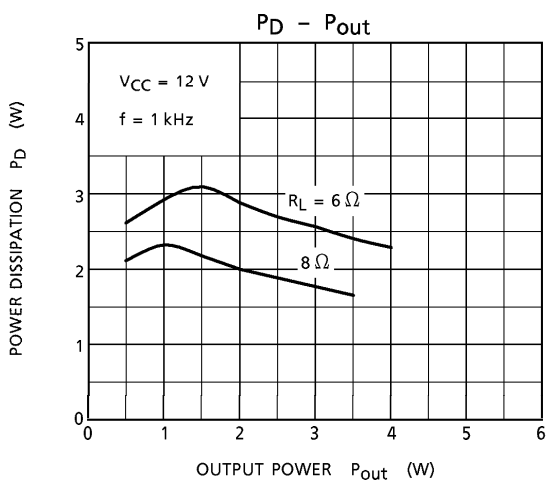
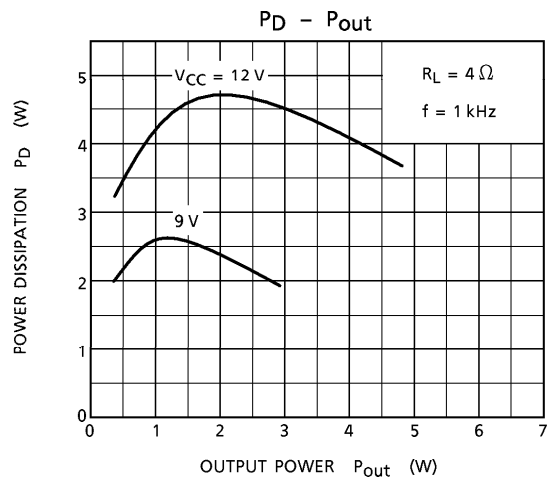
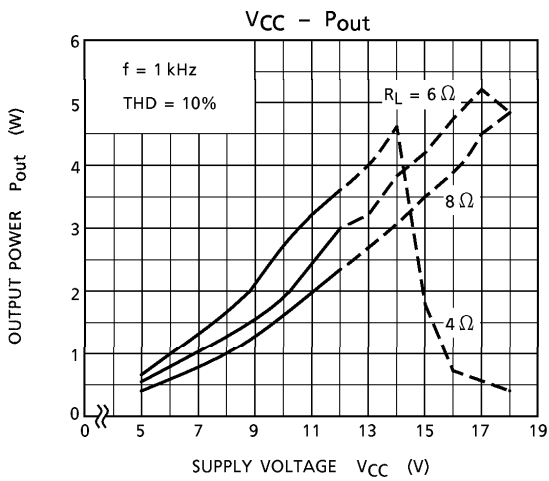
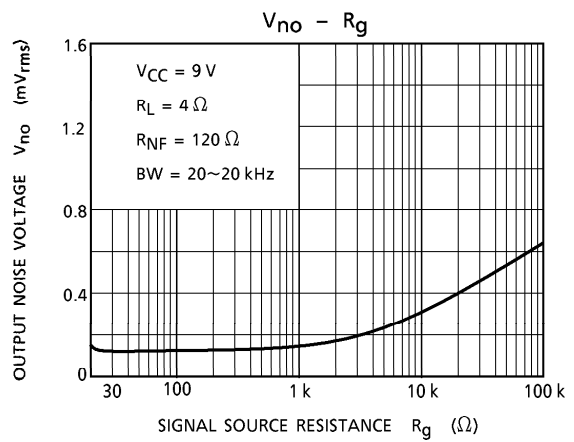
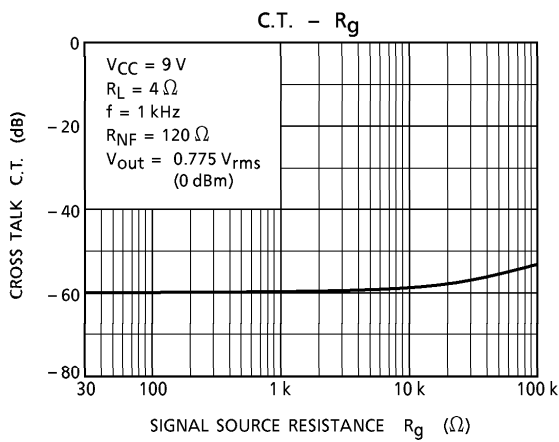
**TEST CIRCUIT**



- (\*1) This IC can be used without coupling capacitor ( $C_{IN}$ ). If volume slide noise occurred by input offset voltage is undesirable, it needs to use the capacitor ( $C_{IN}$ ).
- (\*2) The condenser between the ④pin and the GND ( $C_{11}$ ) is for reducing pop noise when the power ON/OFF switch (SW1) is set to ON/OFF.

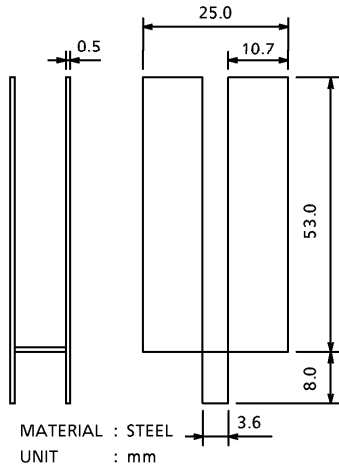




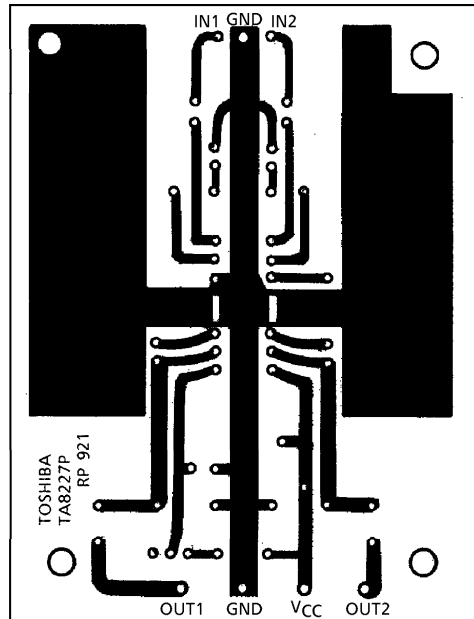




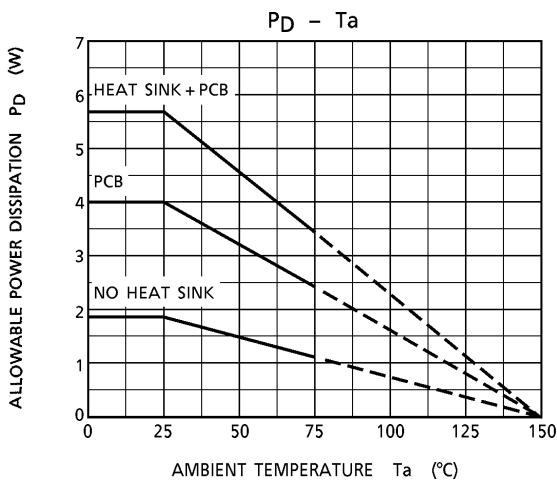
**HEAT SINK**



**RECOMMENDED PCB LAYOUT**

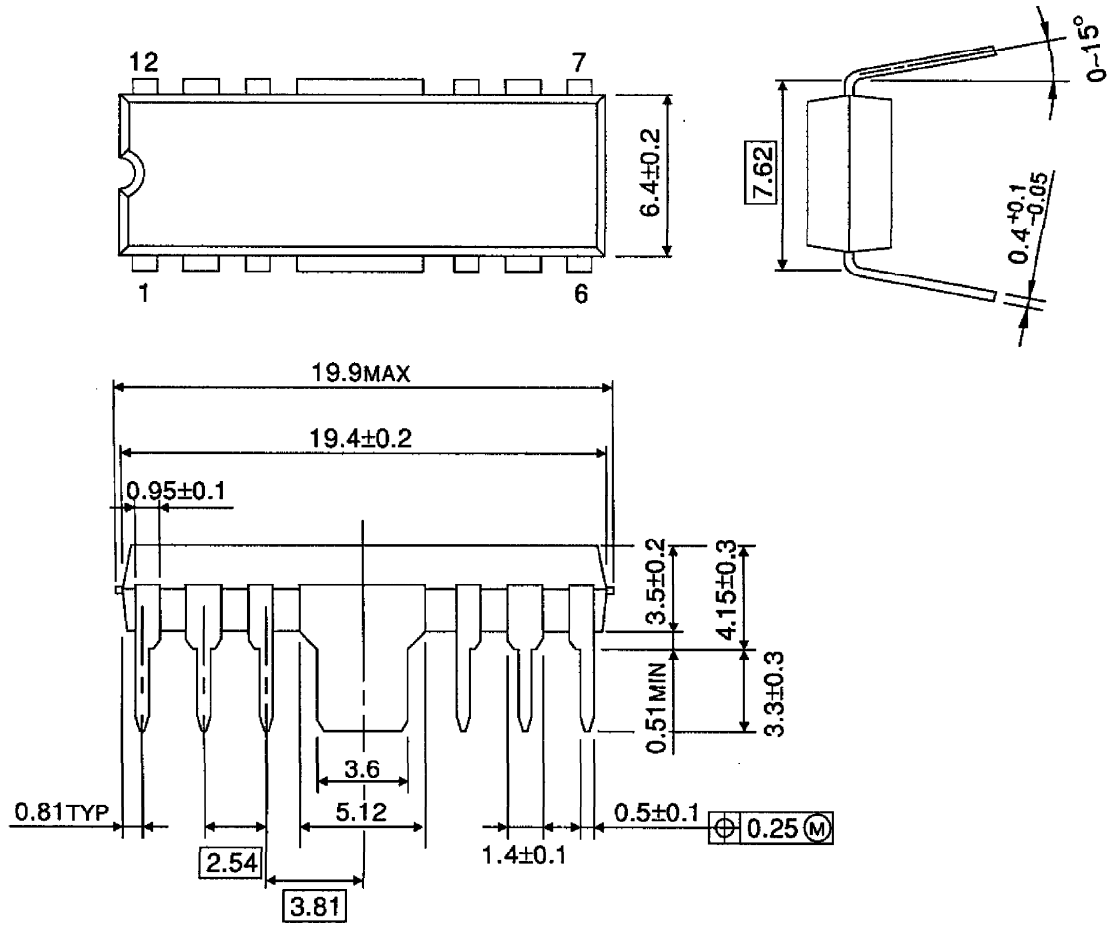


PCB : EPOXY GLASS  
80 mm × 60 mm × 1.2 mm



**OUTLINE DRAWING**  
HDIP12-P-300-2.54

Unit : mm



Weight : 1.4 g (Typ.)