

DATA SHEET

TDA4866

**Full bridge current driven vertical
deflection booster**

Product specification
Supersedes data of 1996 Oct 10
File under Integrated Circuits, IC02

1999 Jun 14

Full bridge current driven vertical deflection booster

TDA4866

FEATURES

- Fully integrated, few external components
- No additional components in combination with the deflection controller TDA485x, TDA4841PS
- Pre-amplifier with differential high CMRR current mode inputs
- Low offsets
- High linear sawtooth signal amplification
- High efficient DC-coupled vertical output bridge circuit
- Powerless vertical shift
- High deflection frequency up to 160 Hz
- Power supply and flyback supply voltage independent adjustable to optimize power consumption and flyback time
- Excellent transition behaviour during flyback
- Guard circuit for screen protection.

GENERAL DESCRIPTION

The TDA4866 is a power amplifier for use in 90 degree colour vertical deflection systems for frame frequencies of 50 to 160 Hz. The circuit provides a high CMRR current driven differential input. Due to the bridge configuration of the two output stages DC-coupling of the deflection coil is achieved. In conjunction with TDA485x, TDA4841PS the ICs offer an extremely advanced system solution.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply; note 1						
V_P	supply voltage (pin 3)		8.2	–	25	V
V_{FB}	flyback supply voltage (pin 7)	note 2	–	–	60	V
I_q	quiescent current (pin 7)		–	7	10	mA
Vertical circuit						
I_{defl}	deflection current (peak-to-peak value; pins 4 and 6)		0.6	–	2	A
I_{id}	differential input current (peak-to-peak value)	note 3	–	±500	±600	µA
Flyback generator						
I_{FB}	maximum current during flyback (peak-to-peak value; pin 7)		–	–	2	A
Guard circuit; note 1						
V_8	guard voltage	guard on	7.5	8.5	10	V
I_8	guard current	guard on	5	–	–	mA

Notes

1. Voltages refer to pin 5 (GND).
2. Up to $60\text{ V} \geq V_{FB} \geq 40\text{ V}$ a decoupling capacitor $C_{FB} = 22\text{ }\mu\text{F}$ (between pin 7 and pin 5) and a resistor $R_{FB} = 100\text{ }\Omega$ (between pin 7 and V_{FB}) are required (see Fig.4).
3. Differential input current $I_{id} = I_1 - I_2$.

Full bridge current driven vertical deflection booster

TDA4866

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4866	SIL9P	plastic single in-line power package; 9 leads	SOT131-2

BLOCK DIAGRAM

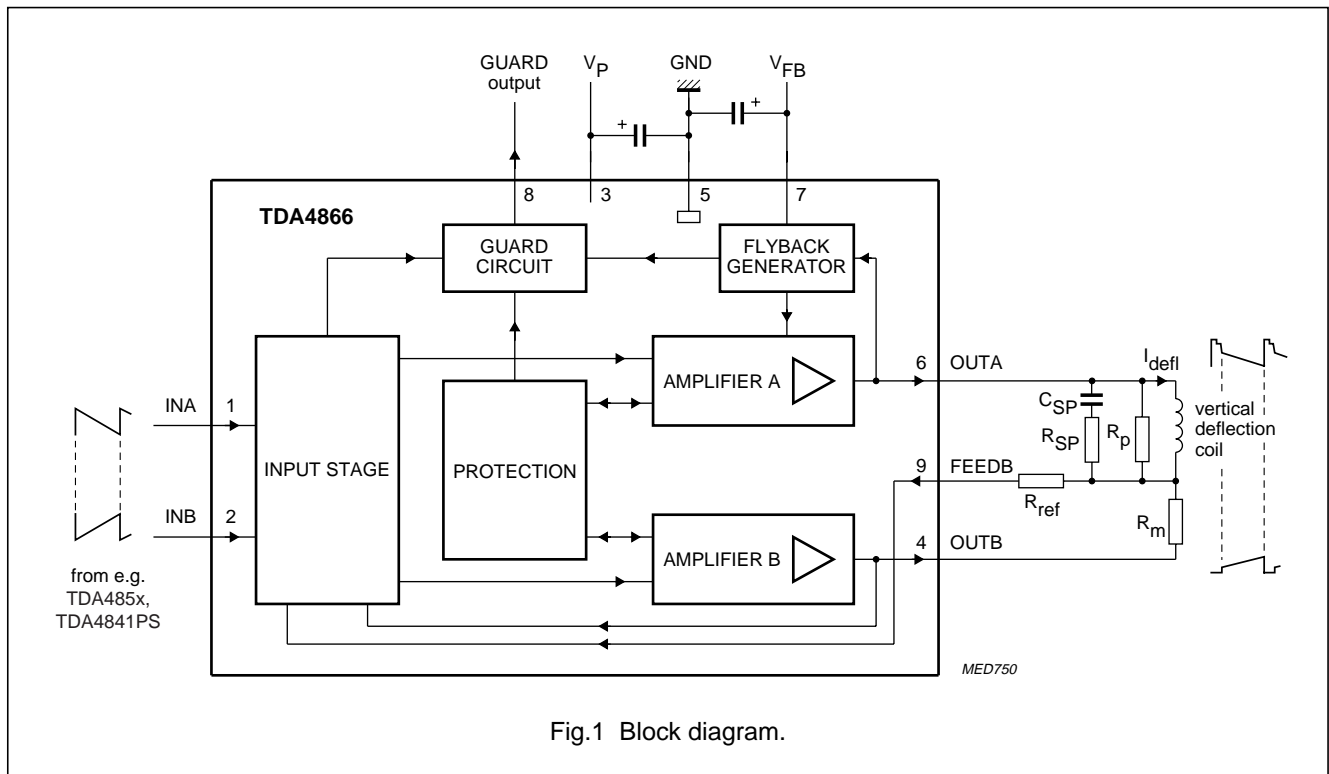


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INA	1	input A
INB	2	input B
V _P	3	supply voltage
OUTB	4	output B
GND	5	ground
OUTA	6	output A
V _{FB}	7	flyback supply voltage
GUARD	8	guard output
FEEDB	9	feedback input

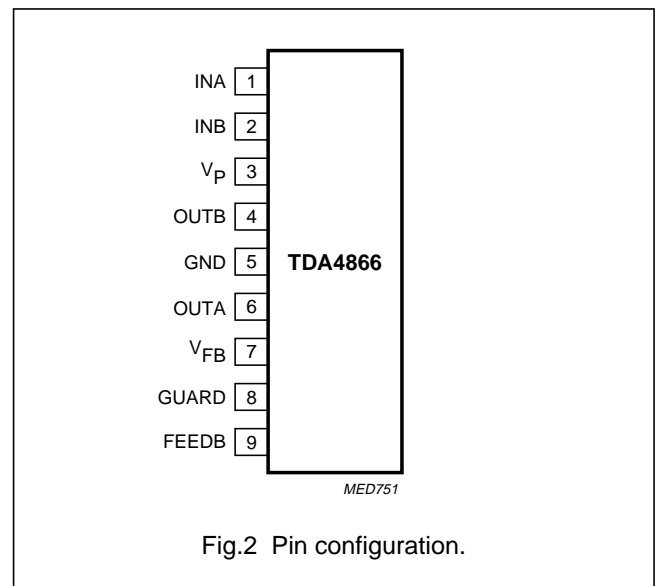


Fig.2 Pin configuration.

Full bridge current driven vertical deflection booster

TDA4866

FUNCTIONAL DESCRIPTION

The TDA4866 consists of a differential input stage, two output stages, a flyback generator, a protection circuit for the output stages and a guard circuit.

Differential input stage

The differential input stage has a high CMRR differential current mode input (pins 1 and 2) that results in a high electro-magnetic immunity and is especially suitable for driver units with differential (e.g. TDA485x, TDA4841PS) and single ended current signals. Driver units with voltage outputs are simply applicable as well (e.g. two additional resistors are required).

The differential input stage delivers the driver signals for the output stages.

Output stages

The two output stages are current driven in opposite phase and operate in combination with the deflection coil in a full bridge configuration. Therefore the TDA4866 requires no external coupling capacitor (e.g. 2200 μF) and operates with one supply voltage V_P and a separate adjustable flyback supply voltage V_{FB} only. The deflection current through the coil (I_{defl}) is measured with the resistor R_m which produces a voltage drop (U_{rm}) of: $U_{rm} \approx R_m \times I_{\text{defl}}$. At the feedback input (pin 9) a part of I_{defl} is fed back to the input stage. The feedback input has a current input characteristic which holds the differential voltage between pin 9 and the output pin 4 on zero. Therefore the feedback current (I_g) through R_{ref} is:

$$I_g \approx \frac{R_m}{R_{\text{ref}}} \times I_{\text{defl}}$$

The input stage directly compares the driver currents into pins 1 and 2 with the feedback current I_g . Any difference of this comparison leads to a more or less driver current for the output stages. The relation between the deflection current and the differential input current (I_{id}) is:

$$I_{\text{id}} = I_g \approx \frac{R_m}{R_{\text{ref}}} \times I_{\text{defl}}$$

Due to the feedback loop gain ($V_{U \text{ loop}}$) and internal bondwire resistance (R_{bo}) correction factors are required to determine the accurate value of I_{defl} :

$$I_{\text{defl}} = I_{\text{id}} \times \frac{R_{\text{ref}}}{R_m + R_{\text{bo}}} \times \left(1 - \frac{1}{V_{U \text{ loop}}}\right)$$

with $R_{\text{bo}} \approx 70 \text{ m}\Omega$ and $\left(1 - \frac{1}{V_{U \text{ loop}}}\right) \approx 0.98$

for $I_{\text{defl}} = 0.7 \text{ A}$.

The deflection current can be adjusted up to $\pm 1 \text{ A}$ by varying R_{ref} when R_m is fixed to 1Ω .

High bandwidth and excellent transition behaviour is achieved due to the transimpedance principle this circuit works with.

Flyback generator

During flyback the flyback generator supplies the output stage A with the flyback voltage. This makes it possible to optimize power consumption (supply voltage V_P) and flyback time (flyback voltage V_{FB}). Due to the absence of a decoupling capacitor the flyback voltage is fully available.

In parallel with the deflection yoke and the damping resistor (R_p) an additional RC combination (R_{SP} ; C_{SP}) is necessary to achieve an optimized flyback behaviour.

Protection

The output stages are protected against:

- Thermal overshoot
- Short-circuit of the coil (pins 4 and 6).

Guard circuit

The internal guard circuit provides a blanking signal for the CRT. The guard signal is active HIGH:

- At thermal overshoot
- When feedback loop is out of range
- During flyback.

The internal guard circuit will not be activated, if the input signals on pins 1 and 2 delivered from the driver circuit are out of range or at short-circuit of the coil (pins 4 and 6).

For this reason an external guard circuit can be applied to detect failures of the deflection (see Fig.6). This circuit will be activated when flyback pulses are missing, which is the indication of any abnormal operation.

Full bridge current driven vertical deflection booster

TDA4866

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages referenced to pin 5 (GND); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 3)		0	30	V
V_{FB}	flyback supply voltage (pin 7)		0	60	V
I_{FB}	flyback supply current		0	± 1.8	A
V_1, V_2	input voltage		0	V_P	V
I_1, I_2	input current		0	± 5	mA
V_4, V_6	output voltage		0	V_P	V
I_4, I_6	output current	note 1	0	± 1.8	A
V_9	feedback voltage		0	V_P	V
I_9	feedback current		0	± 5	mA
V_8	guard voltage	note 2	0	$V_P + 0.4$	V
I_8	guard current		0	± 5	mA
T_{stg}	storage temperature		-20	+150	°C
T_{amb}	operating ambient temperature		-20	+75	°C
T_j	junction temperature	note 3	-20	+150	°C
V_{es}	electrostatic handling for all pins	note 4	-500	+500	V

Notes

1. Maximum output currents I_4 and I_6 are limited by current protection.
2. For $V_P > 13$ V the guard voltage V_8 is limited to 13 V.
3. Internally limited by thermal protection; switching point ≥ 150 °C.
4. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	4	K/W

Full bridge current driven vertical deflection booster

TDA4866

CHARACTERISTICS

$V_P = 15\text{ V}$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$; $V_{\text{FB}} = 40\text{ V}$; voltages referenced to pin 5 (GND); parameters are measured in test circuit (see Fig.3); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 3)		8.2	–	25	V
V_{FB}	flyback supply voltage (pin 7)	note 1	$V_P + 6$	–	60	V
I_{FB}	quiescent feedback current (pin 7)	no load; no signal	–	7	10	mA
Input stage						
$I_{\text{id(p-p)}}$	differential input current ($I_{\text{id}} = I_1 - I_2$) (peak-to-peak value)		–	± 500	± 600	μA
$I_{1, 2(\text{p-p})}$	single ended input current (peak-to-peak value)	note 2	0	± 300	± 600	μA
CMRR	common mode rejection ratio	note 3	–	–54	–	dB
V_1	input clamp voltage	$I_1 = 300\text{ }\mu\text{A}$	2.7	3.0	3.3	V
V_2	input clamp voltage	$I_2 = 300\text{ }\mu\text{A}$	2.7	3.0	3.3	V
$\text{TC}_{i,1}$	input clamp signal TC on pin 1		0	–	± 800	$\mu\text{V/K}$
$\text{TC}_{i,2}$	input clamp signal TC on pin 2		0	–	± 800	$\mu\text{V/K}$
$V_1 - V_2$	differential input voltage	$I_{\text{id}} = 0$	0	–	± 10	mV
I_9	feedback current		–	± 500	± 600	μA
V_9	feedback voltage		1	–	$V_P - 1$	V
$I_{\text{id(offset)}}$	differential input offset current ($I_{\text{id(offset)}} = I_1 - I_2$)	$I_{\text{defl}} = 0$; $R_{\text{ref}} = 1.5\text{ k}\Omega$; $R_{\text{m}} = 1\text{ }\Omega$	0	–	± 20	μA
$C_{i\text{ INA}}$	input capacity pin 1 referenced to GND		–	–	5	pF
$C_{i\text{ INB}}$	input capacity pin 2 referenced to GND		–	–	5	pF
Output stages A and B						
I_4	output current		–	–	± 1	A
I_6	output current		–	–	± 1	A
V_6	output A saturation voltage to GND	$I_6 = 0.7\text{ A}$	–	1.3	1.5	V
		$I_6 = 1.0\text{ A}$	–	1.6	1.8	V
$V_{6,3}$	output A saturation voltage to V_P	$I_6 = 0.7\text{ A}$	–	2.3	2.9	V
		$I_6 = 1.0\text{ A}$	–	2.7	3.3	V
V_4	output B saturation voltage to GND	$I_4 = 0.7\text{ A}$	–	1.3	1.5	V
		$I_4 = 1.0\text{ A}$	–	1.6	1.8	V
$V_{4,3}$	output B saturation voltage to V_P	$I_4 = 0.7\text{ A}$	–	1.0	1.6	V
		$I_4 = 1.0\text{ A}$	–	1.3	1.9	V
LE	linearity error	$I_{\text{defl}} = \pm 0.7\text{ A}$; note 4	–	–	2	%
V_4	DC output voltage	$I_{\text{id}} = 0\text{ A}$; closed-loop	6.6	7.2	7.8	V
V_6	DC output voltage	$I_{\text{id}} = 0\text{ A}$; closed-loop	6.6	7.2	7.8	V
G_{oi}	open-loop current gain ($I_4, 6/I_{\text{id}}$)	$I_4, 6 < 100\text{ mA}$; note 5	–	100	–	dB
G_{ofb}	open-loop current gain ($I_4, 6/I_9$)	$I_4, 6 < 100\text{ mA}$; note 5	–	100	–	dB
G_{ifb}	current ratio (I_{id}/I_9)	closed-loop	–	–0.2	–	dB

Full bridge current driven vertical deflection booster

TDA4866

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{\text{def(ripple)}}$	output ripple current as a function of supply ripple	$V_{\text{P(ripple)}} = \pm 0.5 \text{ V}$; $I_{\text{id}} = 0$; closed-loop	–	± 1	–	mA
Flyback generator						
$V_{7,6}$	voltage drop during flyback reverse	$I_{\text{def}} = 0.7 \text{ A}$	–	–2.0	–3.0	V
		$I_{\text{def}} = 1.0 \text{ A}$	–	–2.3	–3.5	V
	forward	$I_{\text{def}} = 0.7 \text{ A}$	–	+5.6	+6.1	V
		$I_{\text{def}} = 1.0 \text{ A}$	–	+5.9	+6.5	V
V_6	switching on threshold voltage		$V_{\text{P}} - 1$	–	$V_{\text{P}} + 1.5$	V
V_6	switching off threshold voltage		$V_{\text{P}} - 1.5$	–	$V_{\text{P}} + 1$	V
I_7	flyback current during flyback		–	–	± 1	A
Guard circuit						
V_8	output voltage	guard on	7.5	8.5	10	V
V_8	output voltage	guard on; $V_{\text{P}} = 8.2 \text{ V}$	6.9	–	$V_{\text{P}} - 0.4$	V
I_8	output current	guard on	5	–	–	mA
V_8	output voltage	guard off	–	–	0.4	V
I_8	output current	guard off; $V_8 = 5 \text{ V}$	0.5	1	1.5	mA
$V_{8(\text{ext.})}$	allowable external voltage on pin 8		0	–	13	V
		$V_{\text{P}} \leq 13 \text{ V}$	0	–	$V_{\text{P}} + 0.3$	V

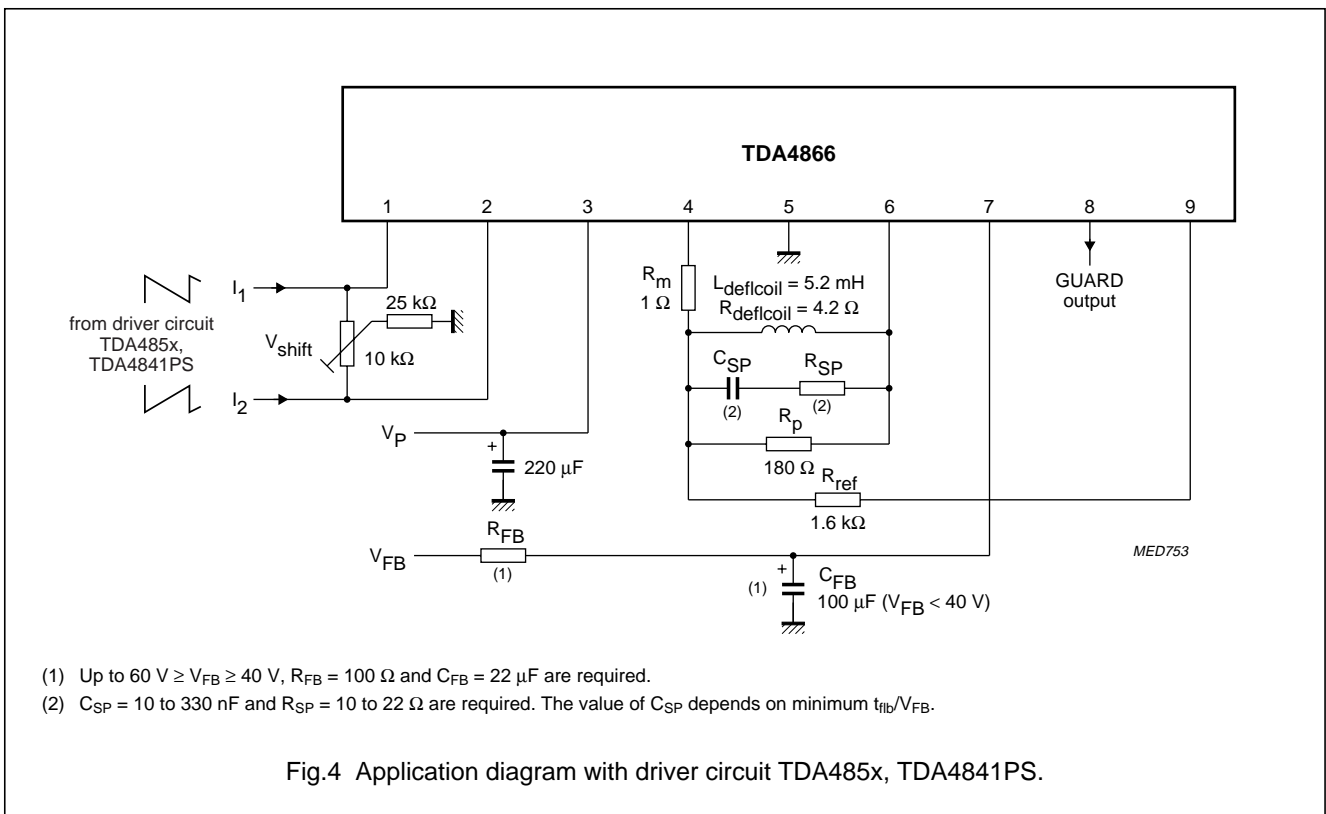
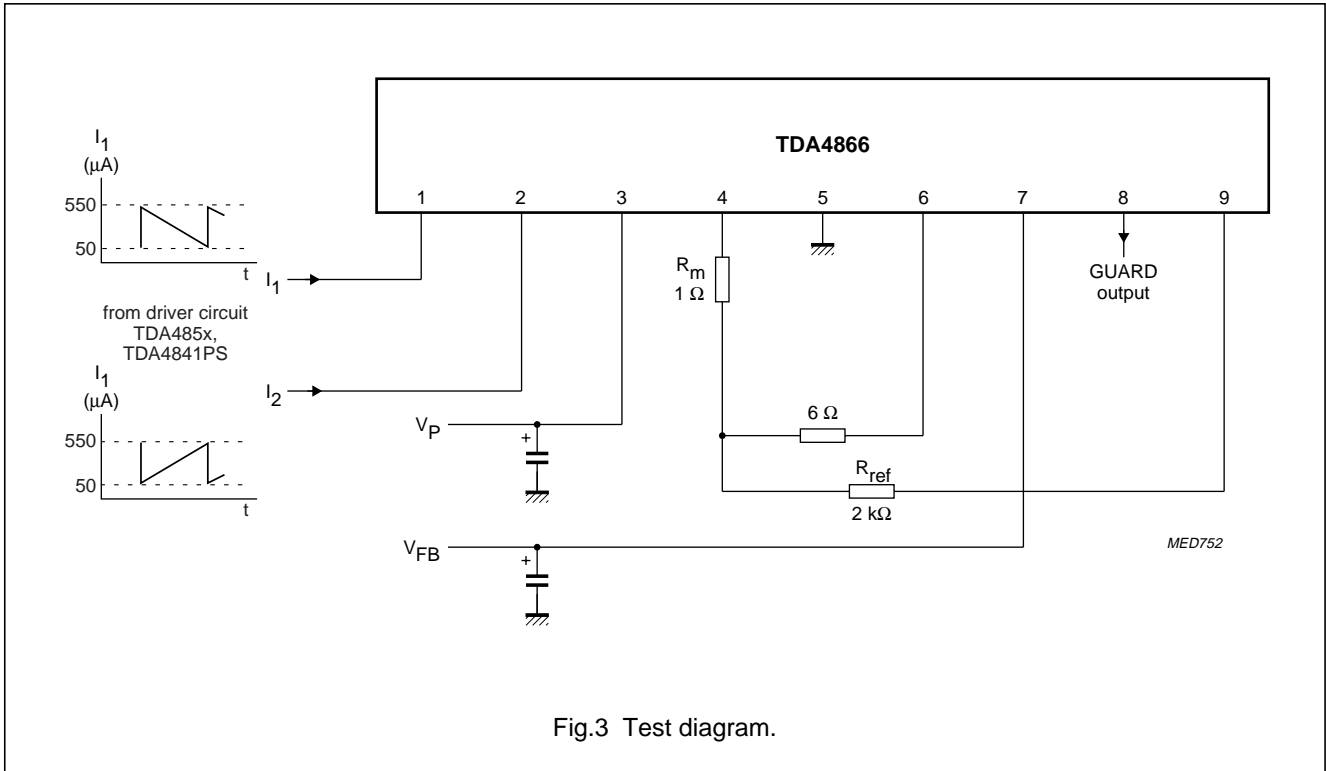
Notes

- Up to $60 \text{ V} \geq V_{\text{FB}} \geq 40 \text{ V}$ a decoupling capacitor $C_{\text{FB}} = 22 \mu\text{F}$ (between pins 7 and 5) and a resistor $R_{\text{FB}} = 100 \Omega$ (between pin 7 and V_{FB}) are required (see Fig.4).
- Saturation voltages of output stages A and B can be increased in the event of negative input currents $I_{1,2} < -500 \mu\text{A}$.
- $D_i = \frac{I_{\text{deflc}}}{I_{\text{idc}}} \times \frac{I_{\text{id}}}{I_{\text{def}}}$ with I_{deflc} = common mode deflection current and I_{idc} = common mode input current.
- Deviation of the output slope at a constant input slope.
- Frequency behaviour of G_{oi} and G_{ofb} :
 - 3 dB open-loop bandwidth (-45°) at 15 kHz; second pole (-135°) at 1.3 MHz.
 - Open-loop gain at second pole (-135°) 55 dB.

Full bridge current driven vertical deflection booster

TDA4866

TEST AND APPLICATION INFORMATION



Full bridge current driven vertical deflection booster

TDA4866

Example

SYMBOL	VALUE	UNIT
Values given from application		
$I_{defl(max)}$	0.71	A
$L_{deflcoil}$	5.2	mH
$R_{deflcoil}$	5.4 [= 4.2 + 7% + $\Delta R(\vartheta)$]	Ω
R_m	1 (+1%)	Ω
R_p	180	Ω
R_{ref}	1.6	k Ω
V_{FB}	35	V
T_{amb}	+50	$^{\circ}C$
$T_{deflcoil}$	+75	$^{\circ}C$
$R_{th(j-mb)}$	4	K/W
$R_{th(mb-amb)}^{(1)}$	8	K/W
Calculated values		
V_P	8.6	V
t_{flb}	270	μs
P_{tot}	3.65	W
P_{defl}	0.9	W
P_{IC}	2.75	W
$R_{th(tot)}$	12	K/W
$T_{j(max)}^{(2)}$	+83	$^{\circ}C$

Notes

1. A layer of silicon grease between the mounting base and the heatsink optimizes thermal resistance.
2. $T_{j(max)} = P_{IC} \times [R_{th(j-mb)} + R_{th(mb-amb)}] + T_{amb}$

Calculation formula for supply voltage and power consumption

$$V_{b1} = V_{6,3} + R_{deflcoil} \times I_{defl(max)} - U'_L + R_m \times I_{defl(max)} + V_4$$

$$V_{b2} = V_6 + R_{deflcoil} \times I_{defl(max)} + U'_L + R_m \times I_{defl(max)} + V_{4,3}$$

for $V_{b1} > V_{b2}$: $V_P = V_{b1}$

for $V_{b2} > V_{b1}$: $V_P = V_{b2}$

with:

$$U'_L = L_{deflcoil} \times 2I_{defl(max)} \times f_v$$

f_v = vertical deflection frequency.

$$P_{tot} = V_P \times \frac{I_{defl(max)}}{2} + V_P \times 0.03 \text{ A} + 0.1 \text{ W} + V_{FB} \times I_{FB}$$

$$P_{defl} = \frac{1}{3} (R_{deflcoil} + R_m) \times I_{defl(max)}^2$$

$$P_{IC} = P_{tot} - P_{defl}$$

P_{IC} = power dissipation of the IC

P_{defl} = power dissipation of the deflection coil

P_{tot} = total power dissipation.

Calculation formula for flyback time (t_{flb})

$$t_{flb} = \frac{L_{deflcoil}}{R_{deflcoil} + R_m} \times \ln \left(\frac{1 + \frac{(R_{deflcoil} + R_m) \times I_{defl(max)}}{V_{FB} + V_{7r} - V_{6r}}}{1 - \frac{(R_{deflcoil} + R_m) \times I_{defl(max)}}{V_{FB} - (V_{7f} - V_{6f})}} \right) + t_{flb(off)}$$

with:

$t_{flb(off)}$ = flyback switch off time = 50 μs for this application ($t_{flb(off)}$ depends on V_{FB} , $I_{defl(max)}$, $L_{deflcoil}$ and C_{SP}).

To achieve good noise suppression the following values for R_p are recommended:

Recommended values

$L_{deflcoil}$ (mH)	R_p (Ω)
3	100
6	180
10	240
15	390

Full bridge current driven vertical deflection booster

TDA4866

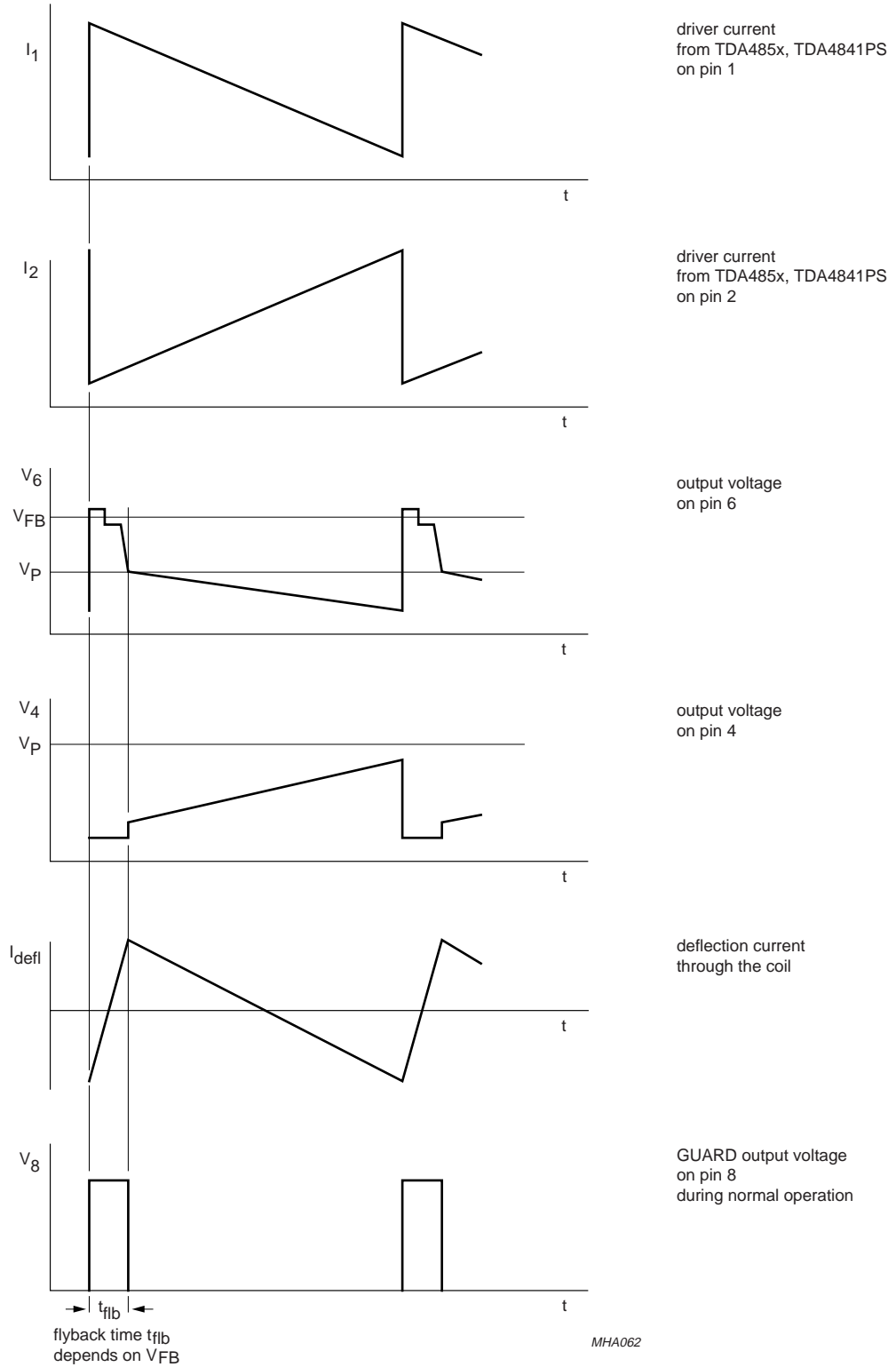


Fig.5 Timing diagram.

Full bridge current driven vertical deflection booster

TDA4866

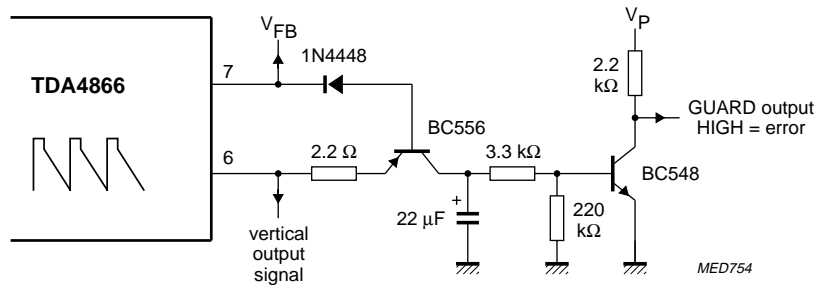


Fig.6 Application circuit for external guard signal generation.

INTERNAL PIN CONFIGURATION

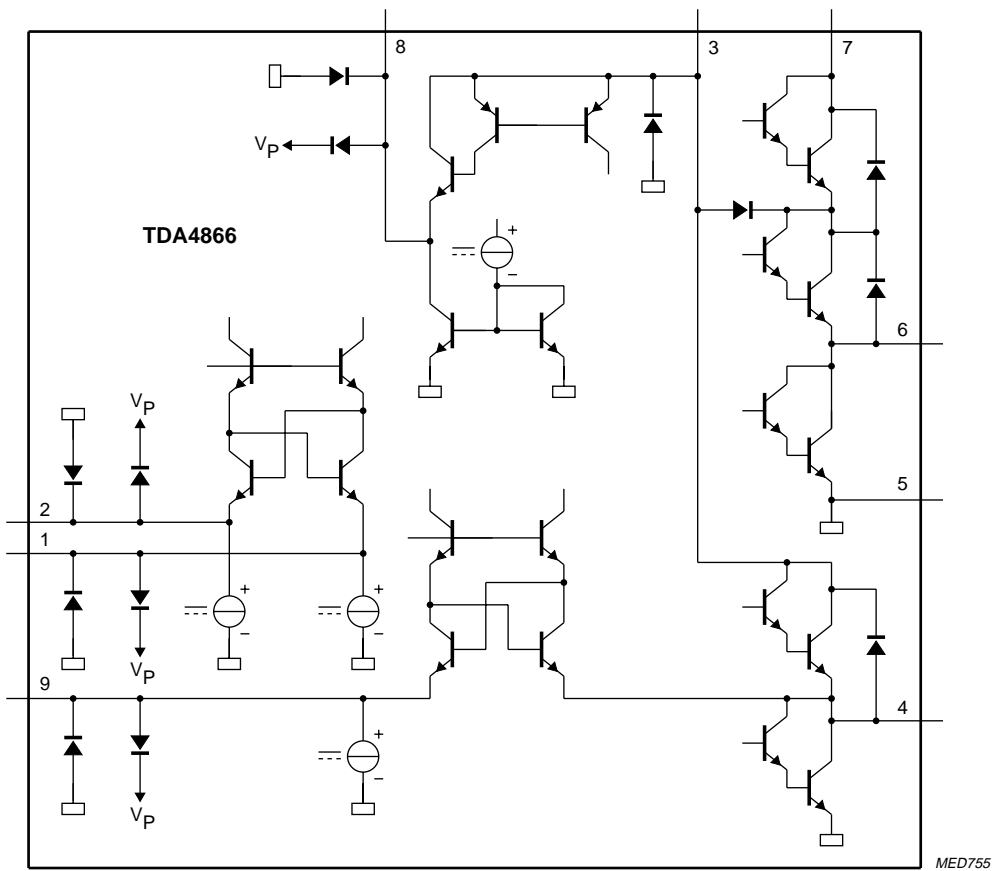


Fig.7 Internal circuits.

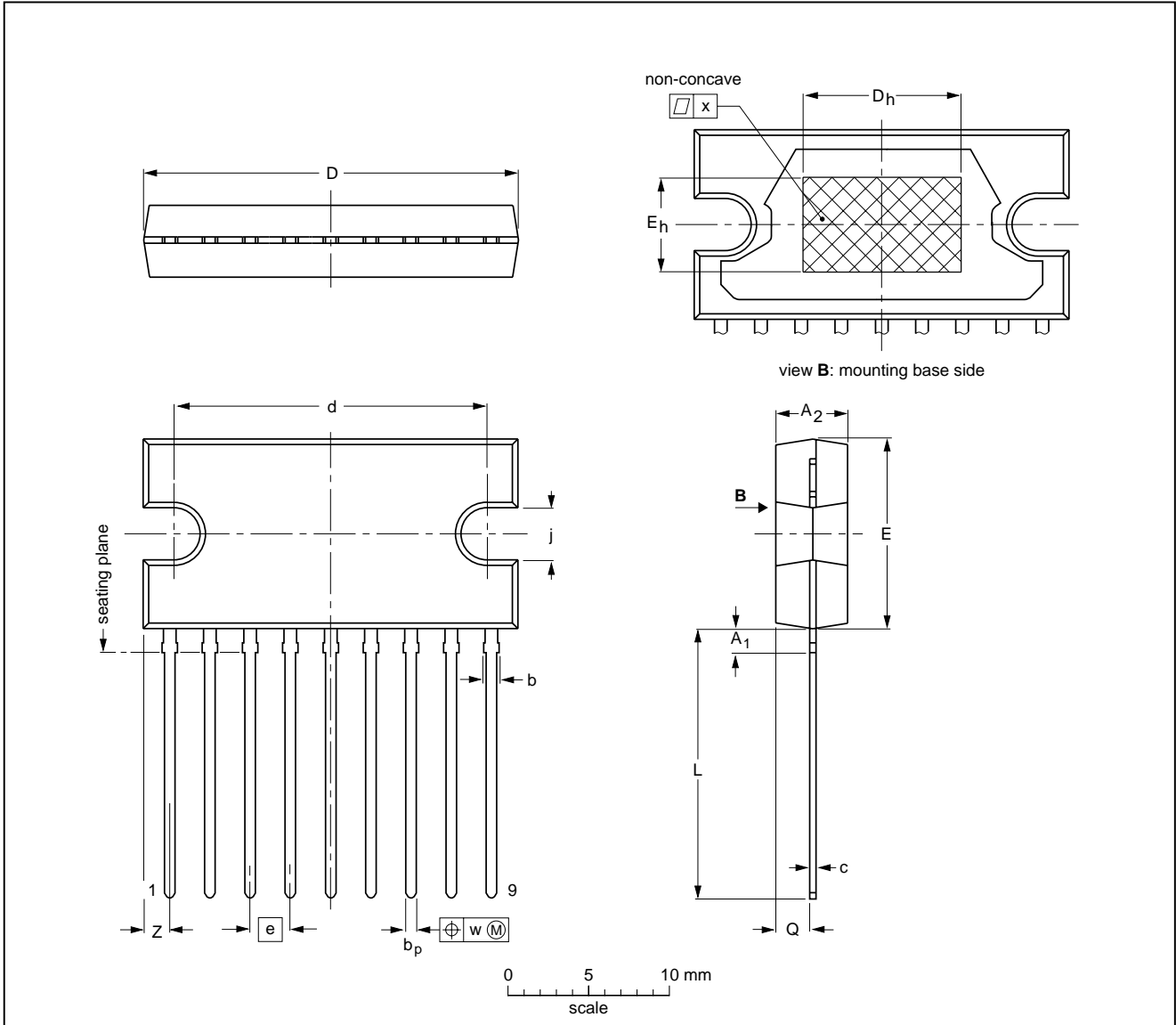
Full bridge current driven vertical deflection booster

TDA4866

PACKAGE OUTLINE

SIL9P: plastic single in-line power package; 9 leads

SOT131-2



DIMENSIONS (mm are the original dimensions)

UNIT	A ₁ max.	A ₂	b max.	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	E _h	j	L	Q	w	x	Z ⁽¹⁾
mm	2.0	4.6 4.2	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						92-11-17 95-03-11

Full bridge current driven vertical deflection booster

TDA4866

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable ⁽¹⁾

Note

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Full bridge current driven vertical deflection
booster

TDA4866

NOTES

Full bridge current driven vertical deflection
booster

TDA4866

NOTES

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SCA 66

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