PRELIMINARY

SMART 3 ADVANCED BOOT BLOCK 4-, 8-, 16-, 32-MBIT FLASH MEMORY FAMILY

28F400B3, 28F800B3, 28F160B3, 28F320B3

28F008B3, 28F016B3, 28F032B3

- **Flexible SmartVoltage Technology**
  - **2.7 V–3.6 V Read/Program/Erase**
  - **12 V V_{PP} Fast Production Programming**
- **2.7 V or 1.65 V I/O Option**
  - **Reduces Overall System Power**
- **High Performance**
  - **2.7 V–3.6 V: 90 ns Max Access Time**
  - **3.0 V–3.6 V: 80 ns Max Access Time**
- **Optimized Block Sizes**
  - **Eight 8-KB Blocks for Data, Top or Bottom Locations**
  - **Up to Sixty-Three 64-KB Blocks for Code**
- **Block Locking**
  - **V_{CC}-Level Control through WP#**
- **Low Power Consumption**
  - **10 mA Typical Read Current**
- **Absolute Hardware-Protection**
  - **V_{PP} = GND Option**
  - **V_{CC} Lockout Voltage**
- **Extended Temperature Operation**
  - **–40 °C to +85 °C**
- **Flash Data Integrator Software**
  - **Flash Memory Manager**
  - **System Interrupt Manager**
  - **Supports Parameter Storage, Streaming Data (e.g., Voice)**
- **Automated Program and Block Erase**
  - **Status Registers**
- **Extended Cycling Capability**
  - **Minimum 100,000 Block Erase Cycles Guaranteed**
- **Automatic Power Savings Feature**
  - **Typical I_{CCS} after Bus Inactivity**
- **Standard Surface Mount Packaging**
  - **48-Ball µBGA* Package**
  - **48-Lead TSOP Package**
  - **40-Lead TSOP Package**
- **Footprint Upgradeable**
  - **Upgrade Path for 4-, 8-, 16-, and 32-Mbit Densities**
- **ETOX™ VI (0.25 µ) Flash Technology**

The Smart 3 Advanced Boot Block, manufactured on Intel's latest 0.25 µ technology, represents a feature-rich solution at overall lower system cost. Smart 3 flash memory devices incorporate low voltage capability (2.7 V read, program and erase) with high-speed, low-power operation. Several new features have been added, including the ability to drive the I/O at 1.65 V, which significantly reduces system active power and interfaces to 1.65 V controllers. A new blocking scheme enables code and data storage within a single device. Add to this the Intel-developed Flash Data Integrator (FDI) software, and you have a cost-effective, monolithic code plus data storage solution. Smart 3 Advanced Boot Block products will be available in 40-lead and 48-lead TSOP and 48-ball µBGA* packages. Additional information on this product family can be obtained by accessing Intel's WWW page: http://www.intel.com/design/flash.

July 1998

Order Number: 290580-005

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REVISION HISTORY

Number	Description
-001	Original version
-002	Section 3.4, *V_{PP} Program and Erase Voltages*, added Updated Figure 9: *Automated Block Erase Flowchart* Updated Figure 10: *Erase Suspend/Resume Flowchart* (added program to table) Updated Figure 16: *AC Waveform: Program and Erase Operations* (updated notes) I_{PPR} maximum specification change from ±25 µA to ±50 µA Program and Erase Suspend Latency specification change Updated Appendix A: *Ordering Information* (included 8 M and 4 M information) Updated Figure, Appendix D: *Architecture Block Diagram* (Block info. in words not bytes) Minor wording changes
-003	Combined byte-wide specification (previously 290605) with this document Improved speed specification to 80 ns (3.0 V) and 90 ns (2.7 V) Improved 1.8 V I/O option to minimum 1.65 V (Section 3.4) Improved several DC characteristics (Section 4.4) Improved several AC characteristics (Sections 4.5 and 4.6) Combined 2.7 V and 1.8 V DC characteristics (Section 4.4) Added 5 V V_{PP} read specification (Section 3.4) Removed 120 ns and 150 ns speed offerings Moved *Ordering Information* from Appendix to Section 6.0; updated information Moved *Additional Information* from Appendix to Section 7.0 Updated figure Appendix B, *Access Time vs. Capacitive Load* Updated figure Appendix C, *Architecture Block Diagram* Moved Program and Erase Flowcharts to Appendix E Updated *Program Flowchart* Updated *Program Suspend/Resume Flowchart* Minor text edits throughout.
-004	Added 32-Mbit density Added 98H as a reserved command (Table 4) A_1–A_{20} = 0 when in read identifier mode (Section 3.2.2) Status register clarification for SR3 (Table 7) V_{CC} and V_{CCQ} absolute maximum specification = 3.7 V (Section 4.1) Combined I_{PPW} and I_{CCW} into one specification (Section 4.4) Combined I_{PPE} and I_{CCE} into one specification (Section 4.4) Max Parameter Block Erase Time (t_{WHQV2}/t_{EHQV2}) reduced to 4 sec (Section 4.7) Max Main Block Erase Time (t_{WHQV3}/t_{EHQV3}) reduced to 5 sec (Section 4.7) Erase suspend time @ 12 V (t_{WHRH2}/t_{EHRH2}) changed to 5 µs typical and 20 µs maximum (Section 4.7) *Ordering Information* updated (Section 6.0) Write State Machine Current/Next States Table updated (Appendix A) Program Suspend/Resume Flowchart updated (Appendix F) Erase Suspend/Resume Flowchart updated (Appendix F) Text clarifications throughout
-005	µBGA package diagrams corrected (Figures 3 and 4) I_{PPD} test conditions corrected (Section 4.4) 32-Mbit ordering information corrected (Section 6) µBGA package top side mark information added (Section 6)

1.0 INTRODUCTION

This datasheet contains the specifications for the Advanced Boot Block flash memory family, which is optimized for low power, portable systems. This family of products features 1.65 V–2.5 V or 2.7 V–3.6 V I/Os and a low V_{CC}/V_{PP} operating range of 2.7 V–3.6 V for read, program, and erase operations. In addition this family is capable of fast programming at 12 V. Throughout this document, the term "2.7 V" refers to the full voltage range 2.7 V–3.6 V (except where noted otherwise) and "V_{PP} = 12 V" refers to 12 V ±5%. Section 1.0 and 2.0 provide an overview of the flash memory family including applications, pinouts and pin descriptions. Section 3.0 describes the memory organization and operation for these products. Sections 4.0 and 5.0 contain the operating specifications. Finally, Sections 6.0 and 7.0 provide ordering and other reference information.

1.1 Smart 3 Advanced Boot Block Flash Memory Enhancements

The Smart 3 Advanced Boot Block flash memory features

- Enhanced blocking for easy segmentation of code and data or additional design flexibility
- Program Suspend to Read command
- V_{CCQ} input of 1.65 V–2.5 V on all I/Os. See Figures 1 through 4 for pinout diagrams and V_{CCQ} location
- Maximum program and erase time specification for improved data storage.

Table 1. Smart 3 Advanced Boot Block Feature Summary

Feature	28F008B3, 28F016B3, 28F032B3(1)	28F400B3(2), 28F800B3, 28F160B3, 28F320B3	Reference
V_{CC} Read Voltage	2.7 V– 3.6 V		Section 4.2, 4.4
V_{CCQ} I/O Voltage	1.65 V–2.5 V or 2.7 V– 3.6 V		Section 4.2, 4.4
V_{PP} Program/Erase Voltage	2.7 V– 3.6 V or 11.4 V– 12.6 V		Section 4.2, 4.4
Bus Width	8-bit	16 bit	Table 3
Speed	80 ns, 90 ns, 100 ns, 110 ns		Section 4.5
Memory Arrangement	1024 Kbit x 8 (8 Mbit), 2048 Kbit x 8 (16 Mbit), 4096 Kbit x 8 (32 Mbit)	256 Kbit x 16 (4 Mbit), 512 Kbit x 16 (8 Mbit), 1024 Kbit x 16 (16 Mbit) 2048 Kbit x 16 (32 Mbit)	Section 2.2
Blocking (top or bottom)	Eight 8-Kbyte parameter blocks **and** Seven 64-Kbyte blocks (4-Mbit) or Fifteen 64-Kbyte blocks (8-Mbit) or Thirty-one 64-Kbyte main blocks (16-Mbit) Sixty-three 64-Kbyte main blocks (32-Mbit)		Section 2.2 Appendix D
Locking	WP# locks/unlocks parameter blocks All other blocks protected using V_{PP}		Section 3.3 Table 8
Operating Temperature	Extended: –40 °C to +85 °C		Section 4.2, 4.4
Program/Erase Cycling	100,000 cycles		Section 4.2, 4.4
Packages	40-lead TSOP(1), 48-Ball µBGA* CSP(2)	48-Lead TSOP, 48-Ball µBGA CSP(2)	Figure 3, Figure 4

NOTES:

1. 4-Mbit and 32-Mbit density not available in 40-lead TSOP.
2. 4-Mbit density not available in µBGA* CSP.

1.2 Product Overview

Intel provides the most flexible voltage solution in the flash industry, providing three discrete voltage supply pins: V_{CC} for read operation, V_{CCQ} for output swing, and V_{PP} for program and erase operation. All Smart 3 Advanced Boot Block flash memory products provide program/erase capability at 2.7 V or 12 V [for fast production programming] and read with V_{CC} at 2.7 V. Since many designs read from the flash memory a large percentage of the time, 2.7 V V_{CC} operation can provide substantial power savings.

The Smart 3 Advanced Boot Block flash memory products are available in either x8 or x16 packages in the following densities: (see *Ordering Information* for availability.)

- 4-Mbit (4,194,304-bit) flash memory organized as 256 Kwords of 16 bits each or 512 Kbytes of 8-bits each
- 8-Mbit (8,388,608-bit) flash memory organized as 512 Kwords of 16 bits each or 1024 Kbytes of 8-bits each
- 16-Mbit (16,777,216-bit) flash memory organized as 1024 Kwords of 16 bits each or 2048 Kbytes of 8-bits each
- 32-Mbit (33,554,432-bit) flash memory organized as 2048 Kwords of 16 bits each or 4096 Kbytes of 8-bits each

The parameter blocks are located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map in order to accommodate different microprocessor protocols for kernel code location. The upper two (or lower two) parameter blocks can be locked to provide complete code security for system initialization code. Locking and unlocking is controlled by WP# (see Section 3.3 for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the flash memory. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations, including verification, thereby un-burdening the microprocessor or microcontroller. The status register indicates the status of the WSM by signifying block erase or word program completion and status.

The Smart 3 Advanced Boot Block flash memory is also designed with an Automatic Power Savings (APS) feature which minimizes system current drain, allowing for very low power designs. This mode is entered following the completion of a read cycle (approximately 300 ns later).

The RP# pin provides additional protection against unwanted command writes that may occur during system reset and power-up/down sequences due to invalid system bus conditions (see Section 3.6).

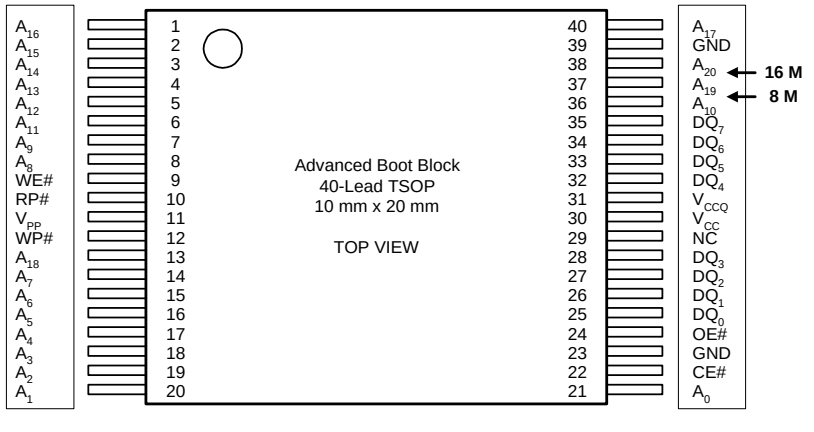
Section 3.0 gives detailed explanation of the different modes of operation. Complete current and voltage specifications can be found in the *DC Characteristics* section. Refer to *AC Characteristics* for read, program and erase performance specifications.

2.0 PRODUCT DESCRIPTION

This section explains device pin description and package pinouts.

2.1 Package Pinouts

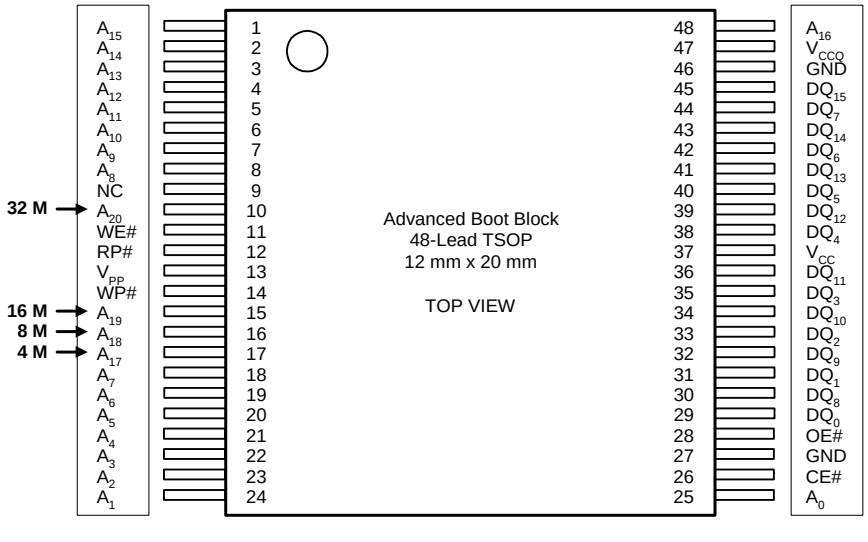
The Smart 3 Advanced Boot Block flash memory is available in 40-lead TSOP (x8, Figure 1), 48-lead TSOP (x16, Figure 2) and 48-ball µBGA packages (x8 and x16, Figure 3 and Figure 4 respectively). In all figures, pin changes necessary for density upgrades have been circled.



NOTES:

1. 40-Lead TSOP available for 8- and 16-Mbit densities only.
2. Lower densities will have NC on the upper address pins. For example, an 8-Mbit device will have NC on Pin 38.

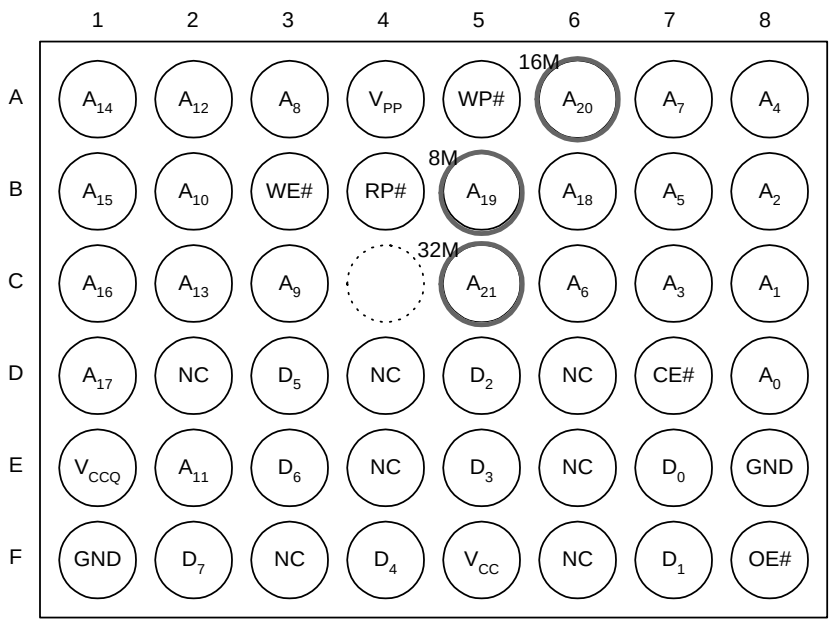
Figure 1. 40-Lead TSOP Package for x8 Configurations



NOTE:

Lower densities will have NC on the upper address pins. For example, an 8-Mbit device will have NC on Pins 9 and 15.

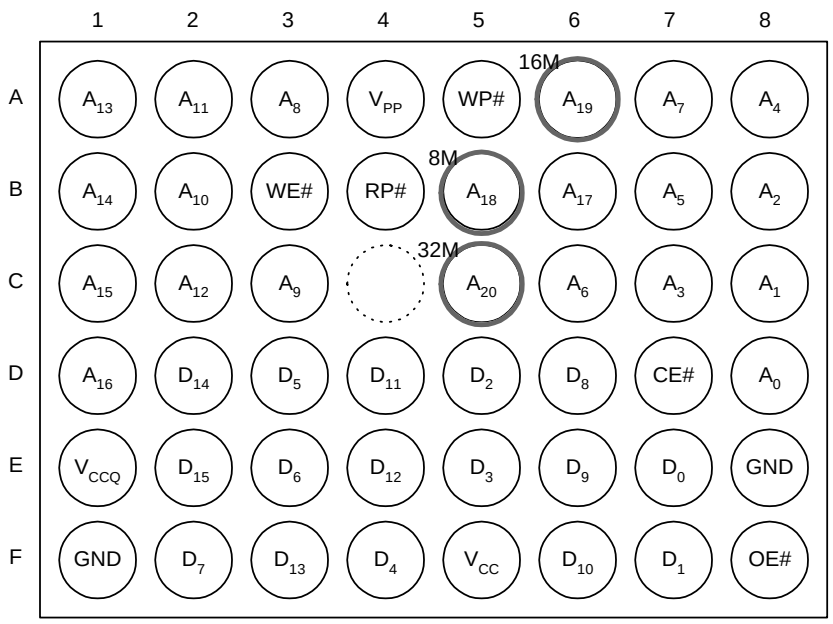
Figure 2. 48-Lead TSOP Package for x16 Configurations



NOTE:

1. Shaded connections indicate the upgrade address connections. Lower density devices will not have the upper address solder balls. Routing is not recommended in this area. A_{20} is the upgrade address for the 16-Mbit device. A_{21} is the upgrade address for the 32-Mbit device.
2. 4-Mbit density not available in µBGA* CSP.

Figure 3. x8 48-Ball µBGA* Chip Size Package (Top View, Ball Down)



NOTES:

1. Shaded connections indicate the upgrade address connections. Lower density devices will not have the upper address solder balls. Routing is not recommended in this area. A_{19} is the upgrade address for the 16-Mbit device. A_{20} is the upgrade address for the 32-Mbit device.
2. 4-Mbit density not available in µBGA* CSP.

Figure 4. x16 48-Ball µBGA* Chip Size Package (Top View, Ball Down)

The pin descriptions table details the usage of each device pin.

Table 2. Smart 3 Advanced Boot Block Pin Descriptions

Symbol	Type	Name and Function
A_0–A_{21}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a program or erase cycle. 28F008B3: A[0-19], 28F016B3: A[0-20], 28F032B3: A[0-21], 28F800B3: A[0-17], 28F800B3: A[0-18], 28F160B3: A[0-19], 28F320B3: A[0-20]
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched. Outputs array, identifier and status register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	INPUT/OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched. Outputs array and identifier data. The data pins float to tri-state when the chip is de-selected. **Not included on x8 products.**
CE#	INPUT	**CHIP ENABLE:** Activates the internal control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels.
OE#	INPUT	**OUTPUT ENABLE:** Enables the device's outputs through the data buffers during a read operation. OE# is active low.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the Command Register and memory array. WE# is active low. Addresses and data are latched on the rising edge of the second WE# pulse.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Uses two voltage levels (V_{IL}, V_{IH}) to control reset/deep power-down mode. **When RP# is at logic low, the device is in reset/deep power-down mode**, which drives the outputs to High-Z, resets the Write State Machine, and minimizes current levels (I_{CCD}). **When RP# is at logic high, the device is in standard operation**. When RP# transitions from logic-low to logic-high, the device resets all blocks to locked and defaults to the read array mode.
WP#	INPUT	**WRITE PROTECT:** Provides a method for locking and unlocking the two lockable parameter blocks. **When WP# is at logic low, the lockable blocks are locked**, preventing program and erase operations to those blocks. If a program or erase operation is attempted on a locked block, SR.1 and either SR.4 [program] or SR.5 [erase] will be set to indicate the operation failed. **When WP# is at logic high, the lockable blocks are unlocked** and can be programmed or erased. See Section 3.3 for details on write protection.

Table 2. Smart 3 Advanced Boot Block Pin Descriptions (Continued)

Symbol	Type	Name and Function
V_{CCQ}	INPUT	**OUTPUT V_{CC}:** Enables all outputs to be driven to 1.8 V – 2.5 V while the V_{CC} is at 2.7 V–3.3 V. If the V_{CC} is regulated to 2.7 V–2.85 V, V_{CCQ} can be driven at 1.65 V–2.5 V to achieve lowest power operation (see Section 4.4, *DC Characteristics*. This input may be tied directly to V_{CC} (2.7 V–3.6 V).
V_{CC}		**DEVICE POWER SUPPLY:** 2.7 V–3.6 V
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** Supplies power for program and erase operations. V_{PP} may be the same as V_{CC} (2.7 V–3.6 V) for single supply voltage operation. For fast programming at manufacturing, 11.4 V–12.6 V may be supplied to V_{PP}. This pin cannot be left floating. Applying 11.4 V–12.6 V to V_{PP} can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum (see Section 3.4 for details). $V_{PP} < V_{PPLK}$ protects memory contents against inadvertent or unintended program and erase commands.
GND		**GROUND:** For all internal circuitry. All ground inputs **must** be connected.
NC		**NO CONNECT:** Pin may be driven or left floating.

2.2 Block Organization

The Smart 3 Advanced Boot Block is an asymmetrically-blocked architecture that enables system integration of code and data within a single flash device. Each block can be erased independently of the others up to 100,000 times. For the address locations of each block, see the memory maps in Appendix D.

2.2.1 PARAMETER BLOCKS

The Smart 3 Advanced Boot Block flash memory architecture includes parameter blocks to facilitate storage of frequently updated small parameters (e.g., data that would normally be stored in an EEPROM). By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. Each device contains eight parameter blocks of 8-Kbytes/4-Kwords (8192 bytes/4,096 words) each.

2.2.2 MAIN BLOCKS

After the parameter blocks, the remainder of the array is divided into equal size main blocks (65,536 bytes / 32,768 words) for data or code storage. The 4-Mbit device contains seven main blocks; 8-Mbit device contains fifteen main blocks; 16-Mbit flash has thirty-one main blocks; 32-Mbit has sixty-three main blocks.

3.0 PRINCIPLES OF OPERATION

Flash memory combines EEPROM functionality with in-circuit electrical program and erase capability. The Smart 3 Advanced Boot Block flash memory family utilizes a Command User Interface (CUI) and automated algorithms to simplify program and erase operations. The CUI allows for 100% CMOS-level control inputs and fixed power supplies during erasure and programming.

When $V_{PP} < V_{PPLK}$, the device will only execute the following commands successfully: Read Array, Read Status Register, Clear Status Register and Read Identifier. The device provides standard EEPROM read, standby and output disable operations. Manufacturer identification and device identification data can be accessed through the CUI. All functions associated with altering memory contents, namely program and erase, are accessible via the CUI. The internal Write State Machine (WSM) completely automates program and erase operations while the CUI signals the start of an operation and the status register reports status. The CUI handles the WE# interface to the data and address latches, as well as system status requests during WSM operation.

3.1 Bus Operation

Smart 3 Advanced Boot Block flash memory devices read, program and erase in-system via the local CPU or microcontroller. All bus cycles to or from the flash memory conform to standard microcontroller bus cycles. Four control pins dictate the data flow in and out of the flash component: CE#, OE#, WE# and RP#. These bus operations are summarized in Table 3.

Table 3. Bus Operations(1)

Mode	Note	RP#	CE#	OE#	WE#	DQ_{0-7}	DQ_{8-15}
Read (Array, Status, or Identifier)	2–4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	D_{OUT}
Output Disable	2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Standby	2	V_{IH}	V_{IH}	X	X	High Z	High Z
Reset	2, 7	V_{IL}	X	X	X	High Z	High Z
Write	2, 5–7	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	D_{IN}

NOTES:

1. 8-bit devices use only DQ[0:7], 16-bit devices use DQ[0:15]
2. X must be V_{IL}, V_{IH} for control pins and addresses.
3. See *DC Characteristics* for V_{PPLK}, V_{PP1}, V_{PP2}, V_{PP3}, V_{PP4} voltages.
4. Manufacturer and device codes may also be accessed in read identifier mode (A_1–A_{21} = 0). See Table 4.
5. Refer to Table 6 for valid D_{IN} during a write operation.
6. To program or erase the lockable blocks, hold WP# at V_{IH}.
7. RP# must be at GND ± 0.2 V to meet the maximum deep power-down current specified.

3.1.1 READ

The flash memory has four read modes available: read array, read identifier, read status and read query. These modes are accessible independent of the V_{PP} voltage. The appropriate Read Mode command must be issued to the CUI to enter the corresponding mode. Upon initial device power-up or after exit from reset, the device automatically defaults to read array mode.

CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control; when active it enables the flash memory device. OE# is the data output control and it drives the selected memory data onto the I/O bus. For all read modes, WE# and RP# must be at V_{IH}. Figure 7 illustrates a read cycle.

3.1.2 OUTPUT DISABLE

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins are placed in a high-impedance state.

3.1.3 STANDBY

Deselecting the device by bringing CE# to a logic-high level (V_{IH}) places the device in standby mode, which substantially reduces device power consumption without any latency for subsequent read accesses. In standby, outputs are placed in a high-impedance state independent of OE#. If deselected during program or erase operation, the device continues to consume active power until the program or erase operation is complete.

3.1.4 DEEP POWER-DOWN / RESET

From read mode, RP# at V_{IL} for time t_{PLPH} deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. After return from reset, a time t_{PHQV} is required until the initial read access outputs are valid. A delay (t_{PHWL} or t_{PHEL}) is required after return from reset before a write can be initiated. After this wake-up interval, normal operation is restored. The CUI resets to read array mode, and the status register is set to 80H. This case is shown in Figure 9A.

If RP# is taken low for time t_{PLPH} during a program or erase operation, the operation will be aborted and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, since the data may be partially erased or written. The abort process goes through the following sequence: When RP# goes low, the device shuts down the operation in progress, a process which takes time t_{PLRH} to complete. After this time t_{PLRH}, the part will either reset to read array mode (if RP# has gone high during t_{PLRH}, Figure 9B) or enter reset mode (if RP# is still logic low after t_{PLRH}, Figure 9C). In both cases, after returning from an aborted operation, the relevant time t_{PHQV} or t_{PHWL}/t_{PHEL} must be waited before a read or write operation is initiated, as discussed in the previous paragraph. However, in this case, these delays are referenced to the end of t_{PLRH} rather than when RP# goes high.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, processor expects to read from the flash memory. Automated flash memories provide status information when read during program or block erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel's Flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.1.5 WRITE

A write takes place when both CE# and WE# are low and OE# is high. Commands are written to the Command User Interface (CUI) using standard microprocessor write timings to control flash operations. The CUI does not occupy an addressable memory location. The address and data buses are latched on the rising edge of the second WE# or CE# pulse, whichever occurs first. Figure 8 illustrates a program and erase operation. The available commands are shown in Table 6, and Appendix A provides detailed information on moving between the different modes of operation using CUI commands.

There are two commands that modify array data: Program (40H) and Erase (20H). Writing either of these commands to the internal Command User Interface (CUI) initiates a sequence of internally-timed functions that culminate in the completion of the requested task (unless that operation is aborted by either RP# being driven to V_{IL} for t_{PLRH} or an appropriate suspend command).

3.2 Modes of Operation

The flash memory has four read modes and two write modes. The read modes are read array, read identifier, read status and read query (see Appendix C). The write modes are program and block erase. Three additional modes (erase suspend to program, erase suspend to read and program suspend to read) are available only during suspended operations. These modes are reached using the commands summarized in Table 4. A comprehensive chart showing the state transitions is in Appendix A.

3.2.1 READ ARRAY

When RP# transitions from V_{IL} (reset) to V_{IH}, the device defaults to read array mode and will respond to the read control inputs (CE#, address inputs, and OE#) without any additional CUI commands.

When the device is in read array mode, four control signals control data output:

- WE# must be logic high (V_{IH})
- CE# must be logic low (V_{IL})
- OE# must be logic low (V_{IL})
- RP# must be logic high (V_{IH})

In addition, the address of the desired location must be applied to the address pins. If the device is not in read array mode, as would be the case after a program or erase operation, the Read Array command (FFH) must be written to the CUI before array reads can take place.

Table 4. Command Codes and Descriptions

Code	Device Mode	Description
00, 01, 60, 2F, C0, 98	Invalid/ Reserved	Unassigned commands that should not be used. Intel reserves the right to redefine these codes for future functions.
FF	Read Array	Places the device in read array mode, such that array data will be output on the data pins.
40	Program Set-Up	This is a two-cycle command. The first cycle prepares the CUI for a program operation. The second cycle latches addresses and data information and initiates the WSM to execute the Program algorithm. The flash outputs status register data when CE# or OE# is toggled. A Read Array command is required after programming to read array data. See Section 3.2.4.
10	Alternate Program Set-Up	(See 40H/Program Set-Up)
20	Erase Set-Up	Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will (a) set both SR.4 and SR.5 of the status register to a “1,” (b) place the device into the read status register mode, and (c) wait for another command. See Section 3.2.5.

Table 4. Command Codes and Descriptions (Continued)

Code	Device Mode	Description
D0	Erase Confirm	If the previous command was an Erase Set-Up command, then the CUI will close the address and data latches, and begin erasing the block indicated on the address pins. During erase, the device will only respond to the Read Status Register and Erase Suspend commands. The device will output status register data when CE# or OE# is toggled.
	Program / Erase Resume	If a program or erase operation was previously suspended, this command will resume that operation
B0	Program / Erase Suspend	Issuing this command will begin to suspend the currently executing program/erase operation. The status register will indicate when the operation has been successfully suspended by setting either the program suspend (SR.2) or erase suspend (SR.6) and the WSM status bit (SR.7) to a “1” (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input control pins except RP#, which will immediately shut down the WSM and the remainder of the chip if it is driven to V_{IL}. See Sections 3.2.4.1 and 3.2.5.1.
70	Read Status Register	This command places the device into read status register mode. Reading the device will output the contents of the status register, regardless of the address presented to the device. The device automatically enters this mode after a program or erase operation has been initiated. See Section 3.2.3.
50	Clear Status Register	The WSM can set the block lock status (SR.1) , V_{PP} status (SR.3), program status (SR.4), and erase status (SR.5) bits in the status register to “1,” but it cannot clear them to “0.” Issuing this command clears those bits to “0.”
90	Read Identifier	Puts the device into the intelligent identifier read mode, so that reading the device will output the manufacturer and device codes (A_0 = 0 for manufacturer, A_0 = 1 for device, all other address inputs must be 0). See Section 3.2.2.

NOTE: See Appendix A for mode transition information.

3.2.2 READ IDENTIFIER

To read the manufacturer and device codes, the device must be in read identifier mode, which can be reached by writing the Read Identifier command (90H). Once in read identifier mode, A_0 = 0 outputs the manufacturer’s identification code and A_0 = 1 outputs the device identifier (see Table 5) Note: A_1–A_{21} = 0. To return to read array mode, write the Read Array command (FFH).

Table 5. Read Identifier Table

Size	Mfr. ID	Device Identifier	
		-T (Top Boot)	-B (Bot. Boot)
28F400B3	0089H	8894H	8895H
28F008B3	0089H	D2	D3
28F800B3		8892H	8893H
28F016B3	0089H	D0	D1
28F160B3		8890H	8891H
28F032B3	0089H	D6	D7
28F320B3		8896	8897

3.2.3 READ STATUS REGISTER

The device status register indicates when a program or erase operation is complete and the success or failure of that operation. To read the status register issue the Read Status Register (70H) command to the CUI. This causes all subsequent read operations to output data from the status register until another command is written to the CUI. To return to reading from the array, issue the Read Array (FFH) command.

The status register bits are output on DQ_0–DQ_7. The upper byte, DQ_8–DQ_{15}, outputs 00H during a Read Status Register command.

The contents of the status register are latched on the falling edge of OE# or CE#. This prevents possible bus errors which might occur if status register contents change while being read. CE# or OE# must be toggled with each subsequent status read, or the status register will not indicate completion of a program or erase operation.

When the WSM is active, SR.7 will indicate the status of the WSM; the remaining bits in the status register indicate whether or not the WSM was successful in performing the desired operation (see Table 7).

3.2.3.1 Clearing the Status Register

The WSM sets status bits 1 through 7 to "1," and clears bits 2, 6 and 7 to "0," but cannot clear status bits 1 or 3 through 5 to "0." Because bits 1, 3, 4 and 5 indicate various error conditions, these bits can only be cleared through the Clear Status Register (50H) command. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several addresses or erasing multiple blocks in sequence) before reading the status register to determine if an error occurred during that series. Clear the status register before beginning another command or sequence. Note, again, that the Read Array command must be issued before data can be read from the memory array.

3.2.4 PROGRAM MODE

Programming is executed using a two-write sequence. The Program Setup command (40H) is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute a sequence of internally timed events to program desired bits of the addressed location, then Verify the bits are sufficiently programmed. Programming the memory results in specific bits within an address location being changed to a "0." If the user attempts to program "1"s, the memory cell contents do not change and no error occurs.

The status register indicates programming status: while the program sequence executes, status bit 7 is "0." The status register can be polled by toggling either CE# or OE#. While programming, the only valid commands are Read Status Register, Program Suspend, and Program Resume.

When programming is complete, the Program Status bits should be checked. If the programming operation was unsuccessful, bit SR.4 of the status register is set to indicate a program failure. If SR.3 is set then V_{PP} was not within acceptable limits, and the WSM did not execute the program command. If SR.1 is set, a program operation was attempted on a locked block and the operation was aborted.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, to prevent inadvertent status register reads, be sure to reset the CUI to read array mode.

3.2.4.1 Suspending and Resuming Program

The Program Suspend halts the in-progress program operation to read data from another location of memory. Once the programming process starts, writing the Program Suspend command to the CUI requests that the WSM suspend the program sequence (at predetermined points in the program algorithm). The device continues to output status register data after the Program Suspend command is written. Polling status register bits SR.7 and SR.2 will determine when the program operation has been suspended (both will be set to "1"). t_{WHRH1}/t_{EHRH1} specify the program suspend latency.

A Read Array command can now be written to the CUI to read data from blocks other than that which is suspended. The only other valid commands while program is suspended, are Read Status Register, Read Identifier, and Program Resume. After the Program Resume command is written to the flash memory, the WSM will continue with the program process and status register bits SR.2 and SR.7 will automatically be cleared. After the Program Resume command is written, the device automatically outputs status register data when read (see Appendix F for *Program Suspend and Resume Flowchart*). V_{PP} must remain at the same V_{PP} level used for program while in program suspend mode. RP# must also remain at $V_{IH.}$

3.2.5 ERASE MODE

To erase a block, write the Erase Set-up and Erase Confirm commands to the CUI, along with an address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1." Only one block can be erased at a time. The WSM will execute a sequence of internally-timed events to program all bits within the block to "0," erase all bits within the block to "1," then verify that all bits within the block are sufficiently erased. While the erase executes, status bit 7 is a "0."

When the status register indicates that erasure is complete, check the erase status bit to verify that the erase operation was successful. If the erase operation was unsuccessful, SR.5 of the status register will be set to a "1," indicating an erase failure. If V_{PP} was not within acceptable limits after the Erase Confirm command was issued, the WSM will not execute the erase sequence; instead, SR.5 of the status register is set to indicate an erase error, and SR.3 is set to a "1" to identify that V_{PP} supply voltage was not within acceptable limits.

After an erase operation, clear the status register (50H) before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, to prevent inadvertent status register reads, it is advisable to place the flash in read array mode after the erase is complete.

3.2.5.1 Suspending and Resuming Erase

Since an erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from or program data to another block in memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The status register will indicate if/when the erase operation has been suspended.

A Read Array/Program command can now be written to the CUI in order to read data from/ program data to blocks other than the one currently suspended. The Program command can subsequently be suspended to read yet another array location. The only valid commands while erase is suspended are Erase Resume, Program, Read Array, Read Status Register, or Read Identifier. During erase suspend mode, the chip can be placed in a pseudo-standby mode by taking CE# to V_{IH}. This reduces active current consumption.

Erase Resume continues the erase sequence when CE# = V_{IL}. As with the end of a standard erase operation, the status register must be read and cleared before the next instruction is issued.

Table 6. Command Bus Definitions(1, 4)

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH			
Read Identifier	2	Write	X	90H	Read	IA	ID
Read Status Register		Write	X	70H	Read	X	SRD
Clear Status Register		Write	X	50H			
Program	3	Write	X	40H / 10H	Write	PA	PD
Block Erase/Confirm		Write	X	20H	Write	BA	D0H
Program/Erase Suspend		Write	X	B0H			
Program/Erase Resume		Write	X	D0H			

NOTES: **PA:** Program Address **PD:** Program Data **BA:** Block Address
IA: Identifier Address **ID:** Identifier Data **SRD:** Status Register Data

1. Bus operations are defined in Table 3.
2. Following the Intelligent Identifier command, two read operations access manufacturer and device codes. $A_0 = 0$ for manufacturer code, $A_0 = 1$ for device code. A_1—$A_{21} = 0$.
3. Either 40H or 10H command is valid although the standard is 40H.
4. When writing commands to the device, the upper data bus [DQ_8–DQ_{15}] should be either V_{IL} or V_{IH}, to minimize current draw.

Table 7. Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check Write State Machine bit first to determine word program or block erase completion, before checking program or erase status bits.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed	When erase suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set at "1" until an Erase Resume command is issued.
SR.5 = ERASE STATUS (ES) 1 = Error In Block Erasure 0 = Successful Block Erase	When this bit is set to "1," WSM has applied the max. number of erase pulses to the block and is still unable to verify successful block erasure.
SR.4 = PROGRAM STATUS (PS) 1 = Error in Word Program 0 = Successful Word Program	When this bit is set to "1," WSM has attempted but failed to program a word.
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	The V_{PP} status bit does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Program or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. The V_{PP} is also checked before the operation is verified by the WSM. The V_{PP} status bit is not guaranteed to report accurate feedback between V_{PPLK} max and V_{PP1} min or between V_{PP1} max and V_{PP4} min.
SR.2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	When program suspend is issued, WSM halts execution and sets both WSMS and PSS bits to "1." PSS bit remains set to "1" until a Program Resume command is issued.
SR.1 = Block Lock Status 1 = Program/Erase attempted on locked block; Operation aborted 0 = No operation to locked blocks	If a program or erase operation is attempted to one of the locked blocks, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	This bit is reserved for future use and should be masked out when polling the status register.

3.3 Block Locking

The Smart 3 Advanced Boot Block flash memory architecture features two hardware-lockable parameter blocks.

3.3.1 WP# = V_{IL} FOR BLOCK LOCKING

The lockable blocks are locked when WP# = V_{IL}; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two parameter blocks (blocks #69 and #70, blocks #37 and #38 for the 16-Mbit, blocks #21 and #22 for the 8-Mbit, blocks #13 and #14 for the 4-Mbit) are lockable. For the bottom configuration, the bottom two parameter blocks (blocks #0 and #1 for 4-/8-/16-/32-Mbit) are lockable. Unlocked blocks can be programmed or erased normally (unless V_{PP} is below V_{PPLK}).

3.3.2 WP# = V_{IH} FOR BLOCK UNLOCKING

WP# = V_{IH} unlocks all lockable blocks.

These blocks can now be programmed or erased.

Note that RP# does not override WP# locking as in previous Boot Block devices. WP# controls all block locking and V_{PP} provides protection against spurious writes. Table 8 defines the write protection methods.

Table 8. Write Protection Truth Table for Advanced Boot Block Flash Memory Family

V_{PP}	WP#	RP#	Write Protection Provided
X	X	V_{IL}	All Blocks Locked
V_{IL}	X	V_{IH}	All Blocks Locked
≥ V_{PPLK}	V_{IL}	V_{IH}	Lockable Blocks Locked
≥ V_{PPLK}	V_{IH}	V_{IH}	All Blocks Unlocked

3.4 V_{PP} Program and Erase Voltages

Intel's Smart 3 products provide in-system programming and erase at 2.7 V. For customers requiring fast programming in their manufacturing environment, Smart 3 includes an additional low-cost 12 V programming feature.

The 12 V V_{PP} mode enhances programming performance during the short period of time typically found in manufacturing processes; however, it is not intended for extended use. 12 V may be applied to V_{PP} during program and erase operations for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum. Stressing the device beyond these limits may cause permanent damage.

During read operations or idle times, V_{PP} may be tied to a 5 V supply. For program and erase operations, a 5 V supply is not permitted. The V_{PP} must be supplied with either 2.7 V–3.6 V or 11.4 V–12.6 V during program and erase operations.

3.4.1 V_{PP} = V_{IL} FOR COMPLETE PROTECTION

The V_{PP} programming voltage can be held low for complete write protection of all blocks in the flash device. When V_{PP} is below V_{PPLK}, any program or erase operation will result in a error, prompting the corresponding status register bit (SR.3) to be set.

3.5 Power Consumption

Intel® Flash devices have a tiered approach to power savings that can significantly reduce overall system power consumption. The Automatic Power Savings (APS) feature reduces power consumption when the device is selected but idle. If the CE# is deasserted, the flash enters its standby mode, where current consumption is even lower. The combination of these features can minimize memory power consumption, and therefore, overall system power consumption.

3.5.1 ACTIVE POWER

With CE# at a logic-low level and RP# at a logic-high level, the device is in the active mode. Refer to the DC Characteristic tables for I_{CC} current values. Active power is the largest contributor to overall system power consumption. Minimizing the active current could have a profound effect on system power consumption, especially for battery-operated devices.

3.5.2 AUTOMATIC POWER SAVINGS (APS)

Automatic Power Savings provides low-power operation during read mode. After data is read from the memory array and the address lines are quiescent, APS circuitry places the device in a mode where typical current is comparable to I_{CCS}., The flash stays in this static state with outputs valid until a new location is read.

3.5.3 STANDBY POWER

With CE# at a logic-high level (V_{IH}) and device in read mode, the flash memory is in standby mode, which disables much of the device's circuitry and substantially reduces power consumption. Outputs are placed in a high-impedance state independent of the status of the OE# signal. If CE# transitions to a logic-high level during erase or program operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

System engineers should analyze the breakdown of standby time versus active time and quantify the respective power consumption in each mode for their specific application. This will provide a more accurate measure of application-specific power and energy requirements.

3.5.4 DEEP POWER-DOWN MODE

The deep power-down mode is activated when RP# = V_{IL} (GND $\pm$ 0.2 V). During read modes, RP# going low de-selects the memory and places the outputs in a high impedance state. Recovery from deep power-down requires a minimum time of t_{PHQV} (see *AC Characteristics—Read Operations*).

During program or erase modes, RP# transitioning low will abort the in-progress operation. The memory contents of the address being programmed or the block being erased are no longer valid as the data integrity has been compromised by the abort. During deep power-down, all internal circuits are switched to a low power savings mode (RP# transitioning to V_{IL} or turning off power to the device clears the status register).

3.6 Power-Up/Down Operation

The device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required, since the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers-up first.

3.6.1 RP# CONNECTED TO SYSTEM RESET

The use of RP# during system reset is important with automated program/erase devices since the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization will not occur because the flash memory may be providing status information instead of array data. Intel recommends connecting RP# to the system CPU RESET# signal to allow proper CPU/flash initialization following system reset.

System designers must guard against spurious writes when V_{CC} voltages are above V_{LKO}. Since both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until RP# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset (RP# connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

3.6.2 V_{CC}, V_{PP} AND RP# TRANSITIONS

The CUI latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its default state upon power-up, after exit from reset mode or after V_{CC} transitions above V_{LKO} (Lockout voltage), is read array mode.

After any program or block erase operation is complete (even after V_{PP} transitions down to V_{PPLK}), the CUI must be reset to read array mode via the Read Array command if access to the flash memory array is desired.

3.7 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling. System designers should consider three supply current issues:

1. Standby current levels (I_{CCS})
2. Read current levels (I_{CCR})
3. Transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

4.0 ELECTRICAL SPECIFICATIONS

NOTICE: This datasheet contains preliminary information on new products in production. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

4.1 Absolute Maximum Ratings*

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

Extended Operating Temperature

- During Read ..... –40 °C to +85 °C
- During Block Erase and Program..... –40 °C to +85 °C
- Temperature Under Bias ..... –40 °C to +85 °C

Storage Temperature..... –65 °C to +125 °C

Voltage on Any Pin (except V_{CC}, V_{CCQ} and V_{PP}) with Respect to GND ..... –0.5 V to 3.7 V(1)

V_{PP} Voltage (for Block Erase and Program) with Respect to GND .....–0.5 V to +13.5 V(1,2,4)

V_{CC} and V_{CCQ} Supply Voltage with Respect to GND ..... –0.2 V to +3.7 V(5)

Output Short Circuit Current.....100 mA(3)

NOTES:

1. Minimum DC voltage is –0.5 V on input/output pins, with allowable undershoot to –2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5 V, with allowable overshoot to V_{CC} + 1.5 V for periods < 20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0 V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. V_{PP} Program voltage is normally 2.7 V–3.6 V.
5. Minimum DC voltage is –0.5 V on V_{CC} and V_{CCQ}, with allowable undershoot to –2.0 V for periods < 20 ns. Maximum DC voltage on V_{CC} and V_{CCQ} pins is V_{CC} + 0.5 V, with allowable overshoot to V_{CC} + 1.5 V for periods < 20 ns.

4.2 Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		–40	+85	°C
V_{CC1}	V_{CC} Supply Voltage	1	2.7	3.6	Volts
V_{CC2}			2.7	2.85	
V_{CC3}			2.7	3.3	
V_{CCQ1}	I/O Supply Voltage	1	2.7	3.6	Volts
V_{CCQ2}			1.65	2.5	
V_{CCQ3}			1.8	2.5	
V_{PP1}	Program and Erase Voltage	1	2.7	3.6	Volts
V_{PP2}			2.7	2.85	
V_{PP3}			2.7	3.3	
V_{PP4}		2, 3	11.4	12.6	
Cycling	Block Erase Cycling	3	100,000		Cycles

NOTES:

1. V_{CC1}, V_{CCQ1}, and V_{PP3} must share the same supply when all three are between 2.7 V and 3.6 V.
2. During read operations or idle time, 5 V may be applied to V_{PP} indefinitely. V_{PP} must be at valid levels for program and erase operations
3. Applying V_{PP} = 11.4 V–12.6 V during a program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum. See Section 3.4 for details.

4.3 Capacitance

T_A = 25 °C, f = 1 MHz

Sym	Parameter	Notes	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	1	6	8	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	1	10	12	pF	V_{OUT} = 0 V

NOTE:

1. Sampled, not 100% tested.

4.4 DC Characteristics(1)

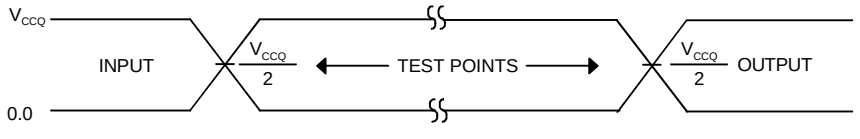
Sym	Parameter	Note	V_{CC} / V_{CCQ}	2.7 V–3.6 V / 2.7 V–3.6 V Typ	2.7 V–3.6 V / 2.7 V–3.6 V Max	2.7 V–2.85 V / 1.65 V–2.5 V Typ	2.7 V–2.85 V / 1.65 V–2.5 V Max	2.7 V–3.3 V / 1.8 V–2.5 V Typ	2.7 V–3.3 V / 1.8 V–2.5 V Max	Unit	Test Conditions
I_{LI}	Input Load Current	6			± 1		± 1		± 1	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max $V_{IN} = V_{CCQ}$ or GND
I_{LO}	Output Leakage Current	6			± 10		± 10		± 10	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max $V_{IN} = V_{CCQ}$ or GND
I_{CCS}	V_{CC} Standby Current	6	18	35	20	50	150	250	µA	$V_{CC} = V_{CC}$Max CE# = RP# = V_{CC} or during Program/ Erase Suspend
I_{CCD}	V_{CC} Power-Down Current	6	7	20	7	20	7	20	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max $V_{IN} = V_{CCQ}$ or GND RP# = GND ± 0.2 V
I_{CCR}	V_{CC} Read Current	4,6	10	18	8	15	9	15	mA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max OE# = V_{IH}, CE# =V_{IL} f = 5 MHz, I_{OUT}=0mA Inputs = V_{IL} or V_{IH}
I_{PPD}	V_{PP} Deep Power-Down Current		0.2	5	0.2	5	0.2	5	µA	RP# = GND ± 0.2 V $V_{PP} \le V_{CC}$
I_{PPR}	V_{PP} Read Current		2	±15	2	±15	2	±15	µA	$V_{PP} \le V_{CC}$
		3	50	200	50	200	50	200	µA	$V_{PP} > V_{CC}$
I_{CCW+} I_{PPW}	V_{CC} + V_{PP} Program Current	3,6	18	55	18	55	18	55	mA	$V_{PP} = V_{PP1, 2, 3}$ Program in Progress
			10	30	10	30	10	30	mA	$V_{PP} = V_{PP4}$ Program in Progress
I_{CCE} + I_{PPE}	V_{CC} + V_{PP} Erase Current	3,6	20	45	21	45	21	45	mA	$V_{PP} = V_{PP1, 2, 3}$ Program in Progress
			16	45	16	45	16	45	mA	$V_{PP} = V_{PP4}$ Program in Progress
I_{PPES} I_{PPWS}	V_{PP} Erase Suspend Current	3	50	200	50	200	50	200	µA	$V_{PP} = V_{PP1, 2, 3, 4}$ Program or Erase Suspend in Progress

4.4 DC Characteristics (Continued)

Sym	Parameter	Note	V_{CC} 2.7 V–3.6 V / V_{CCQ} 2.7 V–3.6 V Min	Max	V_{CC} 2.7 V–2.85 V / V_{CCQ} 1.65 V–2.5 V Min	Max	V_{CC} 2.7 V–3.3 V / V_{CCQ} 1.8 V–2.5 V Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage		–0.4	0.4	–0.2	0.2	–0.2	0.2	V	
V_{IH}	Input High Voltage		V_{CCQ} –0.4V		V_{CCQ} –0.2V		V_{CCQ} –0.2V		V	
V_{OL}	Output Low Voltage			0.10	-0.10	0.10	-0.10	0.10	V	$V_{CC} = V_{CC}Min$ $V_{CCQ} = V_{CCQ}Min$ I_{OL} = 100 µA
V_{OH}	Output High Voltage		V_{CCQ} –0.1V		V_{CCQ} –0.1V		V_{CCQ} –0.1V		V	$V_{CC} = V_{CC}Min$ $V_{CCQ} = V_{CCQ}Min$ I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	2		1.5		1.5		1.5	V	Complete Write Protection
V_{PP1}	V_{PP} during Program and Erase Operations	2	2.7	3.6					V	
V_{PP2}		2			2.7	2.85			V	
V_{PP3}		2					2.7	3.3	V	
V_{PP4}		2,5	11.4	12.6	11.4	12.6	11.4	12.6	V	
V_{LKO}	V_{CC} Prog/Erase Lock Voltage		1.5		1.5		1.5		V	
V_{LKO2}	V_{CCQ} Prog/Erase Lock Voltage		1.2		1.2		1.2		V	

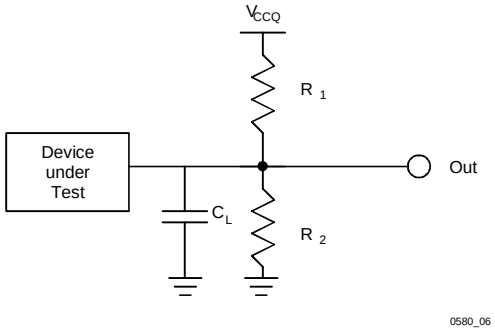
NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC}, T_A = +25 °C.
2. Erase and program are inhibited when $V_{PP} < V_{PPLK}$ and not guaranteed outside the valid V_{PP} ranges of V_{PP1}, V_{PP2}, V_{PP3} and V_{PP4}. For read operations or during idle time, a 5 V supply may be applied to V_{PP} indefinitely. However, V_{PP} must be at valid levels for program and erase operations.
3. Sampled, not 100% tested.
4. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation.
5. Applying V_{PP} = 11.4 V–12.6 V during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum. See Section 3.4 for details. For read operations or during idle time, a 5 V supply may be applied to V_{PP} indefinitely. However, V_{PP} must be at valid levels for program and erase operations.
6. Since each column lists specifications for a different V_{CC} and V_{CCQ} voltage range combination, the test conditions V_{CC}Max, V_{CCQ}Max, V_{CC}Min, and V_{CCQ}Min refer to the maximum or minimum V_{CC} or V_{CCQ} voltage listed at the top of each column.



NOTE:
AC test inputs are driven at V_{CCQ} for a logic "1" and 0.0V for a logic "0." Input timing begins, and output timing ends, at $V_{CCQ}/2$. Input rise and fall times (10%–90%) <10 ns. Worst case speed conditions are when $V_{CCQ} = V_{CCQ}$Min.

Figure 5. Input Range and Measurement Points



NOTE:
See table for component values.

Figure 6. Test Configuration

Test Configuration Component Values for Worst Case Speed Conditions

Test Configuration	C_L (pF)	R_1 (Ω)	R_2 (Ω)
V_{CCQ1} Standard Test	50	25 K	25 K
V_{CCQ2} Standard Test	50	16.7 K	16.7 K

NOTE:
C_L includes jig capacitance.

4.5 AC Characteristics —Read Operations[1]

		Product	3.0 V–3.6 V	80 ns				100 ns				
			2.7 V–3.6 V			90 ns				110 ns		
#	Sym	Parameter	Note	Min	Max	Min	Max	Min	Max	Min	Max	Unit
R1	t_{AVAV}	Read Cycle Time		80		90		100		110		ns
R2	t_{AVQV}	Address to Output Delay			80		90		100		110	ns
R3	t_{ELQV}	CE# to Output Delay	2		80		90		100		110	ns
R4	t_{GLQV}	OE# to Output Delay	2		30		30		30		30	ns
R5	t_{PHQV}	RP# to Output Delay			600		600		600		600	ns
R6	t_{ELQX}	CE# to Output in Low Z	3	0		0		0		0		ns
R7	t_{GLQX}	OE# to Output in Low Z	3	0		0		0		0		ns
R8	t_{EHQZ}	CE# to Output in High Z	3		25		25		25		25	ns
R9	t_{GHQZ}	OE# to Output in High Z	3		25		25		25		25	ns
R10	t_{OH}	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	3	0		0		0		0		ns

NOTES:

1. See *AC Waveform: Read Operations*.
2. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, but not 100% tested.

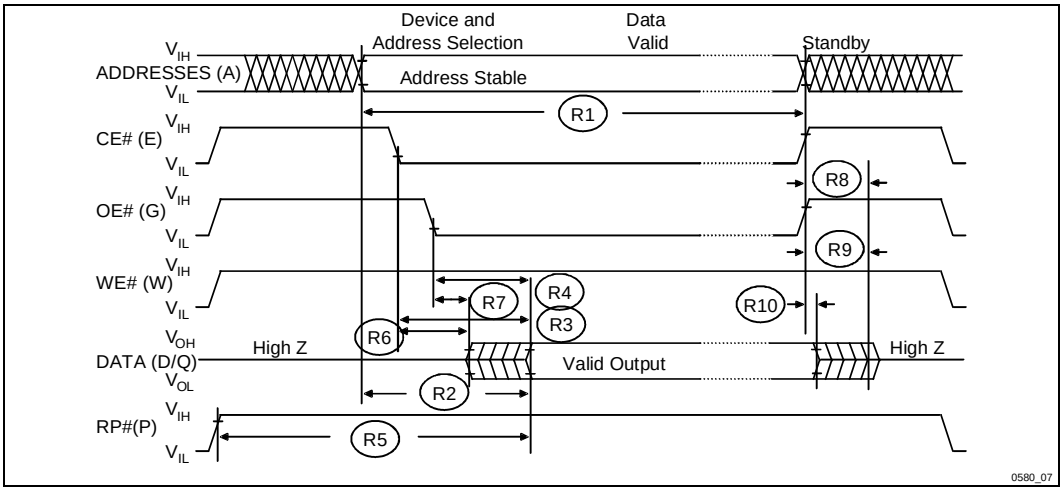


Figure 7. AC Waveform: Read Operations

4.6 AC Characteristics —Write Operations[1]

#	Symbol	Product / Parameter	Note	3.0 V – 3.6 V: 80 Min	2.7 V – 3.6 V: 90 Min	100 Min	110 Min	Unit
W1	t_{PHWL} / t_{PHEL}	RP# High Recovery to WE# (CE#) Going Low		600	600	600	600	ns
W2	t_{ELWL} / t_{WLEL}	CE# (WE#) Setup to WE# (CE#) Going Low		0	0	0	0	ns
W3	t_{ELEH} / t_{WLWH}	WE# (CE#) Pulse Width	4	70	70	70	70	ns
W4	t_{DVWH} / t_{DVEH}	Data Setup to WE# (CE#) Going High	2	50	50	60	60	ns
W5	t_{AVWH} / t_{AVEH}	Address Setup to WE# (CE#) Going High	2	70	70	70	70	ns
W6	t_{WHEH} / t_{EHWH}	CE# (WE#) Hold Time from WE# (CE#) High		0	0	0	0	ns
W7	t_{WHDX} / t_{EHDX}	Data Hold Time from WE# (CE#) High	2	0	0	0	0	ns
W8	t_{WHAX} / t_{EHAX}	Address Hold Time from WE# (CE#) High	2	0	0	0	0	ns
W9	t_{WHWL} / t_{EHEL}	WE# (CE#) Pulse Width High	4	30	30	30	30	ns
W10	t_{VPWH} / t_{VPEH}	V_{PP} Setup to WE# (CE#) Going High	3	200	200	200	200	ns
W11	t_{QVVL}	V_{PP} Hold from Valid SRD	3	0	0	0	0	ns

NOTES:

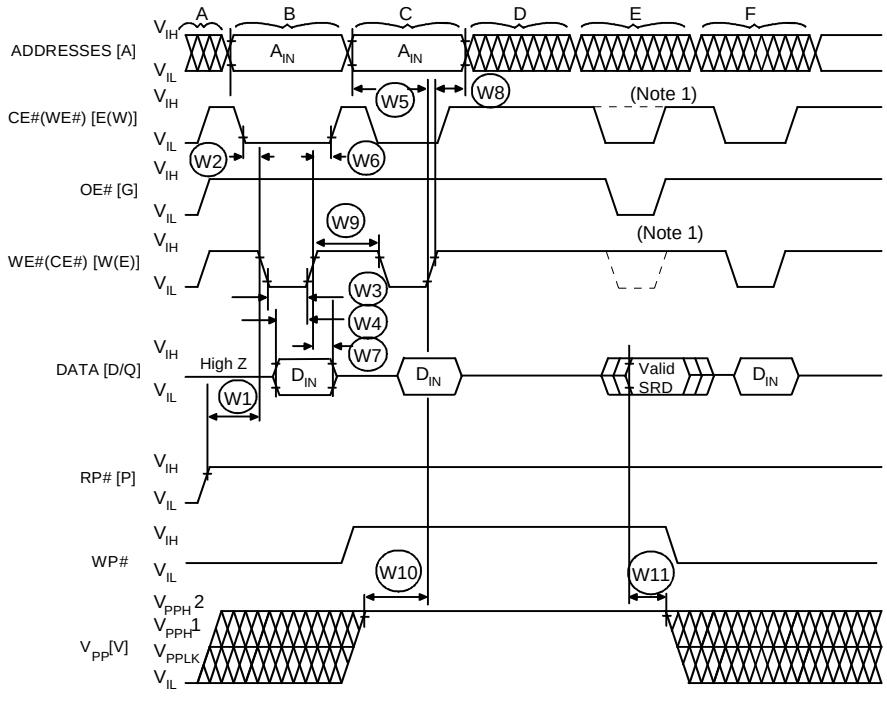
1. Read timing characteristics during program suspend and erase suspend are the same as during read-only operations.
2. Refer to command definition table (Table 6) for valid A_{IN} or D_{IN}.
3. Sampled, but not 100% tested.
4. Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, Write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low first). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.

4.7 Program and Erase Timings

Symbol	Parameter	V_{PP} Notes	2.7 V–3.6 V Typ(1)	2.7 V–3.6 V Max	11.4 V–12.6 V Typ(1)	11.4 V–12.6 V Max	Units
t_{BWPB}	8-KB Parameter Block Program Time (Byte)	2, 3	0.16	0.48	0.08	0.24	s
	4-KW Parameter Block Program Time (Word)	2, 3	0.10	0.30	0.03	0.12	s
t_{BWMB}	64-KB Main Block Program Time (Byte)	2, 3	1.2	3.7	0.6	1.7	s
	32-KW Main Block Program Time(Word)	2, 3	0.8	2.4	0.24	1	s
t_{WHQV1} / t_{EHQV1}	Byte Program Time	2, 3	17	165	8	185	µs
	Word Program Time	2, 3	22	200	8	185	µs
t_{WHQV2} / t_{EHQV2}	8-KB Parameter Block Erase Time (Byte)	2, 3	1	4	0.8	4	s
	4-KW Parameter Block Erase Time (Word)	2, 3	0.5	4	0.4	4	s
t_{WHQV3} / t_{EHQV3}	64-KB Main Block Erase Time (Byte)	2, 3	1	5	1	5	s
	32-KW Main Block Erase Time (Word)	2, 3	1	5	0.6	5	s
t_{WHRH1} / t_{EHRH1}	Program Suspend Latency		5	10	5	10	µs
t_{WHRH2} / t_{EHRH2}	Erase Suspend Latency		5	20	5	20	µs

NOTES:

1. Typical values measured at nominal voltages and T_A = +25 °C.
2. Excludes external system-level overhead.
3. Sampled, not 100% tested.



NOTES:

1. CE# must be toggled low when reading Status Register Data. WE# must be inactive (high) when reading Status Register Data.

A. V_{CC} Power-Up and Standby.

B. Write Program or Erase Setup Command.

C. Write Valid Address and Data (for Program) or Erase Confirm Command.

D. Automated Program or Erase Delay.

E. Read Status Register Data (SRD): reflects completed program/erase operation.

F. Write Read Array Command.

Figure 8. AC Waveform: Program and Erase Operations

5.0 RESET OPERATIONS

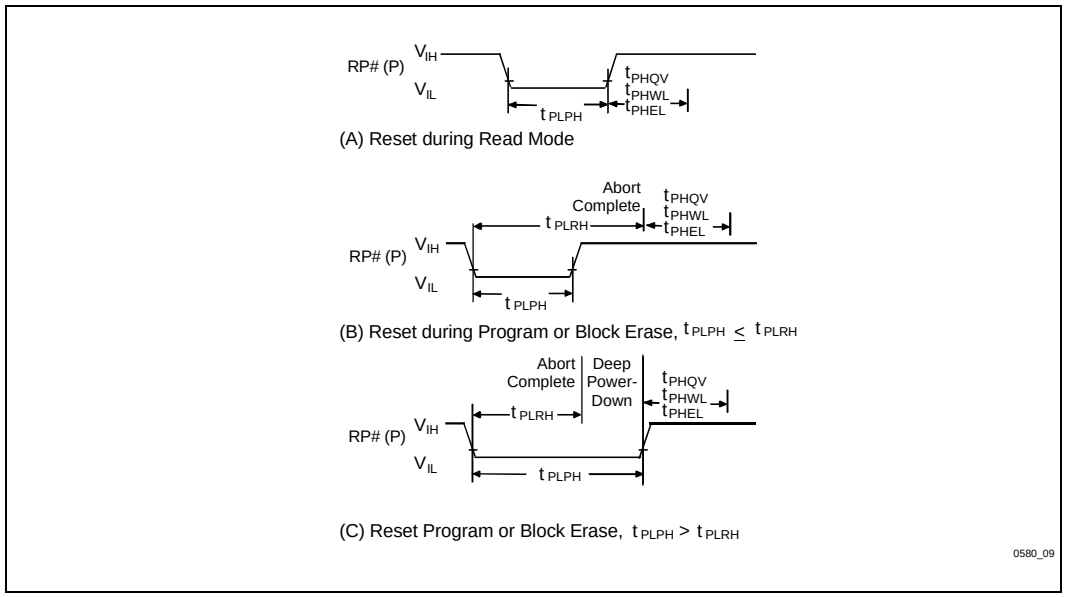


Figure 9. AC Waveform: Deep Power-Down/Reset Operation

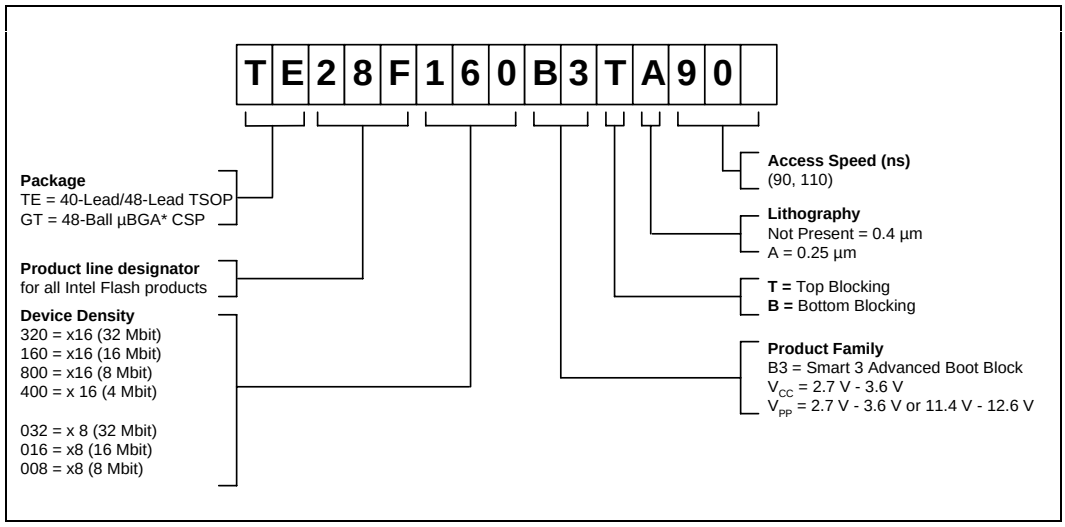
Reset Specifications

Symbol	Parameter	Notes	V_{CC} = 2.7 V–3.6 V		Unit
			Min	Max	
t_{PLPH}	RP# Low to Reset during Read (If RP# is tied to V_{CC}, this specification is not applicable)	1,3	100		ns
t_{PLRH}	RP# Low to Reset during Block Erase or Program	2,3		22	µs

NOTES:

1. If t_{PLPH} is <100 ns the device may still RESET but this is not guaranteed.
2. If RP# is asserted while a block erase or word program operation is not executing, the reset will complete within 100 ns.
3. Sampled, but not 100% tested.

6.0 ORDERING INFORMATION



Ordering Information Valid Combinations

	40-Lead TSOP	48-Ball µBGA* CSP(1)	48-Lead TSOP	48-Ball µBGA CSP
Ext. Temp.		GT28F032B3TA95	TE28F320B3TA95	GT28F320B3TA95
32 M		GT28F032B3BA95	TE28F320B3BA95	GT28F320B3BA95
		GT28F032B3TA115	TE28F320B3TA115	GT28F320B3TA115
		GT28F032B3BA115	TE28F320B3BA115	GT28F320B3BA115
Ext. Temp.	TE28F016B3TA90(2)	GT28F016B3TA90(2)	TE28F160B3TA90(2)	GT28F160B3TA90(2)
16 M	TE28F016B3BA90(2)	GT28F016B3BA90(2)	TE28F160B3BA90(2)	GT28F160B3BA90(2)
	TE28F016B3TA110(2)	GT28F016B3TA110(2)	TE28F160B3TA110(2)	GT28F160B3TA110(2)
	TE28F016B3BA110(2)	GT28F016B3BA110(2)	TE28F160B3BA110(2)	GT28F160B3BA110(2)
Ext. Temp.	TE28F008B3TA90(2)	GT28F008B3T90	TE28F800B3TA90(2)	GT28F800B3T90
8 M	TE28F008B3BA90(2)	GT28F008B3B90	TE28F800B3BA90(2)	GT28F800B3B90
	TE28F008B3TA110(2)	GT28F008B3T110	TE28F800B3TA110(2)	GT28F800B3T110
	TE28F008B3BA110(2)	GT28F008B3B110	TE28F800B3BA110(2)	GT28F800B3B110
Ext. Temp			TE28F400B3T110	
4 M			TE28F400B3B110	

NOTES:

1. The 48-ball µBGA package top side mark reads F160B3 [or F800B3]. This mark is identical for both x8 and x16 products. All product shipping boxes or trays provide the correct information regarding bus architecture. However, once the devices are removed from the shipping media, it may be difficult to differentiate based on the top side mark. The device identifier (accessible through the Device ID command: see Section 3.2.2 for further details) enables x8 and x16 µBGA package product differentiation.
2. The second line of the 48-ball µBGA package top side mark specifies assembly codes. For samples only, the first character signifies either "E" for engineering samples or "S" for silicon daisy chain samples. All other assembly codes without an "E" or "S" as the first character are production units.
3. Product can be ordered in either 0.25 µm or 0.4 µm material. The "A" before the access speed specifies 0.25 µm material.
4. For new designs, Intel recommends using 0.25 µm Advanced Boot Block devices.

7.0 ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
210830	*1997 Flash Memory Databook*
297948	*Smart 3 Advanced Boot Block Flash Memory Family Specification Update*
297835	*28F160B3 Specification Update*
	Smart 3 Advanced Boot Block Algorithms ('C' and assembly) http://developer.intel.com/design/flcomp
Contact your Intel Representative	*Flash Data Integrator (FDI) Software Developer's Kit*
297874	*FDI Interactive: Play with Intel's Flash Data Integrator on Your PC*

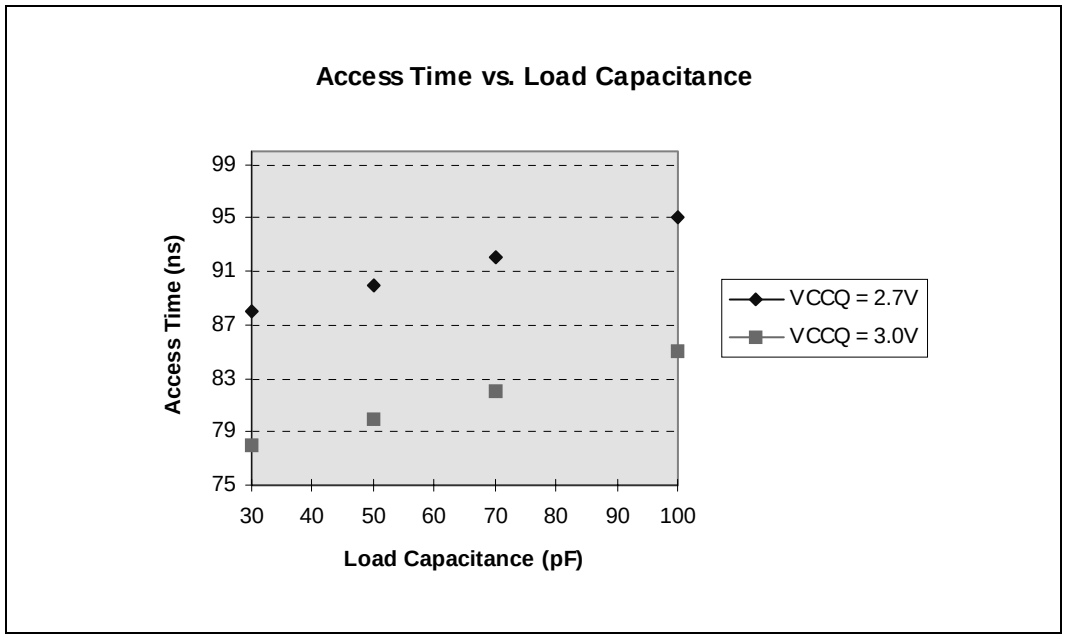
NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com or http://developer.intel.com for technical documentation and tools.

APPENDIX A
WRITE STATE MACHINE CURRENT/NEXT STATES

Current State	SR.7	Data When Read	Command Input (and Next State)								
			Read Array (FFH)	Program Setup (10/40H)	Erase Setup (20H)	Erase Confirm (D0H)	Prog/Ers Suspend (B0H)	Prog/Ers Resume (D0H)	Read Status (70H)	Clear Status (50H)	Read Identifier. (90H)
Read Array	"1"	Array	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Read Status	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Read Identifier	"1"	Identifier	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Prog. Setup	"1"	Status	Program (Command Input = Data to be Programmed)								
Program (continue)	"0"	Status	Program (continue)				Prog. Susp. to Rd. Status	Program (continue)			
Program Suspend to Read Status	"1"	Status	Prog. Sus. to Read Array	Program Suspend to Read Array		Program (continue)	Program Susp. to Read Array	Program (continue)	Prog. Susp. to Read Status	Prog. Sus. to Read Array	Prog. Susp. to Read Identifier
Program Suspend to Read Array	"1"	Array	Prog. Susp. to Read Array	Program Suspend to Read Array		Program (continue)	Program Susp. to Read Array	Program (continue)	Prog. Susp. to Read Status	Prog. Sus. to Read Array	Prog. Susp. to Read Identifier
Prog. Susp. to Read Identifier	"1"	Identifier	Prog. Susp. to Read Array	Program Suspend to Read Array		Program (continue)	Program Susp. to Read Array	Program (continue)	Prog. Susp. to Read Status	Prog. Sus. to Read Array	Prog. Susp. to Read Identifier
Program (complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase Setup	"1"	Status	Erase Command Error			Erase (continue)	Erase Cmd. Error	Erase (continue)	Erase Command Error		
Erase Cmd. Error	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase (continue)	"0"	Status	Erase (continue)				Erase Sus. to Read Status	Erase (continue)			
Erase Suspend to Status	"1"	Status	Erase Susp. to Read Array	Program Setup	Erase Susp. to Read Array	Erase	Erase Susp. to Read Array	Erase	Erase Susp. to Read Status	Erase Susp. to Read Array	Ers. Susp. to Read Identifier
Erase Susp. to Read Array	"1"	Array	Erase Susp. to Read Array	Program Setup	Erase Susp. to Read Array	Erase	Erase Susp. to Read Array	Erase	Erase Susp. to Read Status	Erase Susp. to Read Array	Ers. Susp. to Read Identifier
Erase Susp. to Read Identifier	"1"	Identifier	Erase Susp. to Read Array	Program Setup	Erase Susp. to Read Array	Erase	Erase Susp. to Read Array	Erase	Erase Susp. to Read Status	Erase Susp. to Read Array	Ers. Susp. to Read Identifier
Erase (complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier

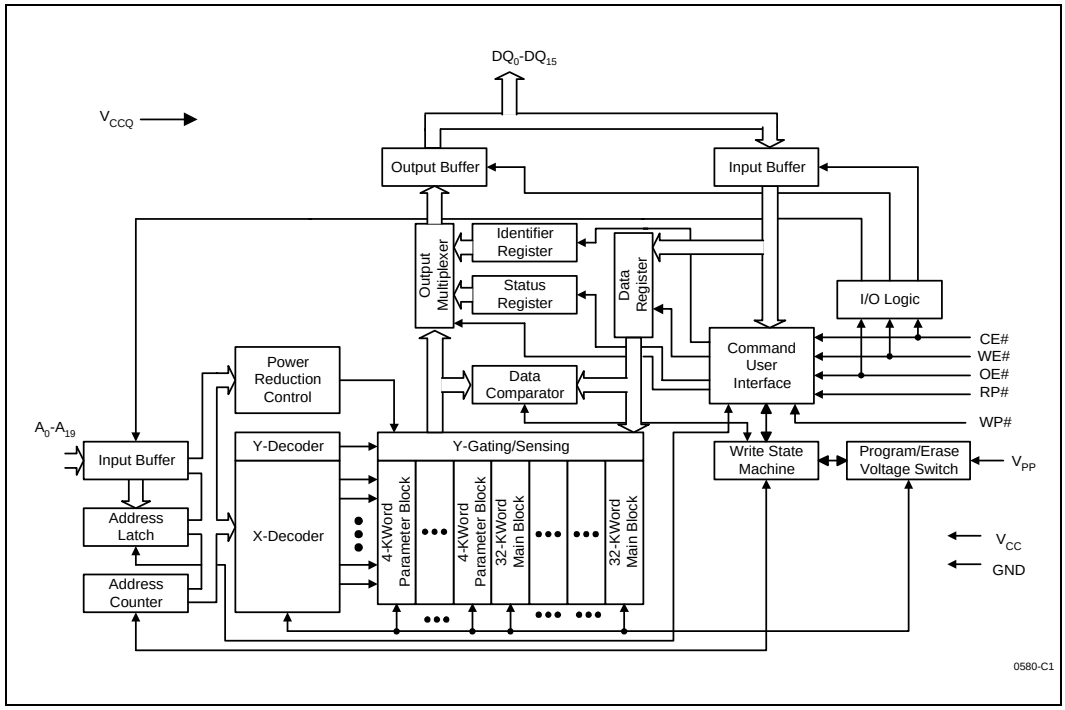
APPENDIX B
ACCESS TIME VS. CAPACITIVE LOAD (t_{AVQV} vs. C_L)



This chart shows a derating curve for device access time with respect to capacitive load. The value in the *DC Characteristics* section of the specification corresponds to C_L = 50 pF.

NOTE:
Sampled, but not 100% tested

APPENDIX C
ARCHITECTURE BLOCK DIAGRAM



APPENDIX D
WORD-WIDE MEMORY MAP DIAGRAMS

8-Mbit, 16-Mbit, and 32-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)	**8M**	**16M**	**32M**	**Size (KW)**	**8M**	**16M**	**32M**
4	7F000-7FFFF	FF000-FFFFF	1FF000-1FFFFF	32			1F8000-1FFFFF
4	7E000-7EFFF	FE000-FEFFF	1FE000-1FEFFF	32			1F0000-1F7FFF
4	7D000-7DFFF	FD000-FDFFF	1FD000-1FDFFF	32			1E8000-1EFFFF
4	7C000-7CFFF	FC000-FCFFF	1FC000-1FCFFF	32			1E0000-1E7FFF
4	7B000-7BFFF	FB000-FBFFF	1FB000-1FBFFF	32			1D8000-1DFFFF
4	7A000-7AFFF	FA000-FAFFF	1FA000-1FAFFF	32			1D0000-1D7FFF
4	79000-79FFF	F9000-F9FFF	1F9000-1F9FFF	32			1C8000-1CFFFF
4	78000-78FFF	F8000-F8FFF	1F8000-1F8FFF	32			1C0000-1C7FFF
32	70000-77FFF	F0000-F7FFF	1F0000-1F7FFF	32			1B8000-1BFFFF
32	68000-6FFFF	E8000-EFFFF	1E8000-1EFFFF	32			1B0000-1B7FFF
32	60000-67FFF	E0000-E7FFF	1E0000-1E7FFF	32			1A8000-1AFFFF
32	58000-5FFFF	D8000-DFFFF	1D8000-1DFFFF	32			1A0000-1A7FFF
32	50000-57FFF	D0000-D7FFF	1D0000-1D7FFF	32			198000-19FFFF
32	48000-4FFFF	C8000-CFFFF	1C8000-1CFFFF	32			190000-197FFF
32	40000-47FFF	C0000-C7FFF	1C0000-1C7FFF	32			188000-18FFFF
32	38000-3FFFF	B8000-BFFFF	1B8000-1BFFFF	32			180000-187FFF
32	30000-37FFF	B0000-B7FFF	1B0000-1B7FFF	32			178000-17FFFF
32	28000-2FFFF	A8000-AFFFF	1A8000-1AFFFF	32			170000-177FFF
32	20000-27FFF	A0000-A7FFF	1A0000-1A7FFF	32			168000-16FFFF
32	18000-1FFFF	98000-9FFFF	198000-19FFFF	32			160000-167FFF
32	10000-17FFF	90000-97FFF	190000-197FFF	32			158000-15FFFF
32	08000-0FFFF	88000-8FFFF	188000-18FFFF	32			150000-157FFF
32	00000-07FFF	80000-87FFF	180000-187FFF	32			148000-14FFFF
32		78000-7FFFF	178000-17FFFF	32			140000-147FFF
32		70000-77FFF	170000-177FFF	32			138000-13FFFF
32		68000-6FFFF	168000-16FFFF	32			130000-137FFF
32		60000-67FFF	160000-167FFF	32			128000-12FFFF
32		58000-5FFFF	158000-15FFFF	32			120000-127FFF
32		50000-57FFF	150000-157FFF	32			118000-11FFFF
32		48000-4FFFF	148000-14FFFF	32			110000-117FFF
32		40000-47FFF	140000-147FFF	32			108000-10FFFF
32		38000-3FFFF	138000-13FFFF	32			100000-107FFF
32		30000-37FFF	130000-137FFF	32		F8000-FFFFF	0F8000-0FFFFF
32		28000-2FFFF	128000-12FFFF	32		F0000-F7FFF	0F0000-0F7FFF
32		20000-27FFF	120000-127FFF	32		E8000-EFFFF	0E8000-0EFFFF
32		18000-1FFFF	118000-11FFFF	32		E0000-E7FFF	0E0000-0E7FFF
32		10000-17FFF	110000-117FFF	32		D8000-DFFFF	0D8000-0DFFFF
32		08000-0FFFF	108000-10FFFF	32		D0000-D7FFF	0D0000-0D7FFF
32		00000-07FFF	100000-107FFF	32		C8000-CFFFF	0C8000-0CFFFF
This column continues on next page				This column continues on next page			

8-Mbit, 16-Mbit, and 32-Mbit Word-Wide Memory Addressing (Continued)

Top Boot				Bottom Boot			
Size (KW)	**8M**	**16M**	**32M**	**Size (KW)**	**8M**	**16M**	**32M**
32			0F8000-0FFFFF	32		C0000-C7FFF	0C0000-0C7FFF
32			0F0000-0F7FFF	32		B8000-BFFFF	0B8000-0BFFFF
32			0E8000-0EFFFF	32		B0000-B7FFF	0B0000-0B7FFF
32			0E0000-0E7FFF	32		A8000-AFFFF	0A8000-0AFFFF
32			0D8000-0DFFFF	32		A0000-A7FFF	0A0000-0A7FFF
32			0D0000-0D7FFF	32		98000-9FFFF	098000-09FFFF
32			0C8000-0CFFFF	32		90000-97FFF	090000-097FFF
32			0C0000-0C7FFF	32		88000-8FFFF	088000-08FFFF
32			0B8000-0BFFFF	32		80000-87FFF	080000-087FFF
32			0B0000-0B7FFF	32	78000-7FFFF	78000-7FFFF	78000-7FFFF
32			0A8000-0AFFFF	32	70000-77FFF	70000-77FFF	70000-77FFF
32			0A0000-0A7FFF	32	68000-6FFFF	68000-6FFFF	68000-6FFFF
32			098000-09FFFF	32	60000-67FFF	60000-67FFF	60000-67FFF
32			090000-097FFF	32	58000-5FFFF	58000-5FFFF	58000-5FFFF
32			088000-08FFFF	32	50000-57FFF	50000-57FFF	50000-57FFF
32			080000-087FFF	32	48000-4FFFF	48000-4FFFF	48000-4FFFF
32			078000-07FFFF	32	40000-47FFF	40000-47FFF	40000-47FFF
32			070000-077FFF	32	38000-3FFFF	38000-3FFFF	38000-3FFFF
32			068000-06FFFF	32	30000-37FFF	30000-37FFF	30000-37FFF
32			060000-067FFF	32	28000-2FFFF	28000-2FFFF	28000-2FFFF
32			058000-05FFFF	32	20000-27FFF	20000-27FFF	20000-27FFF
32			050000-057FFF	32	18000-1FFFF	18000-1FFFF	18000-1FFFF
32			048000-04FFFF	32	10000-17FFF	10000-17FFF	10000-17FFF
32			040000-047FFF	32	08000-0FFFF	08000-0FFFF	08000-0FFFF
32			038000-03FFFF	4	07000-07FFF	07000-07FFF	07000-07FFF
32			030000-037FFF	4	06000-06FFF	06000-06FFF	06000-06FFF
32			028000-02FFFF	4	05000-05FFF	05000-05FFF	05000-05FFF
32			020000-027FFF	4	04000-04FFF	04000-04FFF	04000-04FFF
32			018000-01FFFF	4	03000-03FFF	03000-03FFF	03000-03FFF
32			010000-017FFF	4	02000-02FFF	02000-02FFF	02000-02FFF
32			008000-00FFFF	4	01000-01FFF	01000-01FFF	01000-01FFF
32			000000-007FFF	4	00000-00FFF	00000-00FFF	00000-00FFF

4-Mbit Word-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KW)			**4M**	**Size (KW)**			**4M**
4			3F000-3FFFF	32			38000-3FFFF
4			3E000-3EFFF	32			30000-37FFF
4			3D000-3DFFF	32			28000-2FFFF
4			3C000-3CFFF	32			20000-27FFF
4			3B000-3BFFF	32			18000-1FFFF
4			3A000-3AFFF	32			10000-017FFF
4			39000-39FFF	32			08000-0FFFF
4			38000-38FFF	4			07000-07FFF
32			30000-037FFF	4			06000-06FFF
32			28000-2FFFF	4			05000-05FFF
32			20000-2FFFF	4			04000-04FFF
32			18000-1FFFF	4			03000-03FFF
32			10000-017FFF	4			02000-02FFF
32			08000-0FFFF	4			01000-01FFF
32			00000-07FFF	4			00000-00FFF

APPENDIX E
BYTE-WIDE MEMORY MAP DIAGRAMS

Byte-Wide Memory Addressing

Top Boot				Bottom Boot			
Size (KB)	**8M**	**16M**	**32M**	**Size (KB)**	**8M**	**16M**	**32M**
8	FE000-FFFFF	1FE000-1FFFFF	3FE000-3FFFFF	64			3F0000-3FFFFF
8	FC000-FDFFF	1FC000-1FDFFF	3FC000-3FDFFF	64			3E0000-3EFFFF
8	FA000-FBFFF	1FA000-1FBFFF	3FA000-3FBFFF	64			3D0000-3DFFFF
8	F8000-F9FFF	1F8000-1F9FFF	3F8000-3F9FFF	64			3C0000-3CFFFF
8	F6000-F7FFF	1F6000-1F7FFF	3F6000-3F7FFF	64			3B0000-3BFFFF
8	F4000-F5FFF	1F4000-1F5FFF	3F4000-3F5FFF	64			3A0000-3AFFFF
8	F2000-F3FFF	1F2000-1F3FFF	3F2000-3F3FFF	64			390000-39FFFF
8	F0000-F1FFF	1F0000-1F1FFF	3F0000-3F1FFF	64			380000-38FFFF
64	E0000-EFFFF	1E0000-1EFFFF	3E0000-3EFFFF	64			370000-37FFFF
64	D0000-DFFFF	1D0000-1DFFFF	3D0000-3DFFFF	64			360000-36FFFF
64	C0000-CFFFF	1C0000-1CFFFF	3C0000-3CFFFF	64			350000-35FFFF
64	B0000-BFFFF	1B0000-1BFFFF	3B0000-3BFFFF	64			340000-34FFFF
64	A0000-AFFFF	1A0000-1AFFFF	3A0000-3AFFFF	64			330000-33FFFF
64	90000-9FFFF	190000-19FFFF	390000-39FFFF	64			320000-32FFFF
64	80000-8FFFF	180000-18FFFF	380000-38FFFF	64			310000-31FFFF
64	70000-7FFFF	170000-17FFFF	370000-37FFFF	64			300000-30FFFF
64	60000-6FFFF	160000-16FFFF	360000-36FFFF	64			2F0000-2FFFFF
64	50000-5FFFF	150000-15FFFF	350000-35FFFF	64			2E0000-2EFFFF
64	40000-4FFFF	140000-14FFFF	340000-34FFFF	64			2D0000-2DFFFF
64	30000-3FFFF	130000-13FFFF	330000-33FFFF	64			2C0000-2CFFFF
64	20000-2FFFF	120000-12FFFF	320000-32FFFF	64			2B0000-2BFFFF
64	10000-1FFFF	110000-11FFFF	310000-31FFFF	64			2A0000-2AFFFF
64	00000-0FFFF	100000-10FFFF	300000-30FFFF	64			290000-29FFFF
64		0F0000-0FFFFF	2F0000-2FFFFF	64			280000-28FFFF
64		0E0000-0EFFFF	2E0000-2EFFFF	64			270000-27FFFF
64		0D0000-0DFFFF	2D0000-2DFFFF	64			260000-26FFFF
64		0C0000-0CFFFF	2C0000-2CFFFF	64			250000-25FFFF
64		0B0000-0BFFFF	2B0000-2BFFFF	64			240000-24FFFF
64		0A0000-0AFFFF	2A0000-2AFFFF	64			230000-23FFFF
64		090000-09FFFF	290000-29FFFF	64			220000-22FFFF
64		080000-08FFFF	280000-28FFFF	64			210000-21FFFF
64		070000-07FFFF	270000-27FFFF	64			200000-20FFFF
64		060000-06FFFF	260000-26FFFF	64		1F0000-1FFFFF	1F0000-1FFFFF
64		050000-05FFFF	250000-25FFFF	64		1E0000-1EFFFF	1E0000-1EFFFF
64		040000-04FFFF	240000-24FFFF	64		1D0000-1DFFFF	1D0000-1DFFFF
64		030000-03FFFF	230000-23FFFF	64		1C0000-1CFFFF	1C0000-1CFFFF
64		020000-02FFFF	220000-22FFFF	64		1B0000-1BFFFF	1B0000-1BFFFF
64		010000-01FFFF	210000-21FFFF	64		1A0000-1AFFFF	1A0000-1AFFFF
64		000000-00FFFF	200000-20FFFF	64		190000-19FFFF	190000-19FFFF
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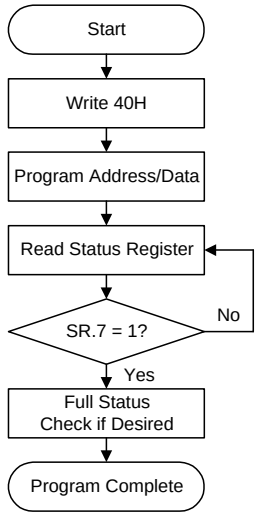
Byte-Wide Memory Addressing (Continued)

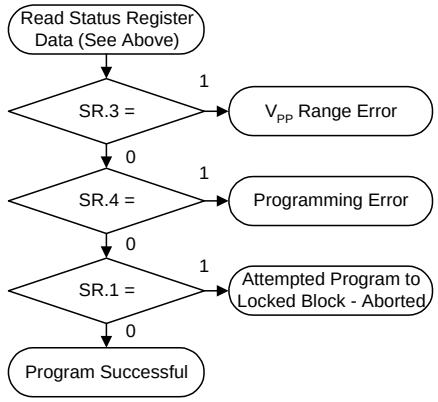
Top Boot				Bottom Boot			
Size (KB)	**8M**	**16M**	**32M**	**Size (KB)**	**8M**	**16M**	**32M**
64			1F0000-1FFFFF	64		180000-18FFFF	180000-18FFFF
64			1E0000-1EFFFF	64		170000-17FFFF	170000-17FFFF
64			1D0000-1DFFFF	64		160000-16FFFF	160000-16FFFF
64			1C0000-1CFFFF	64		150000-15FFFF	150000-15FFFF
64			1B0000-1BFFFF	64		140000-14FFFF	140000-14FFFF
64			1A0000-1AFFFF	64		130000-13FFFF	130000-13FFFF
64			190000-19FFFF	64		120000-12FFFF	120000-12FFFF
64			180000-18FFFF	64		110000-11FFFF	110000-11FFFF
64			170000-17FFFF	64		100000-10FFFF	100000-10FFFF
64			160000-16FFFF	64	F0000-FFFFF	0F0000-0FFFFF	0F0000-0FFFFF
64			150000-15FFFF	64	E0000-EFFFF	0E0000-0EFFFF	0E0000-0EFFFF
64			140000-14FFFF	64	D0000-DFFFF	0D0000-0DFFFF	0D0000-0DFFFF
64			130000-13FFFF	64	C0000-CFFFF	0C0000-0CFFFF	0C0000-0CFFFF
64			120000-12FFFF	64	B0000-BFFFF	0B0000-0BFFFF	0B0000-0BFFFF
64			110000-11FFFF	64	A0000-AFFFF	0A0000-0AFFFF	0A0000-0AFFFF
64			100000-10FFFF	64	90000-9FFFF	090000-09FFFF	090000-09FFFF
64			0F0000-0FFFFF	64	80000-8FFFF	080000-08FFFF	080000-08FFFF
64			0E0000-0EFFFF	64	70000-7FFFF	070000-07FFFF	070000-07FFFF
64			0D0000-0DFFFF	64	60000-6FFFF	060000-06FFFF	060000-06FFFF
64			0C0000-0CFFFF	64	50000-5FFFF	050000-05FFFF	050000-05FFFF
64			0B0000-0BFFFF	64	40000-4FFFF	040000-04FFFF	040000-04FFFF
64			0A0000-0AFFFF	64	30000-3FFFF	030000-03FFFF	030000-03FFFF
64			090000-09FFFF	64	20000-2FFFF	020000-02FFFF	020000-02FFFF
64			080000-08FFFF	64	10000-1FFFF	010000-01FFFF	010000-01FFFF
64			070000-07FFFF	8	0E000-0FFFF	00E000-00FFFF	00E000-00FFFF
64			060000-06FFFF	8	0C000-0DFFF	00C000-00DFFF	00C000-00DFFF
64			050000-05FFFF	8	0A000-0BFFF	00A000-00BFFF	00A000-00BFFF
64			040000-04FFFF	8	08000-09FFF	008000-009FFF	008000-009FFF
64			030000-03FFFF	8	06000-07FFF	006000-007FFF	006000-007FFF
64			020000-02FFFF	8	04000-05FFF	004000-005FFF	004000-005FFF
64			010000-01FFFF	8	02000-03FFF	002000-003FFF	002000-003FFF
64			000000-00FFFF	8	00000-01FFF	000000-001FFF	000000-001FFF

APPENDIX F
PROGRAM AND ERASE FLOWCHARTS



Bus Operation	Command	Comments
Write	Program Setup	Data = 40H
Write	Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent programming operations. SR Full Status Check can be done after each program or after a sequence of program operations. Write FFH after the last program operation to reset device to read array mode.		

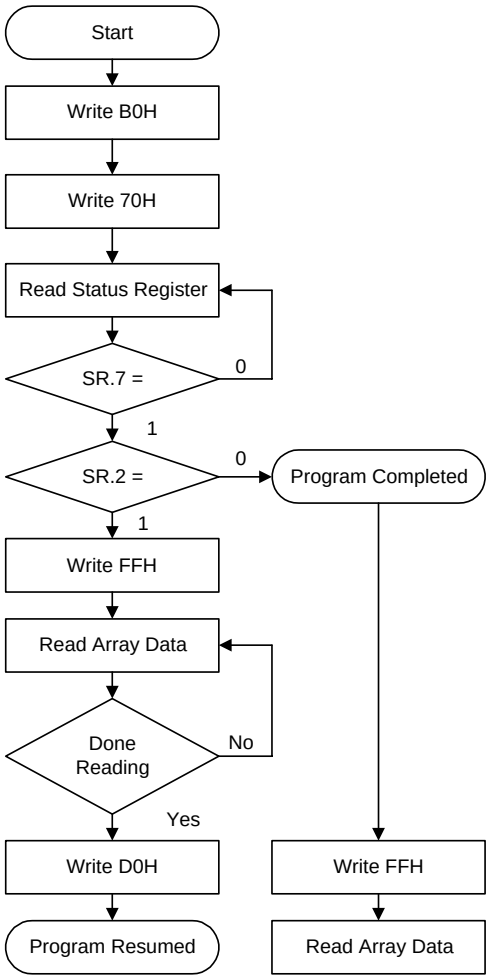
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = V_{PP} Program Error
Standby		Check SR.1 1 = Attempted Program to Locked Block - Program Aborted
SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine. SR.1, SR.3 and SR.4 are only cleared by the Clear Staus Register Command, in cases where multiple bytes are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

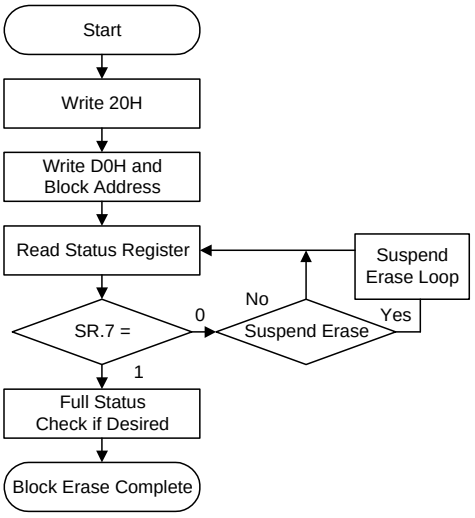
0580_E1

Figure 10. Program Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0H Addr = X
Write	Read Status	Data=70H Addr=X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Program Suspended 0 = Program Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being programmed.
Write	Program Resume	Data = D0H Addr = X

Figure 11. Program Suspend/Resume Flowchart



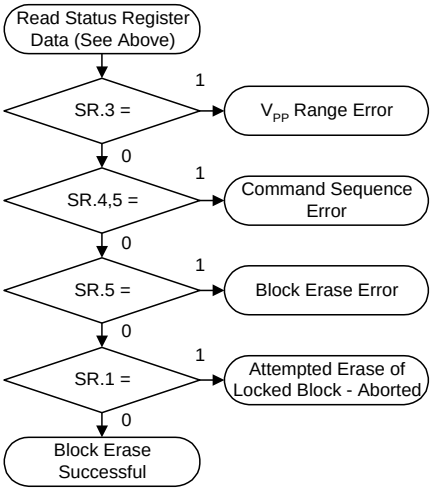
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to Be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to Be Erased
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.

Full Status Check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last write operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
Standby		Check SR.1 1 = Attempted Erase of Locked Block - Erase Aborted

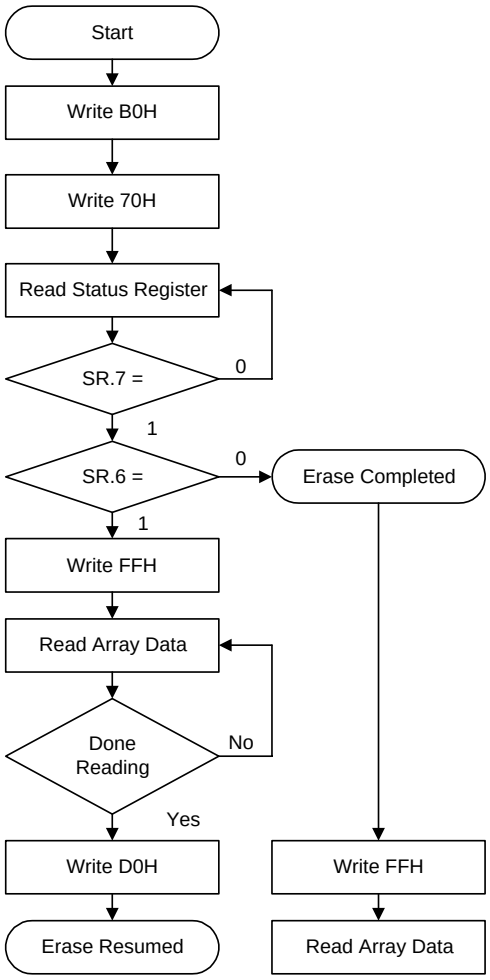
SR. 1 and 3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.1, 3, 4, 5 are only cleared by the Clear Staus Register Command, in cases where multiple bytes are erased before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

0580_E3

Figure 12. Block Erase Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Write	Read Status	Data=70H Addr=X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being erased.
Write	Erase Resume	Data = D0H Addr = X

Figure 13. Erase Suspend/Resume Flowchart