

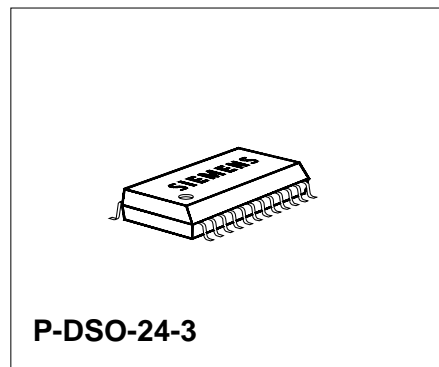
## Intelligent Sixfold Low-Side Switch

**TLE 4226 G**

**Bipolar-IC**

### Features

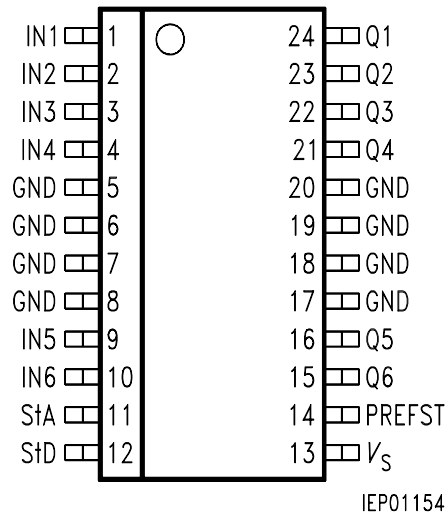
- Quad 50 mA outputs
- Dual 500 mA outputs
- Operating range  $V_S = 5\text{ V} \pm 5\%$
- Output stages with power limiting
- Open-collector outputs
- Shorted load protected within operating range
- Clamp-diodes to ground
- Status signaling
- TTL-compatible control inputs
- Overtemperature monitoring
- Temperature range – 40 to 125 °C



Type	Ordering Code	Package
▼ TLE 4226 G	Q67000-A9118	P-DSO-24-3 (SMD)
▼ New type		

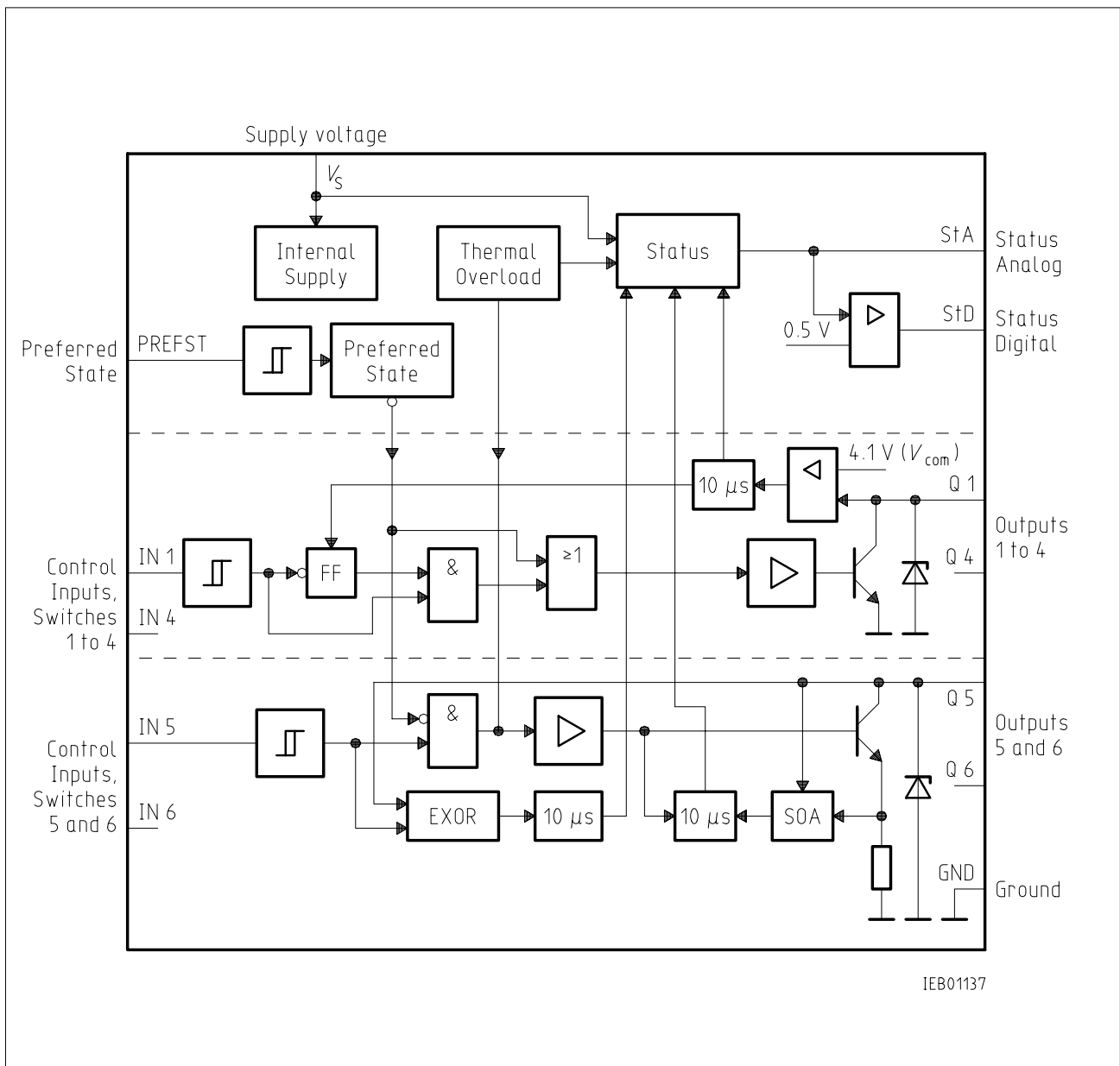
TLE 4226 G is an integrated, sixfold low-side power switch with power limiting of the 0.5 A outputs, shorted-load protection of the 50 mA switches and Z-diodes on all switches from output to ground. TLE 4226 G is particularly suitable for automotive and industrial applications.

## Pin Configuration (top view)



## Pin Definitions and Functions

Pin	Symbol	Function
1	IN1	Input switch 1, active high (50 mA)
2	IN2	Input switch 2, active high (50 mA)
3	IN3	Input switch 3, active high (50 mA)
4	IN4	Input switch 4, active high (50 mA)
5, 6, 7, 8	GND	Ground, cooling
9	IN5	Input switch 5, active high (500 mA)
10	IN6	Input switch 6, active high (500 mA)
11	StA	Status output analog
12	StD	Status output digital (error = low)
13	V <sub>s</sub>	Supply voltage
14	PREFST	Preferred state input, active low
15	Q6	Output switch 6 (500 mA)
16	Q5	Output switch 5 (500 mA)
17, 18, 19, 20	GND	Ground, cooling
21	Q4	Output switch 4 (50 mA)
22	Q3	Output switch 3 (50 mA)
23	Q2	Output switch 2 (50 mA)
24	Q1	Output switch 1 (50 mA)



**Block Diagram**

## Application Description

Applications in automotive electronics call for intelligent power switches that can be activated by logic signals, which have to be shorted load protected and which provide error feedback.

This IC contains six power switches connected to ground (low-side switches). On inductive loads the integrated Z-diodes clamp the discharging voltage.

By means of TTL signals on the control inputs (active high) all six switches can be activated independently of one another when a high level appears on the preferred-state input. When there is a low level on the preferred-state input, switches 1 to 4 are switched on, switches 5 and 6 are switched off regardless of the control-input levels. The inputs are highly resistive and therefore must not be left unconnected but should always be on fixed potential (noise immunity). Inputs that are not used, should be connected to low level to reduce the power consumption.

The analog status output signals the following errors by analog voltage levels:

- Overload
- Thermal overload
- Openload or shorted load to ground (only switches 5 and 6)

The following levels signal errors at the analog and digital status outputs.

Errors	Analog Status	Digital Status
Normal function	Low	High
Overload	1.0 V to 3.3 V	Low
Openload or shorted load to ground (only switches 5 and 6)	1.0 V to 1.7 V	Low
Thermal overload	> 3.5 V	Low

## Possible Input and Output Levels

Supply Voltage $V_s$	PREFST	IN1-6	Q1-Q4	Q5, Q6
2 to 5 V	Low	Random	Low	High
5 V	High	Low	High	High
5 V	High	High	Low	Low

## Circuit Description

### Input Circuits

The control inputs and the preferred-state input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors.

### Switching Stages

The output stages consist of NPN power transistors with open collectors. Each stage has its own protective circuit for limiting power dissipation and shorted load current, which makes the outputs shorted load protected to the supply voltage throughout the operating range. Integrated clamp-diodes limit positive voltage spikes that occur when inductive loads are discharged. Output currents, caused through negative voltages at the outputs, are compensated up to 50 mA for all outputs in total.

### Monitoring and Protective Functions

Each output is monitored (for overload) in its activated status. For the switches 1 to 4 overload is detected, if the switches are activated and the output voltage at the transistor is higher than 4.1 V for more than 10  $\mu$ s. The concerned output will be shutdown and both status outputs will be set. The switch can only be activated again if the corresponding input is switched off and then on again. If the output voltage does not exceed 4.1 V, the output is not shutdown and the status outputs are not set, although an overload may occur. The switches 5 and 6 are protected through a SOA-circuit. It is suppressed for at least 10  $\mu$ s when the switch is turned on before it can start limiting the overload current. The status outputs also monitor openload or shorted load to ground at the switches 5 and 6 in deactivated mode.

An analog signal is applied to the analog status output only when protection function is active. If several malfunctions appear coincident, the highest voltage level of the analog status output will dominate. Simultaneously the digital status output will be set.

The IC is also protected against thermal overload. If a chip temperature of typically 155 °C is attained, the status outputs monitor overtemperature. If the temperature continues to increase, the inputs and outputs of the switches 5 and 6 are shutdown. The switches 1 to 4 will not shutdown, so precaution has to be taken in the application to prevent a further increase of the chip temperature, which may destroy the IC. After cooling down below 140 °C the overtemperature monitoring will be reset and the outputs of the switches 5 and 6 can be activated again.

If the minimum supply voltage for operation is not maintained, the outputs are deactivated. At a supply voltage of higher than 1.8 V, the outputs 1 to 4 are switched on, if pin 14 (PREFST) is connected to ground over a resistance smaller 1 M $\Omega$ . The outputs 1 to 4 can be controlled via the inputs, if pin 14 (PREFST) is switched to high or not connected. Characteristics may be beyond the specified values. Full function is guaranteed in the supply voltage range of 5 V  $\pm$  5 %.

## Absolute Maximum Ratings

$T_j = -40$  to  $150\text{ °C}$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

## Voltages

Supply voltage	$V_S$	– 1	10	V	
Supply voltage load circuit	$V_{Q1-6}$	– 0.7	25	V	
Input voltage	$V_{IN1-6}$ , $V_{PREFST}$	– 0.7	20	V	

## Currents

Output current	$I_{Q1-6}$				limited internally
Current at reverse poling	$I_{Q5-6}$	– 500		mA	
Current at reverse poling	$I_{Q1-4}$	– 50		mA	
Clamping current	$I_{QZ5-6}$		700	mA	see diagram
Clamping current	$I_{QZ1-4}$		70	mA	
Junction temperature	$T_j$	– 40	150	°C	Overtemperature protection shuts down the switches 5 and 6 at $165\text{ °C}$
Storage temperature	$T_{stg}$	– 55	125	°C	

## Operating Range

Supply voltage	$V_S$ $V_S$	4.75 4	5.25	V	full function, but status outputs cannot be evaluated
Output voltage	$V_Q$	– 0.3	24	V	
Ambient temperature	$T_A$	– 40	110	°C	$T_j \leq 150\text{ °C}$
Invert current for $Q_{1-6}$ in total	$I_{sup}$	50		mA	
Input voltage	$V_{IN}$	– 0.5	15	V	
Thermal resistance junction to case	$R_{th\,JC}$		15	K/W	1)
Thermal resistance junction to ambient	$R_{th\,JA}$		65	K/W	

1) Pins 5 to 8 and 17 to 20 have to be connected to the ground-plane used as thermal heatsink to achieve the optimum thermal resistance.

## Characteristics

$V_S = 5\text{ V}$ , unless stated otherwise;  $T_j = -40\text{ to }140\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

## Supply Voltage ( $V_S$ )

Quiescent current	$I_S$		8	11	mA	Outputs OFF
Supply Current	$I_S$		50	65	mA	Outputs ON

## Inputs (IN1-6, PREFST)

H-input voltage	$V_{IH}$	1.3	1.8	2.1	V	
L-input voltage	$V_{IL}$	0.9	1.2	1.5	V	
Hysteresis	$\Delta V_I$	0.3	0.6	1.0	V	
H-Input current	$I_{IH}$	-2		3	$\mu\text{A}$	$0.9\text{ V} < V_I < 6\text{ V}$
L-Input current	$I_{IL}$	-10		1	$\mu\text{A}$	$0.2\text{ V} < V_I < 0.9\text{ V}$
Input current	$I_I$	-2		3	$\mu\text{A}$	$0\text{ V} < V_I < 6\text{ V}; V_S = 0\text{ V}$

## Power Outputs (Q1-6)

Load Current	$I_{Q1-4}$	50			mA	$V_S = 2\text{ V}$ and resistance from PREFST to ground $< 1\text{ M}\Omega$
Saturation voltage	$V_{QSat5,6}$		0.5	0.8	V	$I_Q = 0.4\text{ A}$ ; output ON
Saturation voltage	$V_{QSat1-4}$		0.4	0.6	V	$I_Q = 50\text{ mA}$ ; output ON
Saturation voltage	$V_{QSat1-4}$			0.22	V	$I_Q = 20\text{ mA}$ ; output ON
Compare voltage	$V_{com}$	4.1		4.7	V	
Turn-ON delay time	$t_{DON}$	0.2	1	1.5	$\mu\text{s}$	see diagrams
Turn-OFF delay time	$t_{DOFF}$	0.2	2	3.5	$\mu\text{s}$	$20\text{ mA} < I_{Q1-4} < 50\text{ mA}$ , $200\text{ mA} < I_{Q5,6} < 500\text{ mA}$

## Overtemp. Protection

Monitoring threshold	$T_{thSt}$	150	155		$^{\circ}\text{C}$	only switches 5 and 6 are shut down
Shutdown threshold hysteresis	$T_{tho}$	5	10		K	
Reset threshold	$T_{thRes}$	140		150	$^{\circ}\text{C}$	after shutdown

## Characteristics (cont'd)

$V_S = 5 \text{ V}$ , unless stated otherwise;  $T_j = -40 \text{ to } 140 \text{ }^\circ\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

## Outputs (Q1-6)

Clamping voltage	$V_{Q1-4}$	25.5		33	V	$I_Q = 50 \text{ mA}$
Clamping voltage	$V_{Q5, 6}$	25.5		35	V	$I_Q = 500 \text{ mA}$
Shorted load current	$I_{Q1-4 \text{ max}}$	60		170	mA	$V_Q < 16.5 \text{ V}$
Shorted load current	$I_{Q5, 6}$	500		900	mA	$V_Q \leq 10 \text{ V}; T_j \leq 130 \text{ }^\circ\text{C}$
Sink current	$I_{Q5, 6}$	2		10	$\mu\text{A}$	$V_Q = 5 \text{ V}$
Shutdown threshold						
Leakage current	$I_{Q1-4}$			1	$\mu\text{A}$	switches off, $V_Q = 24 \text{ V}$ $T_j = 125 \text{ }^\circ\text{C}$
Leakage current	$I_{Q5, 6}$			200	$\mu\text{A}$	switches off, $V_Q = 16.5 \text{ V}$ $T_j = 125 \text{ }^\circ\text{C}$

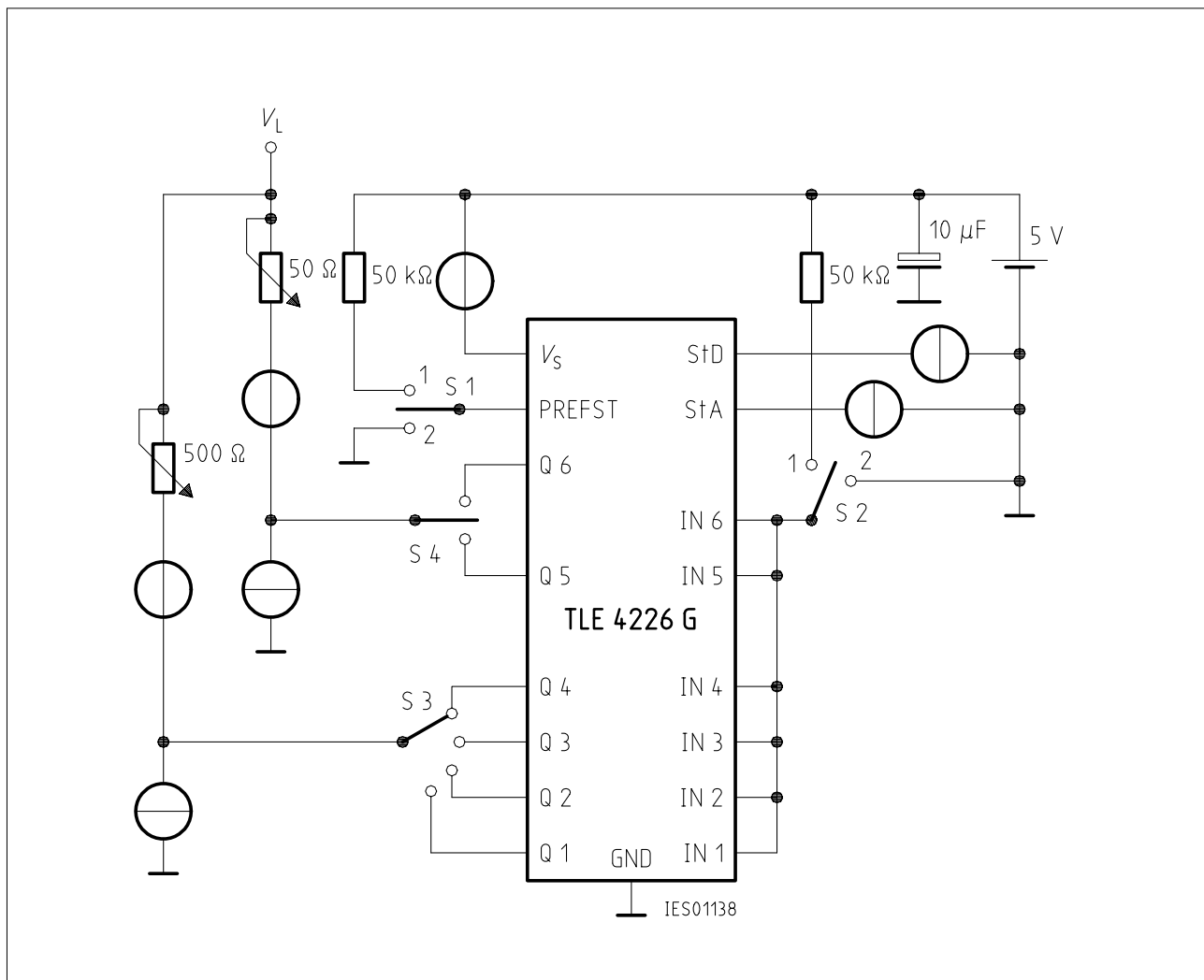
## Status Output Analog (StA)

Normal function	$V_{StA}$			0.5	V	
Error output 6	$V_{StA}$	1.0		1.3	V	
Error output 5	$V_{StA}$	1.4		1.7	V	
Overload output 4	$V_{StA}$	1.8		2.1	V	
Overload output 3	$V_{StA}$	2.2		2.5	V	
Overload output 2	$V_{StA}$	2.6		2.9	V	
Overload output 1	$V_{StA}$	3.0		3.3	V	
Thermal overload	$V_{StA}$	3.5			V	
Source resistance of analog status output	$R_{QStA}$	30		250	$\Omega$	$-I_{QStA} = 50 \dots 100 \text{ } \mu\text{A}$
Delay time of status	$t_{dStA/D}$	10	15	30	$\mu\text{s}$	overload at switches 5 and 6
Delay time of output protection	$t_{dSQ1-6}$	10		30	$\mu\text{s}$	switches 5 and 6 during turn on

## Status Output Digital (StD)

Pull-up resistance	$R_{StD}$	10	20	30	k $\Omega$	
Saturation voltage	$V_{StDSat}$			0.4	V	$I_{StD} = 4 \text{ mA}$

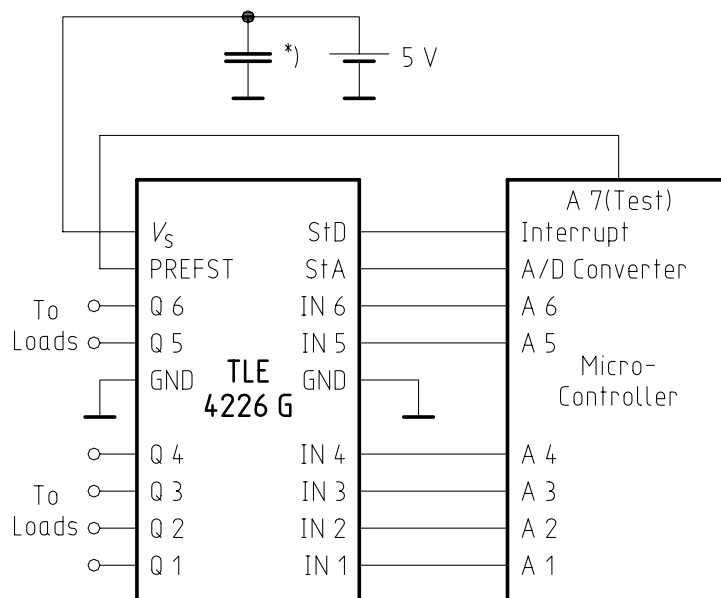




## Test Circuit

S1 in position 1: all outputs can be activated (position 1) or deactivated (position 2) by S2

S1 in position 2: preferred state



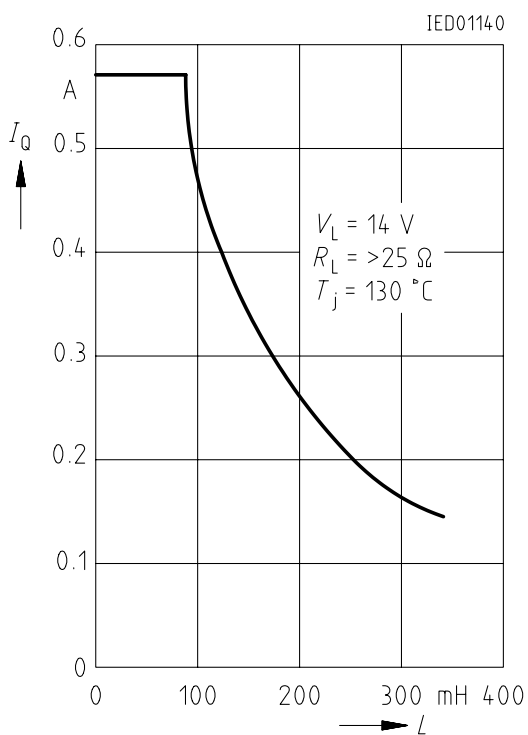
\*) The capacitance depends on the inductance and current load of the supply.

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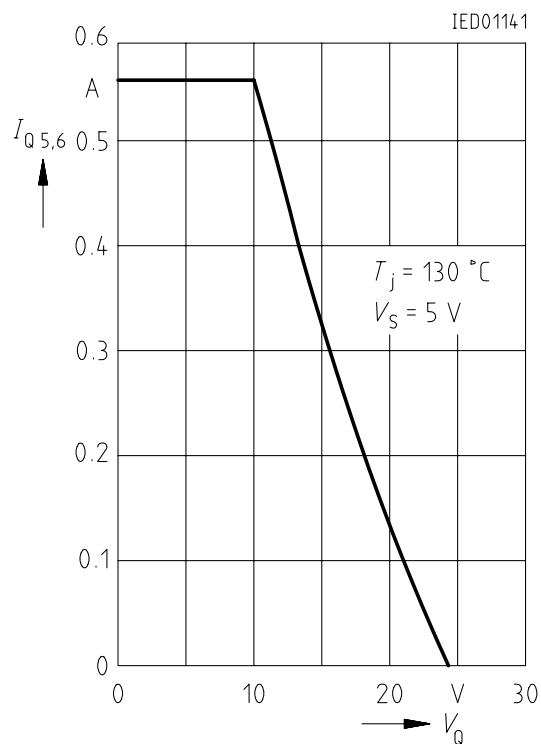
## Application Circuit

\*) The capacitance depends on the inductance and current load of the supply.

**Permissible Load Inductance versus Load Current**

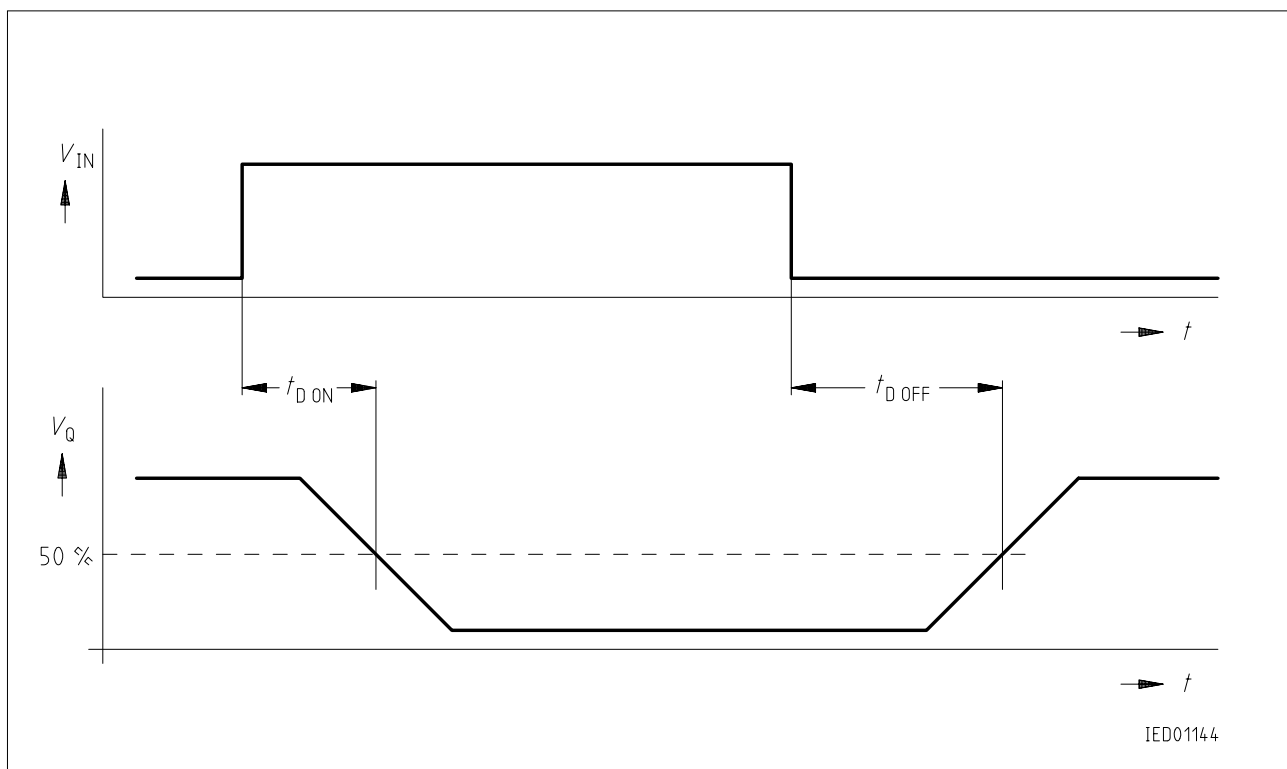


**Shorted Load Current  $I_{Q5,6}$  versus Output Voltage (Outputs 5 and 6)**

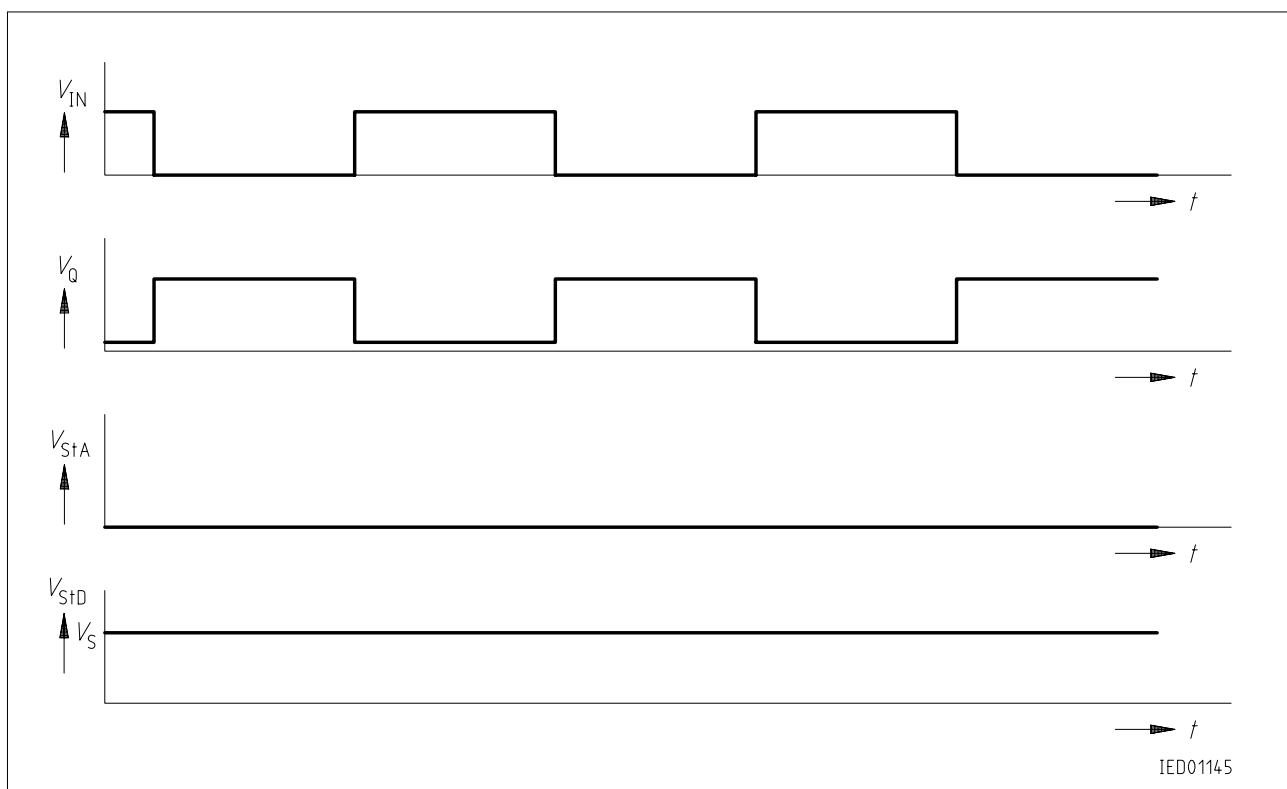


**Note:**

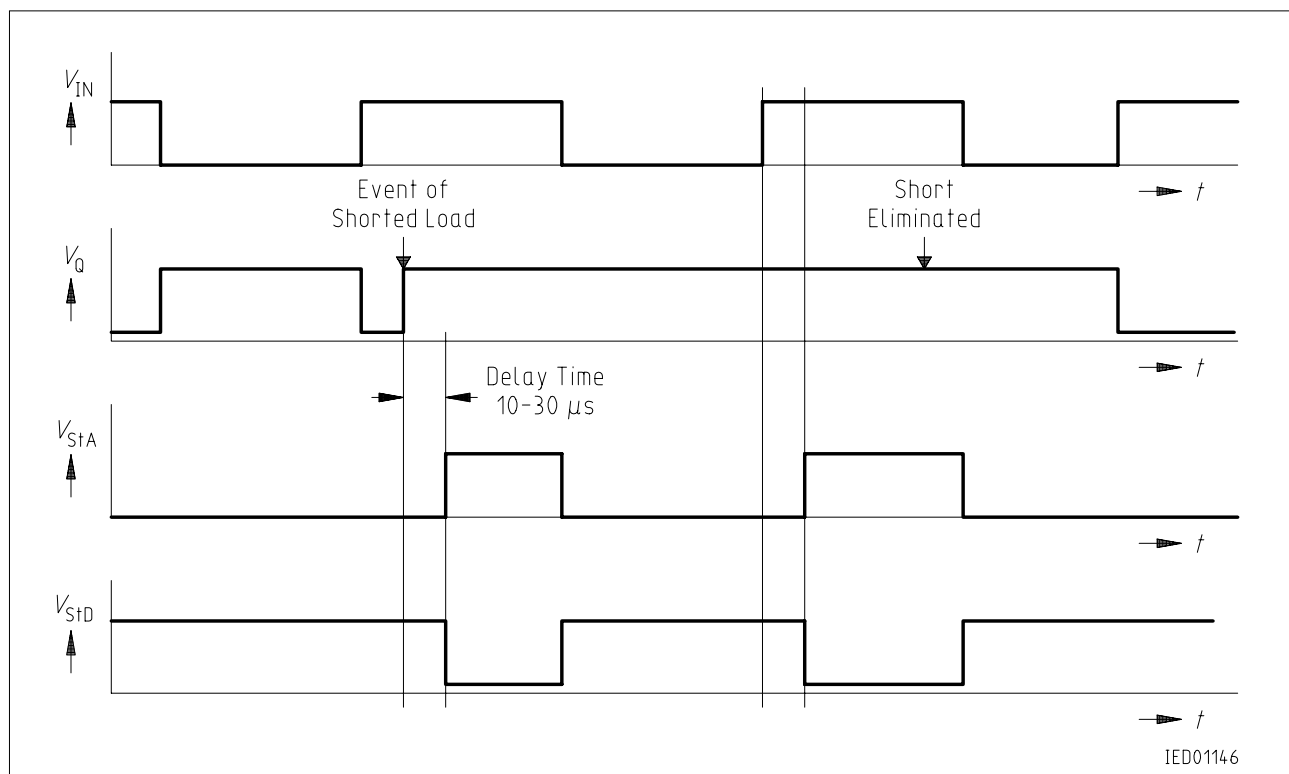
While switching the maximum inductive loads, the maximum temperature  $T_j$  of  $150^\circ \text{C}$  may be briefly exceeded. The IC will not be destroyed by this, but the restrictions concerning useful life should be observed.



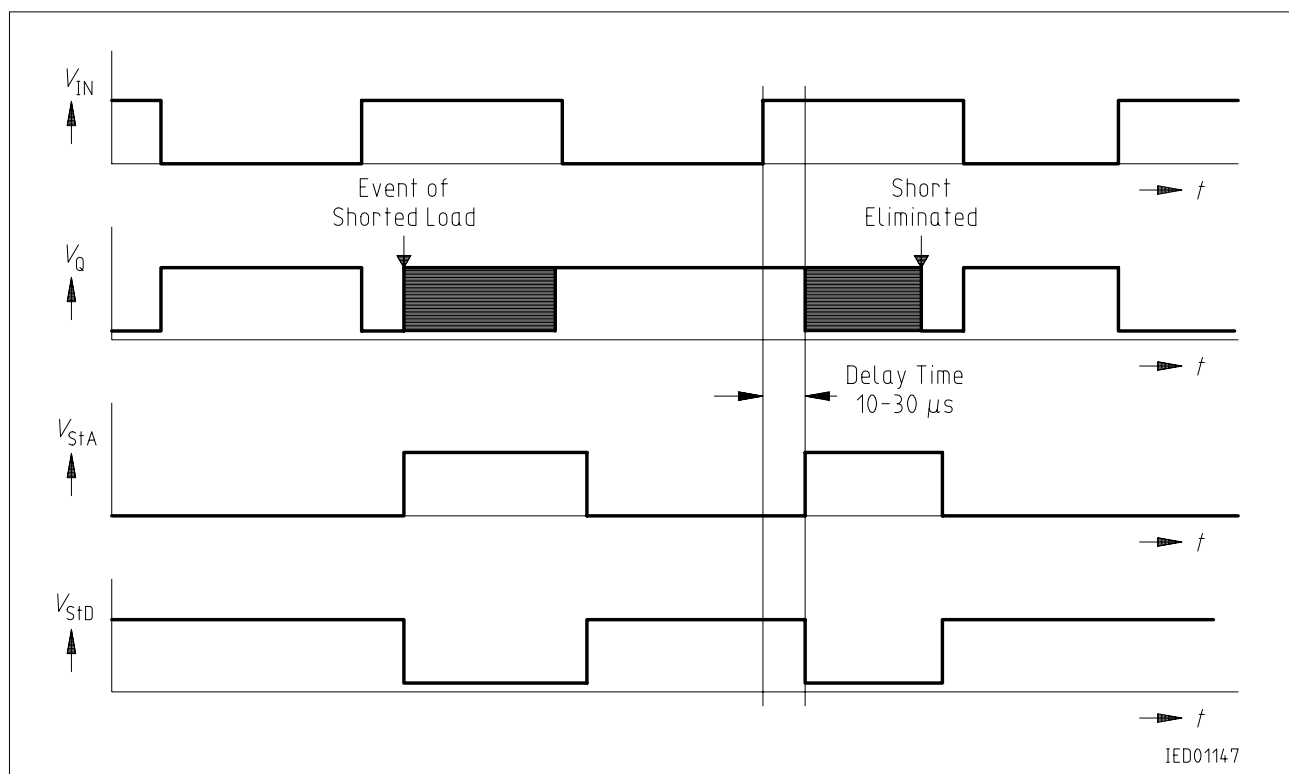
## Timing Diagrams



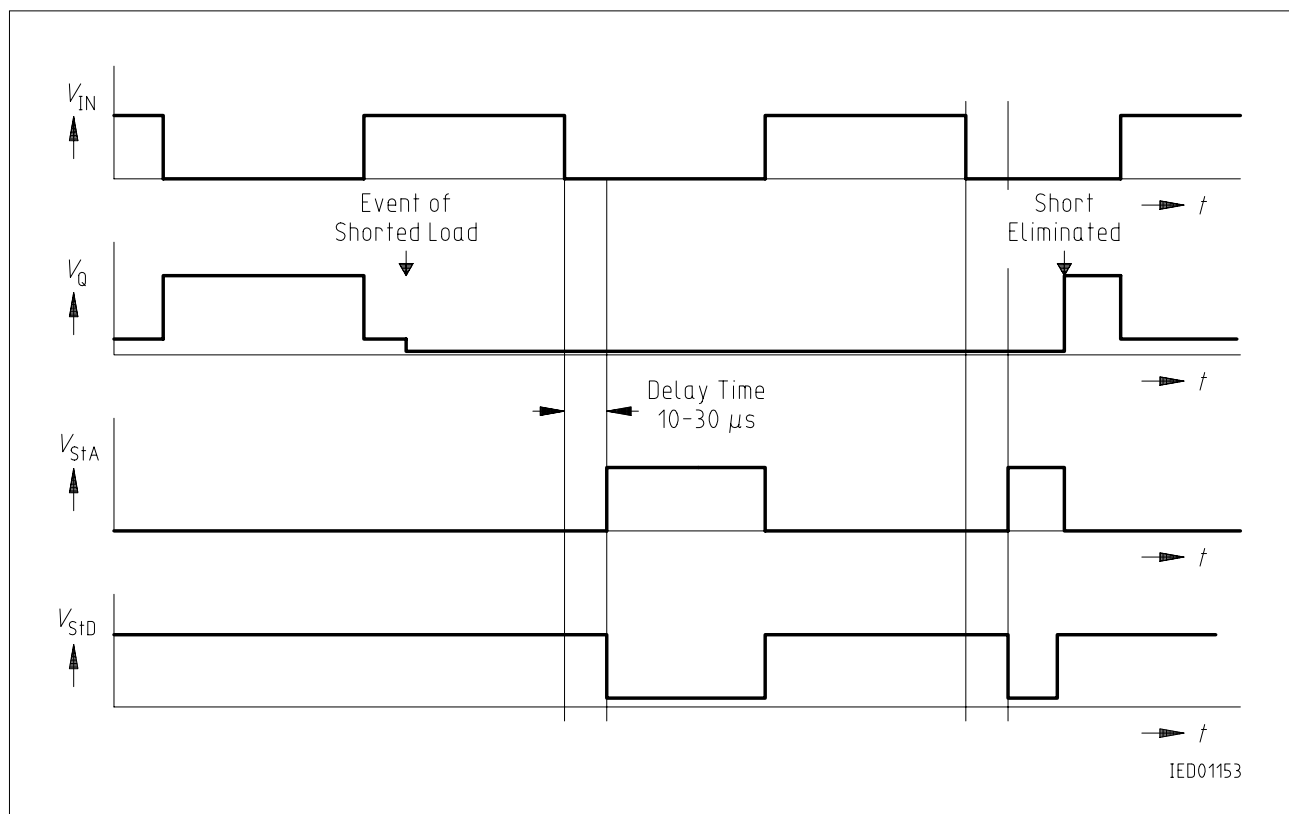
## Signals of Inputs and Outputs of Switches 1 to 6 Normal Function (no Error)



**Signals of Inputs and Outputs of Switches 1 to 4  
Shorted Load to Supply Voltage of Load Circuit**



**Signals of Inputs and Outputs of Switches 5 and 6  
Shorted Load to Supply Voltage of Load Circuit**

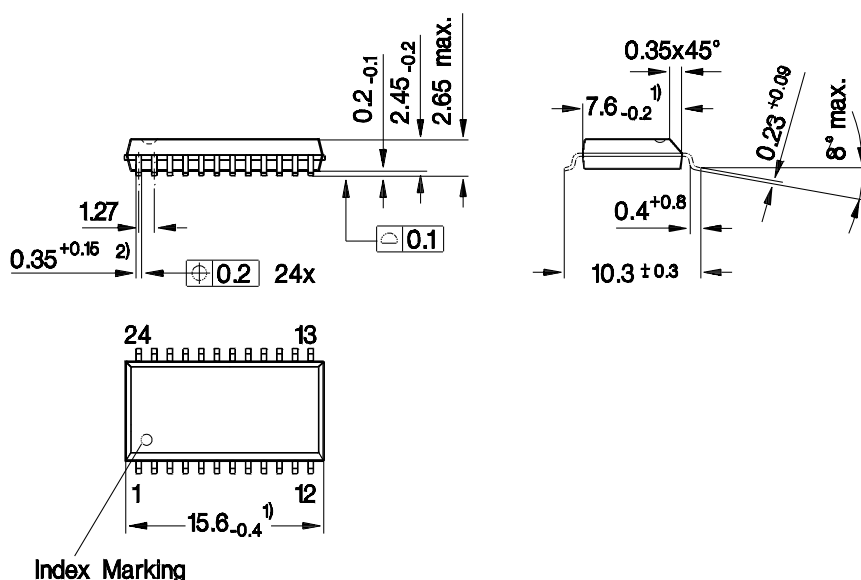


**Signals of Inputs and Outputs of Switches 5 and 6  
Shorted Load to Ground**

## Package Outlines

### P-DSO-24-3

(Plastic Dual Small Outline Package)



- Index Marking
- 1) Does not include plastic or metal protrusion of  $0.15$  max. per side
  - 2) Does not include dambar protrusion

GPS05144

## Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm