

12V MOSFET Drivers with Output Disable for Single Phase Synchronous-Rectified Buck Converter

General Description

The uP6281 is a dual, high voltage MOSFET driver optimized for driving two N-Channel MOSFETs in a synchronous-rectified buck converter. Each driver is capable of driving a 5000pF load with 30ns transition time. This device combined with uPI multi-phase buck PWM controller forms a complete core voltage regulator for advanced micro-processors.

The uP6281 features adaptive anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintains minimum deadtime for optimized efficiency.

Both gate drives are turned off by pulling low OD# pin or high-impedance at PWM pin, preventing rapid output capacitor discharge during system shutdowns.

Other feature is supply input under voltage lockout. The uP6281 is available in thermal enhanced PSOP-8L or WDFN3x3-8L packages.

Applications

- Core Voltage Supplies for Desktop, Motherboard CPUs
- High Frequency Low Profile DC/DC Converters
- High Current Low Voltage DC/DC Converters

Features

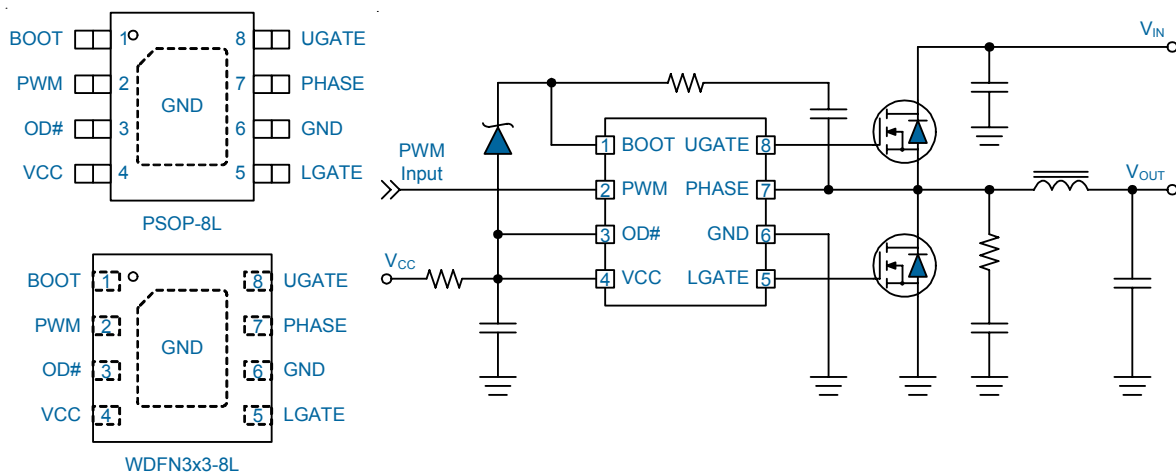
- All-In-One Synchronous Buck Drivers
- Bootstrapped High-Side Driver
- Adaptive Anti-Shoot-Through Protection Circuitry
- 1 PWM Signal Generates both Drivers
- Tri-State Input for Bridge Shutdown
- Output Disable Control Turns Off both MOSFETs
- Under Voltage Lockout for Supply Input
- PSOP-8L or WDFN3x3-8L Packages
- RoHS Compliant and Halogen Free

Ordering Information

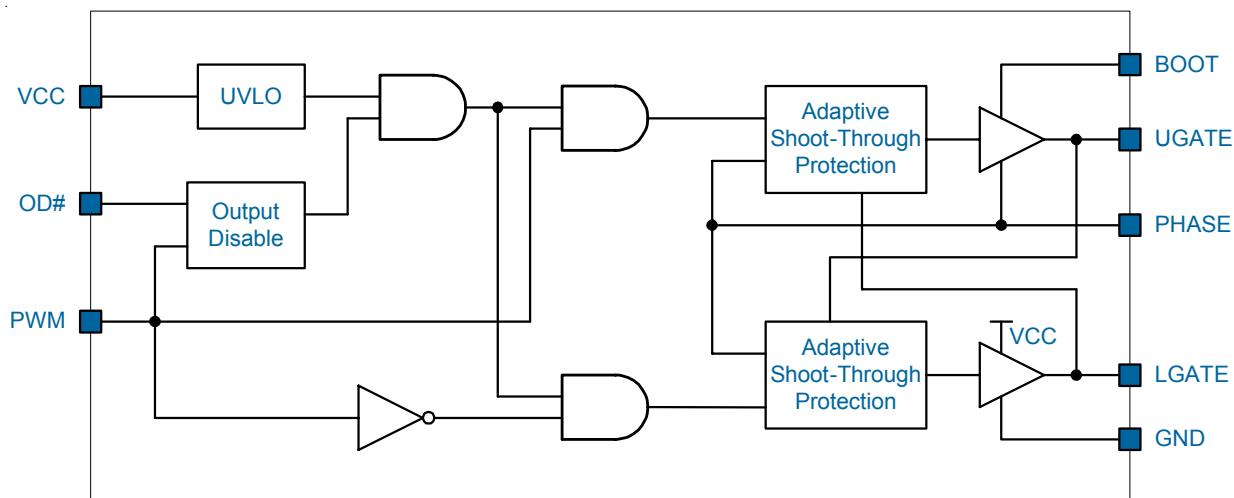
Order Number	Package Type	Remark
uP6281ASU8	PSOP - 8L	
uP6281ADD8	WDFN3x3 - 8L	

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration & Typical Application Circuit



Functional Block Diagram



Functional Pin Description

No.	Pin Name	Pin Function
1	BOOT	Bootstrap Supply for the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Ensure that C_{BOOT} is placed near the IC.
2	PWM	PWM Input. This pin receives logic level input and controls the driver outputs.
3	OD#	Output Disable. This pin disables normal operation and forces both UGATE and LGATE off when it is pulled low.
4	VCC	Supply Voltage for the IC. This pin provides bias voltage for the IC. Connect this pin to 12V voltage source and bypass it with an R/C filter.
5	LGATE	Lower Gate Driver Output. Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turn off.
6	GND	Ground for the IC. All voltages levels are measured with respect to this pin.
7	PHASE	PHASE Switch Node. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
8	UGATE	Upper Gate Driver Output. Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
Exposed Pad (GND)		Ground for the IC. The exposed pad should be well soldered to PCB for effective heat conduction.

Functional Description

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The uP6281 features adaptive anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintains minimum deadtime for optimized efficiency.

Both gate drives are turned off by pulling low OD# pin or high-impedance at PWM pin, preventing rapid output capacitor discharge during system shutdowns.

Other feature is supply input under voltage lockout. The uP6281 is available in thermal enhanced PSOP-8L or WDFN3x3-8L packages.

Output Disable

Logic low of OD# disables the gate drivers and keep both output low. Tie the OD# pin to controller power directly if the output disable function is not used.

PWM Input

The PWM pin is a tri-state input. Logic high turns on the high-side gate driver and turns off the low side gate driver once the POR of VCC is granted and OD# is kept high. Logic low turns off the high side gate driver and turns off the low side gate driver.

High impedance input at PWM pin will keep both high-side and low-side gate drivers low and turns off both MOSFETs. The PWM pin voltage is kept around 2.0V by internal bias resistors when floating.

Low Side Driver

The low-side driver is designed to drive a ground-referenced N-Channel MOSFET. The bias to the low-side driver is internally connected to VCC supply and GND. The low-side driver output is out of phase with the PWM input when it is enabled. The low side driver is held low if the OD# pin is pulled low or high-impedance at PWM pin.

High-Side Driver

The high-side driver is designed to drive a floating N-Channel MOSFET. The bias voltage to the high-side driver internally connected to BOOT and PHASE pins. An external bootstrap supply circuit that is connected between BOOT and PHASE pins provides the bias current for the high-side gate driver.

The bootstrap capacitor C_{BOOT} is charged to V_{CC} when PHASE pin is grounded by turning on the low-side MOSFET. The PHASE raises to V_{IN} when the high-side MOSFET is turned on, forcing the BOOT pin voltage to $V_{IN} + V_{CC}$ that provides voltage to hold the high-side MOSFET on.

The high-side gate driver output is in phase with the PWM input when it is enabled. The high-side driver is held low if the OD# pin is pulled low or high-impedance at PWM pin.

Adaptive Shoot Through Protection

The adaptive shoot-through circuit prevents the high-side and low-side MOSFETs from being ON simultaneously and conducting destructive large current. It is done by turning on one MOSFET only after the other MOSFET is off already with adequately delay time.

At the high-side off edge, UGATE and PHASE voltages are monitored for anti-shoot-through protection. The uP6281 will not begin to output low-side driver high until both $(V_{UGATE} - V_{PHASE})$ and V_{PHASE} are lower than 1.2V, making sure the high-side MOSFET is turned off completely.

At the low-side off edge, LGATE voltage is monitored for anti-shoot-through protection. The uP6281 will not begin to output high-side driver high until V_{LGATE} is lower than 1.2V, making sure the low-side MOSFET is turned off completely.

Absolute Maximum Rating

Supply Input Voltage, VCC12 (Note 1)	-0.3V to +15V
BOOT to PHASE	-0.3V to +15V
PHASE to GND	
DC	-0.7V to 15V
< 200ns	-8V to 30V
BOOT to GND	
DC	-0.3V to VCC12 + 15V
< 200ns	-0.3V to 42V
UGATE to PHASE	
DC	-0.3V to (BOOT - PHASE + 0.3V)
<200ns	-5V to (BOOT - PHASE + 0.3V)
LGATE to GND	
DC	-0.3V to + (VCC12 + 0.3V)
<200ns	-5V to VCC12 + 0.3V
PWM	-0.3V to +6V
OD#	-0.3V to (VCC + 0.3)V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
ESD Rating (Note 2)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

Thermal Information

Package Thermal Resistance (Note 3)	
PSOP-8 θ_{JA}	50°C/W
WDFN3x3-8L θ_{JA}	68°C/W
PSOP-8L θ_{JC}	5°C/W
WDFN3x3-8L θ_{JC}	6°C/W
Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$	
PSOP-8L	2.0W
WDFN3x3-8L	1.47W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4)	-40°C to +125°C
Operating Ambient Temperature Range	-40°C to +85°C
Supply Input Voltage, V_{CC}	+10.8V to 13.2V

Electrical Characteristics

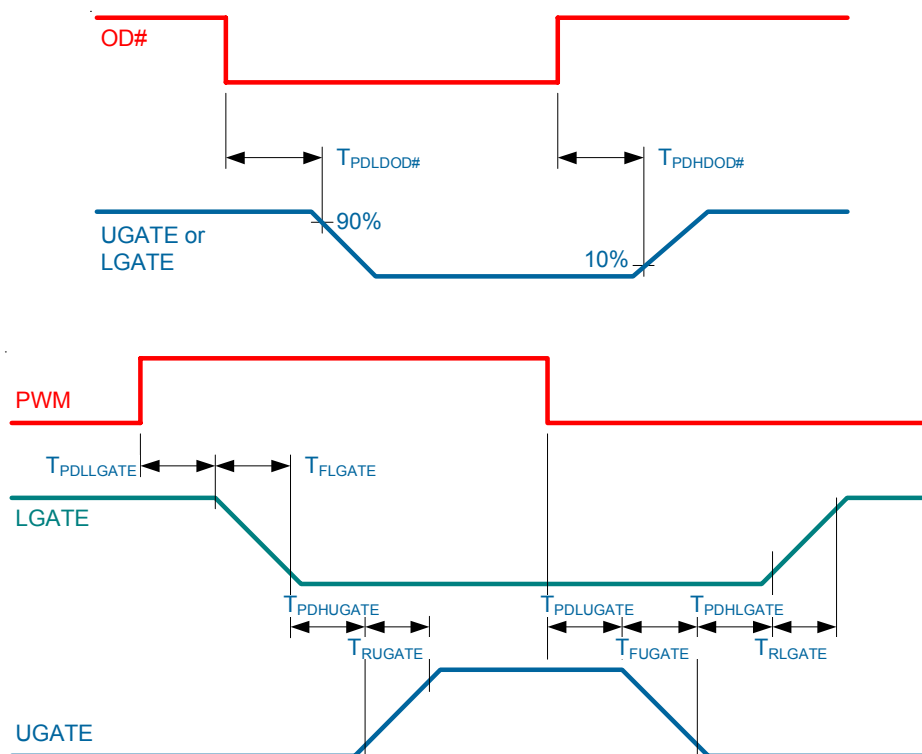
($V_{CC} = 12\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Input Voltage	V_{CC}		10.8	--	13.2	V
Supply Input Current	I_{CC}	PWM = OD# = 0V, each channel	--	1	2.5	mA
VCC POR Rising Threshold	V_{CCRTH}	V_{CC} rising	4.0	4.2	4.4	V
VCC POR Hysteresis	V_{CCHYS}		--	0.25	--	V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Input						
Input High Threshold	PWM _{RTH}		3.15	3.45	3.75	V
Input Low Threshold	PWM _{FTH}		0.6	0.9	1.2	V
PWM Floating Voltage	PWM _{FLT}		--	2.0	--	V
PWM Input Current	I _{PWM}	PWM = 0V	-420	-280	-140	uA
		PWM = 5V	1.0	1.6	1.9	mA
Output Disable Input OD#						
Input High	OD# _H		2.6	--	--	V
Input Low	OD# _L		--	--	0.8	V
OD# Input Current	I _{OD#}	OD# = 0V to 5V	-1	--	1	uA
Propogation Delay Time	T _{PDHOD#}		--	20	45	ns
	T _{PDL0D#}		--	20	45	ns
High Side Driver						
Output Resistance, Sourcing	R _{H_SRC}	V _{BOOT} - V _{PHASE} = 12V, I _{UGATE} = -80mA	--	1.2	2.4	Ω
Output Resistance, Sinking	R _{H_SNK}	V _{BOOT} - V _{PHASE} = 12V, I _{UGATE} = 80mA	--	0.8	1.6	Ω
Output Rising Time	T _{RUGATE}	V _{BOOT} - V _{PHASE} = 12V, C _{LOAD} = 3nF	--	35	45	ns
Output Falling Time	T _{FUGATE}	V _{BOOT} - V _{PHASE} = 12V, C _{LOAD} = 3nF	--	20	30	ns
Propagation Delay Time	T _{PDHUGATE}	V _{BOOT} - V _{PHASE} = 12V	--	40	65	ns
	T _{PDLUGATE}	V _{BOOT} - V _{PHASE} = 12V	--	20	35	ns
Low Side Driver						
Output Resistance, Sourcing	R _{L_SRC}	V _{CC} = 12V, I _{LGATE} = -80mA	--	1.2	2.4	Ω
Output Resistance, Sinking	R _{L_SNK}	V _{CC} = 12V, I _{LGATE} = 80mA	--	0.8	1.6	Ω
Output Rising Time	T _{RLGATE}	V _{CC} = 12V, C _{LOAD} = 3nF	--	35	45	ns
Output Falling Time	T _{FLGATE}	V _{CC} = 12V, C _{LOAD} = 3nF	--	20	30	ns
Propagation Delay Time	T _{PDHLGATE}	V _{CC} = 12V	--	40	65	ns
	T _{PDL LGATE}	V _{CC} = 12V	--	20	35	ns

Electrical Characteristics



Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

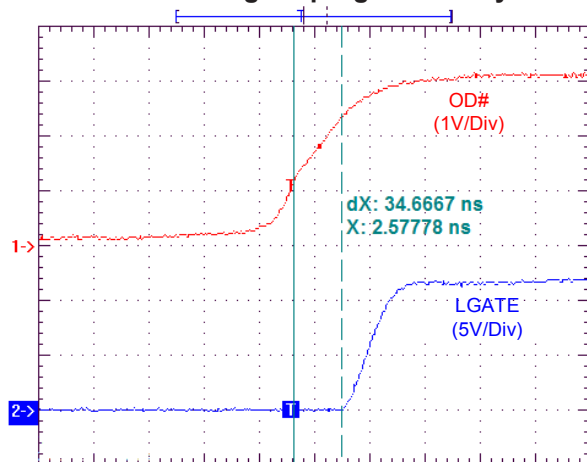
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

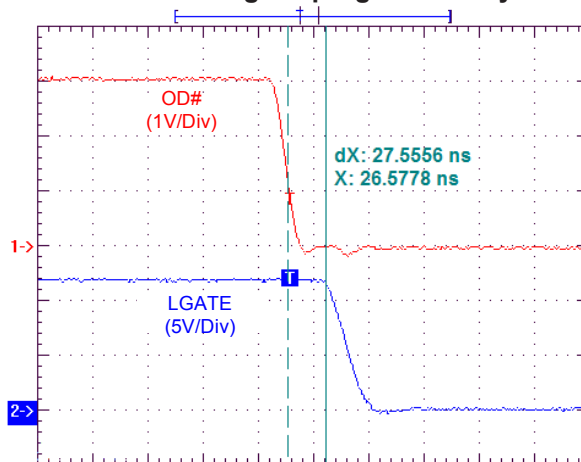
Typical Operation Characteristics

OD# Rising Propagation Delay



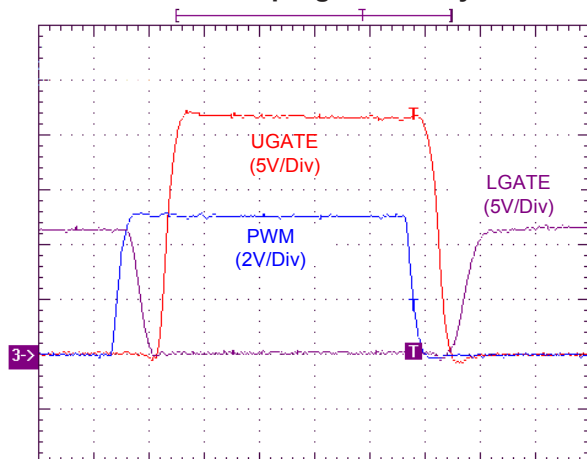
Time (40ns/Div)
PWM = 0V, 20MHz bandwidth limited

OD# Falling Propagation Delay



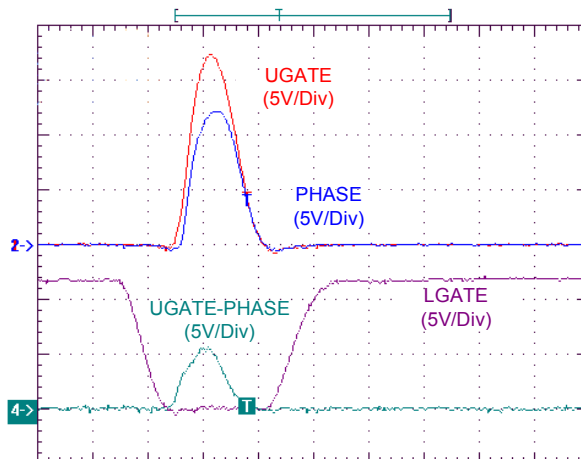
Time (40ns/Div)
PWM = 0V, 20MHz bandwidth limited

PWM Propagation Delay



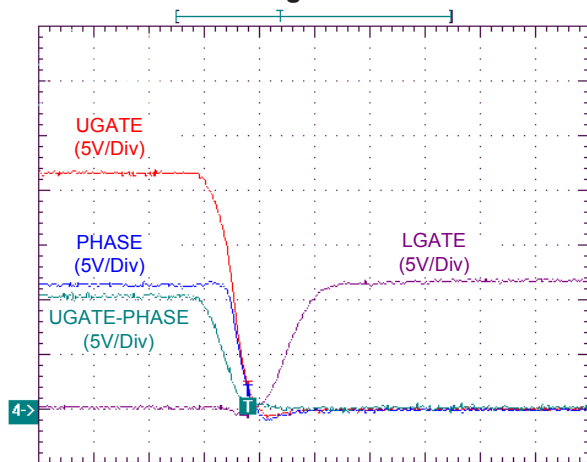
Time (80ns/Div)
20MHz bandwidth limited

Short Pulse Waveforms



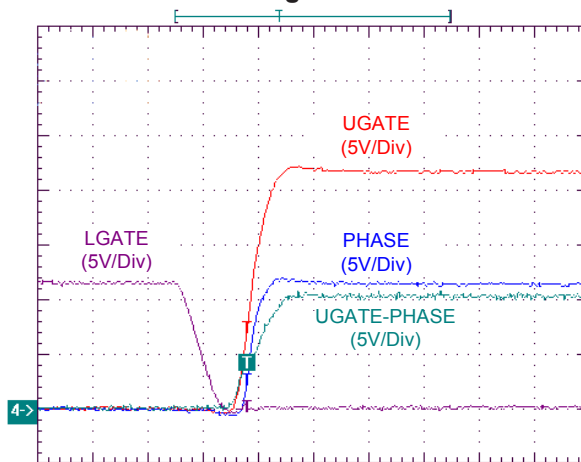
Time (40ns/Div)
20MHz bandwidth limited

Switching Waveforms



Time (40ns/Div)
20MHz bandwidth limited

Switching Waveforms



Time (40ns/Div)
20MHz bandwidth limited

Application Information

The power dissipation in uP6281 is dependent of the supply voltage, the PWM frequency and the input capacitance of the MOSFET:

$$P_{LOSS} = V_{CC} \{ I_{CC} + [V_{CC}(C_{ISS_U} + C_{ISS_L}) + V_{IN} \times C_{OSS_U}] f_{PWM} \}$$

where V_{CC} is the supply voltage, I_{CC} is the operation current of the control circuit, C_{ISS_U} and C_{ISS_L} are the total input capacitance of the upper and lower MOSFET respectively, V_{IN} is the supply voltage of the buck converter, C_{OSS_U} is the reverse transfer capacitance regarding the Miller effect and f_{PWM} is the PWM input frequency. Take a typical case for example, $V_{CC} = 12V$, $I_{CC} = 1mA$, $C_{ISS_U} = 2 \times 1.5nF$, $C_{OSS_U} = 2 \times 0.1nF$, $V_{IN} = 12V$, $C_{ISS_L} = 2 \times 3nF$, $f_{OSC} = 300kHz$, the power dissipation is calculated as:

$$\begin{aligned} P_{LOSS} &= 12V \{ 1mA + [12V(3nF + 6nF) + 12V \times 0.2nF] 300kHz \} \\ &= 0.41W \end{aligned}$$

The uP6281 is available in thermal enhanced PSOP-8L or WDFN3x3-8L packages. However, the thermal resistance θ_{JA} still highly depends on the PCB design. Copper plane under the exposed pad is an effective heatsink and is useful for improving thermal conductivity. Figure 1 shows the relationship between thermal resistance θ_{JA} of PSOP-8L package vs. copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at $T_A = 25^\circ C$. A 50mm² copper plane reduces θ_{JA} from 75°C/W to 50°C/W.

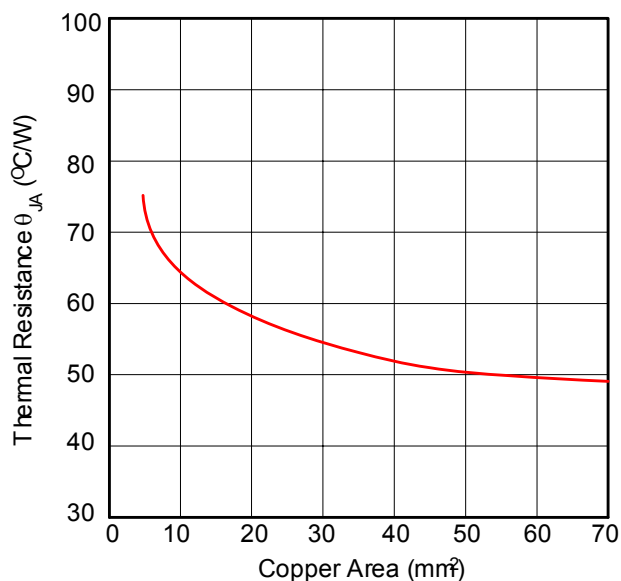
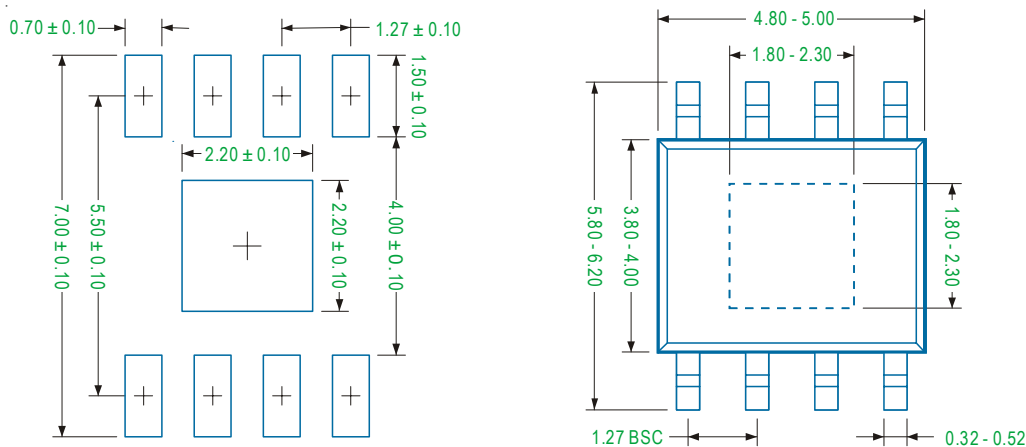


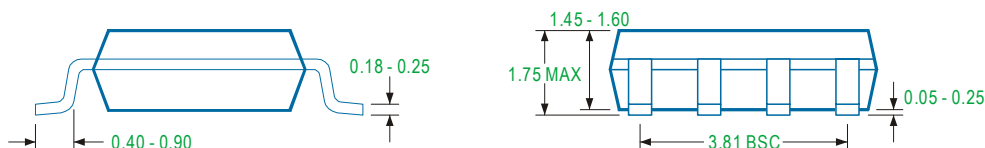
Figure 1. Thermal Resistance θ_{JA} vs. Copper Area

Take the above case for example, 0.41W power loss will cause $0.41W \times 50^\circ C/W = 20.5^\circ C$ temperature raise with 50mm² copper area.

PSOP-8 Package



Recommended Solder Pad Layout



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

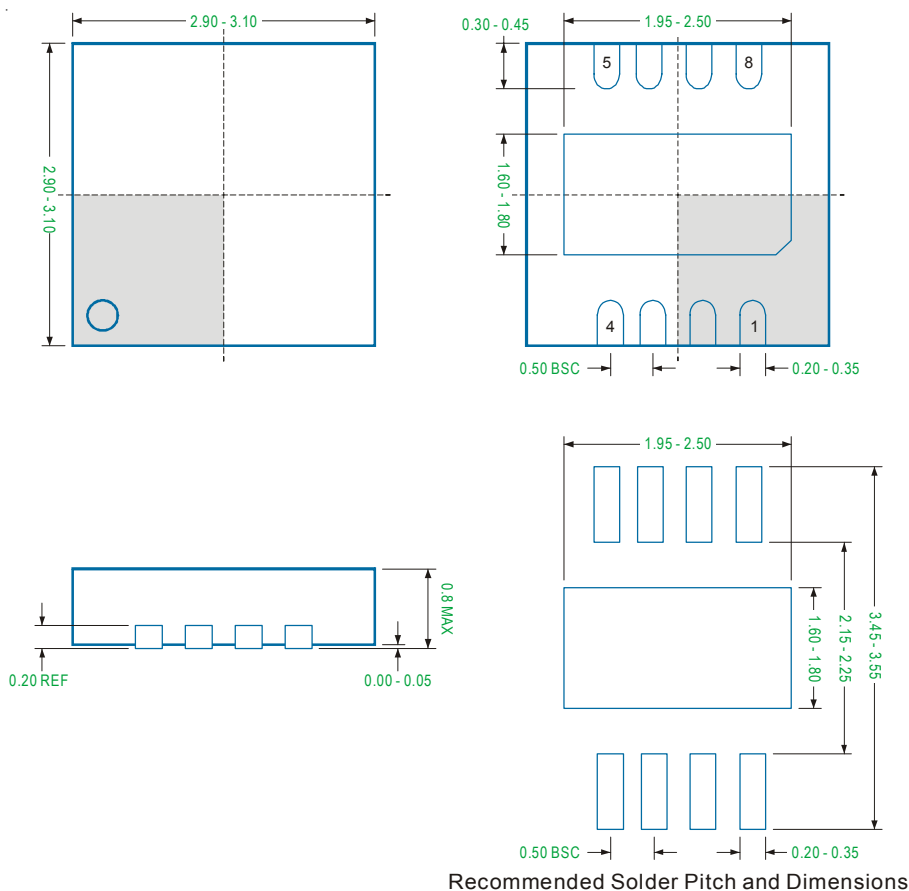
TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

WDFN3x3-8L Package



Recommended Solder Pitch and Dimensions

Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.