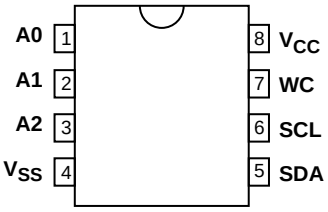
8,192-Bit Serial Electrically Erasable PROM
1.8 to 5.5 Volt Operation

FEATURES

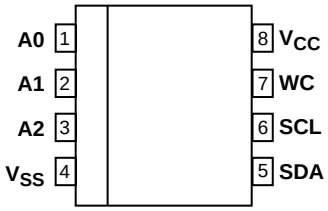
- **Low Power CMOS**
  - **— Active current less than 3mA**
  - **— Standby current less than 5μA**
- **Hardware Write Protection**
  - **— Write Control pin**
- **Industry's lowest power 8K E^2PROM**
- **High reliability**
  - **— All commercial devices tested to industrial temp range (-40°C to +85°C)**
- **True Philips licensed I^2C interface**
- **Internally Organized 1,024 X 8**
- **Two Wire Serial Interface (I^2C™)**
  - **— Bidirectional data transfer protocol**
  - **— Standard 100KHz and Fast 400KHz**
- **Sixteen-Byte Page-Write Mode**
  - **— Minimizes total write time per byte**
- **Automatic Word Address Incrementing**
  - **— Sequential register read**
- **Self-Timed Write Cycle**
- **High Reliability**
  - **— Endurance: 100,000 erase/write cycles**
  - **— Data retention: 100 years**
- **8-Pin PDIP or SOIC Packages**

PIN CONFIGURATIONS

Plastic Dual-in-line "P" Package



JEDEC Small Outline "Y" Package



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PIN NAMES

A0, A1	Unused Address Inputs
A2	Device Select Input
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{SS}	Ground
V_{CC}	Supply Voltage

OVERVIEW

The XL24C08 is a cost-effective, 8,192-bit serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. This part operates from a single power supply over the range of 1.8 to 5.5 volts.

The XL24C08 is internally organized as 1,024 x 8. It features the I^2C™ serial interface and software protocol allowing operation on a simple two-wire bus.

PIN DESCRIPTIONS

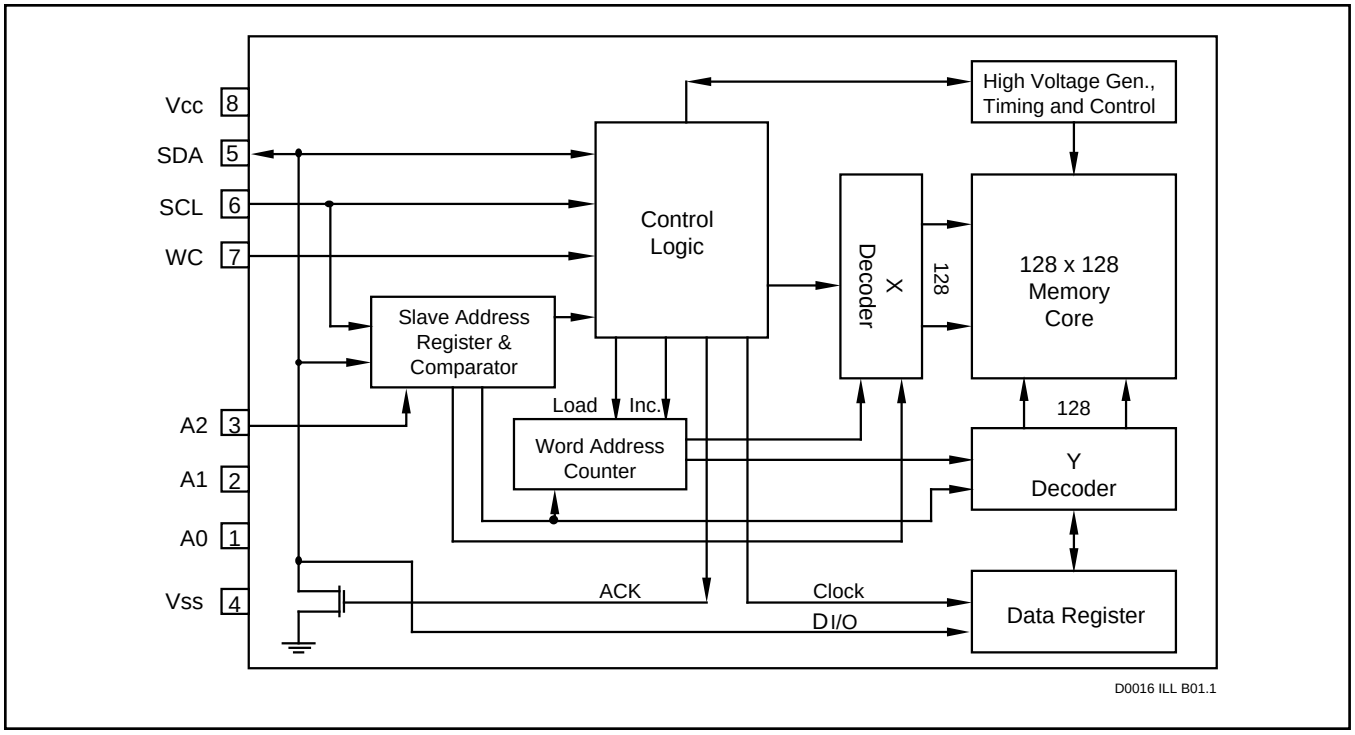
Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

Address Inputs (A0, A1) - The A0 and A1 inputs are unused by the XL24C08; however, to insure proper operation they can be unconnected or tied to ground. They must not be tied to V_{CC}.

Address Input (A2) - The A2 input is unused to set the appropriate bit of the seven bit slave address. It may be actively driven or tied to V_{CC} or V_{SS}. It cannot be a no connect.

BLOCK DIAGRAM



Write Control (WC) - The Write Control input pin is used to disable the write circuitry to the memory. This input must be tied HIGH, LOW, or left unconnected. When HIGH, the write function is disabled, protecting previously written data; when LOW or unconnected, the write function is enabled.

ENDURANCE AND DATA RETENTION

The XL24C08 is designed for applications requiring up to 100,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 100,000 erase/write cycles.

APPLICATIONS

The XL24C08 is ideal for applications requiring low voltage and low power consumption. This device uses a cost effective, space-saving, 8-pin plastic package, SOIC and PDIP. Typical applications include alarm devices, electronic locks, meters, keys, pagers and cellular phones.

CHARACTERISTICS OF THE I^2C BUS

General Description

The I^2C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition (See Figure 2).

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the “START” condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the “STOP” condition (See Figure 3).

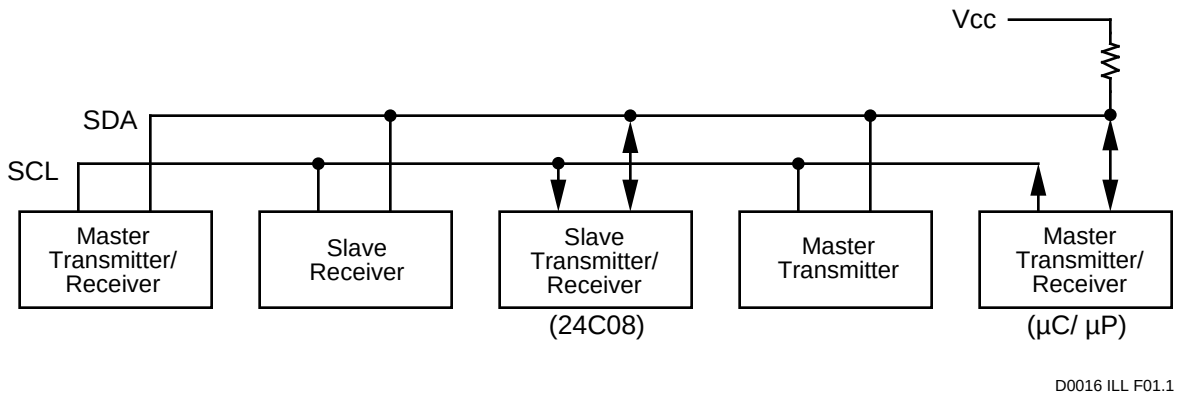


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

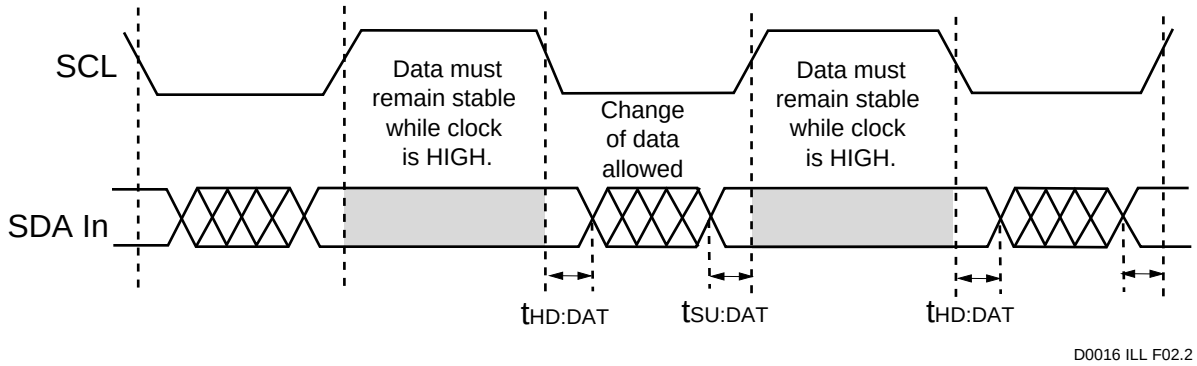


FIGURE 2. INPUT DATA PROTOCOL

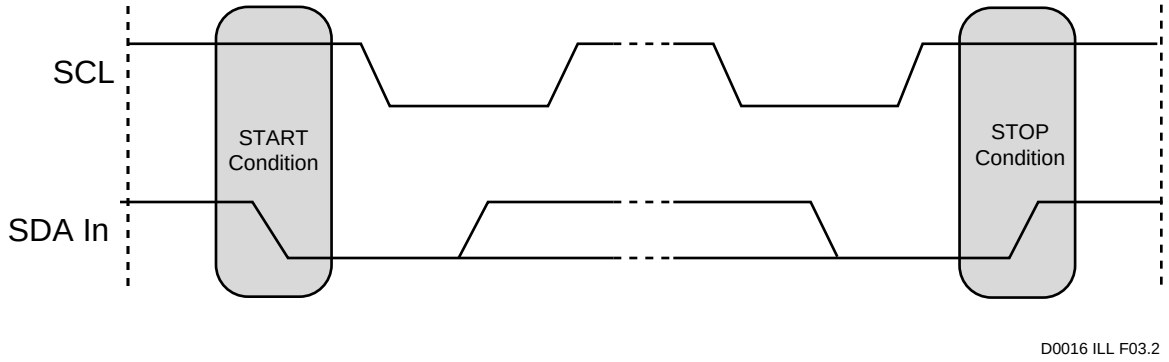


FIGURE 3. START AND STOP CONDITIONS

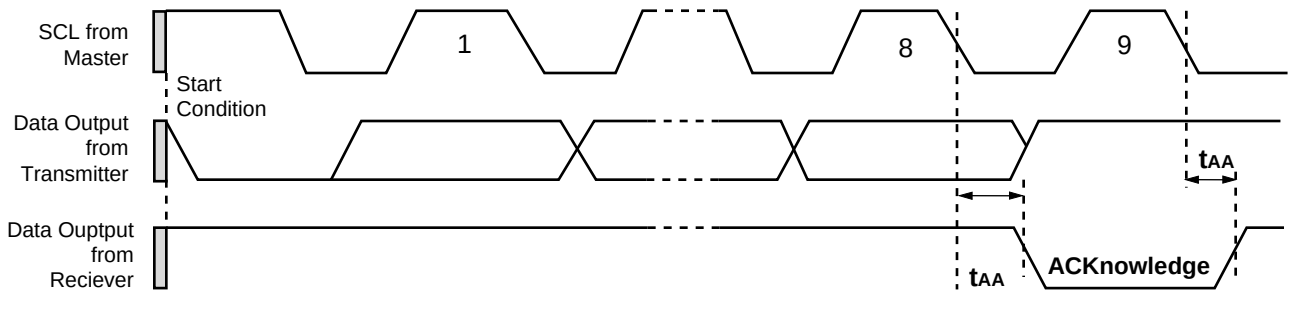


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

DEVICE OPERATION

The XL24C08 is a 8,192-bit serial E^2PROM. The device supports the I^2C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the XL24C08 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 4).

The XL24C08 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the XL24C08 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C08 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C08 will continue to transmit data. If an ACKnowledge is not detected, the XL24C08 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 5). For the XL24C08 this is fixed as 1010[B]. The next bit is used to select one of 2 devices on the bus as selected by the A0 input.

Word Address

The next two bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the 1,024 X 8 array.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

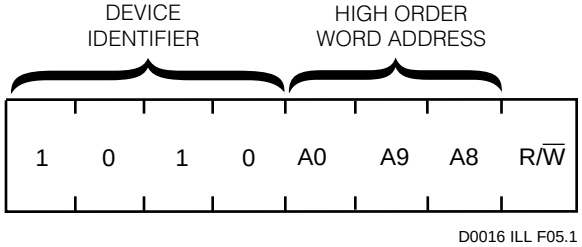


FIGURE 5. SLAVE ADDRESS BYTE

WRITE OPERATIONS

The XL24C08 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to full 16-byte in the same page to be written during t_{WR}.

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 2,048 words in the array.

Upon receipt of the word address, the XL24C08 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C08 begins the internal write cycle.

While the internal write cycle is in progress, the XL24C08 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The XL24C08 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the XL24C08 will respond with an ACKnowledge.

The XL24C08 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will “roll over,” and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

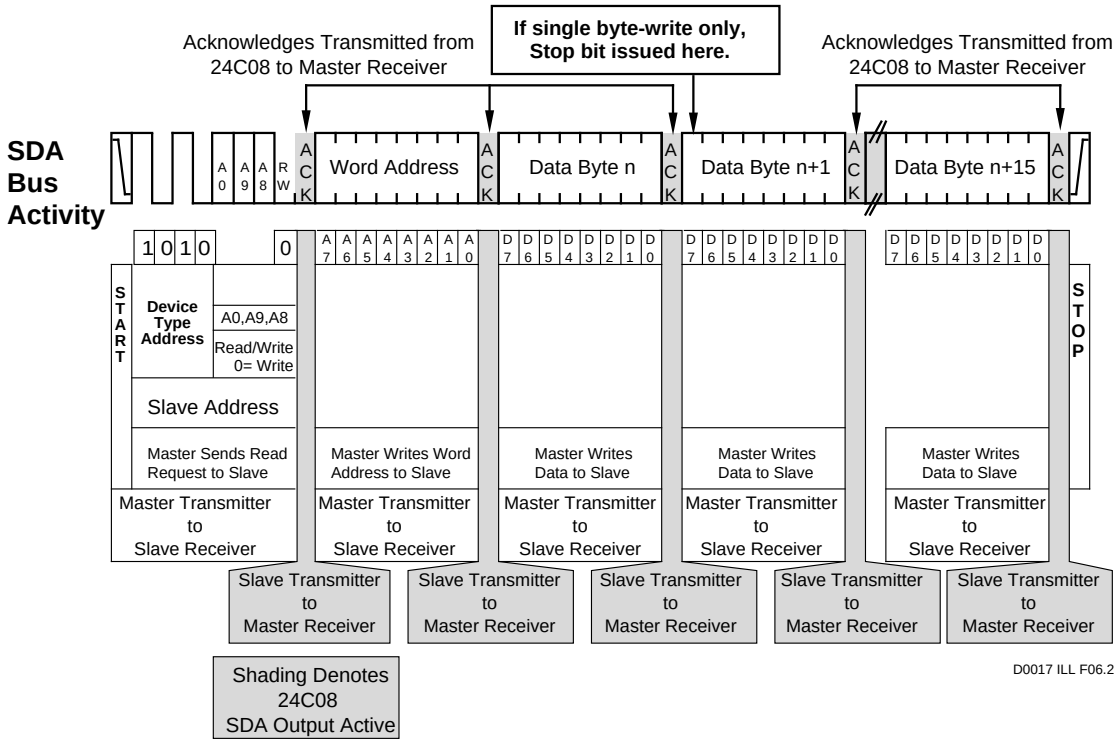


FIGURE 6. PAGE/BYTE WRITE MODE

Acknowledge Polling

When the XL24C08 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).

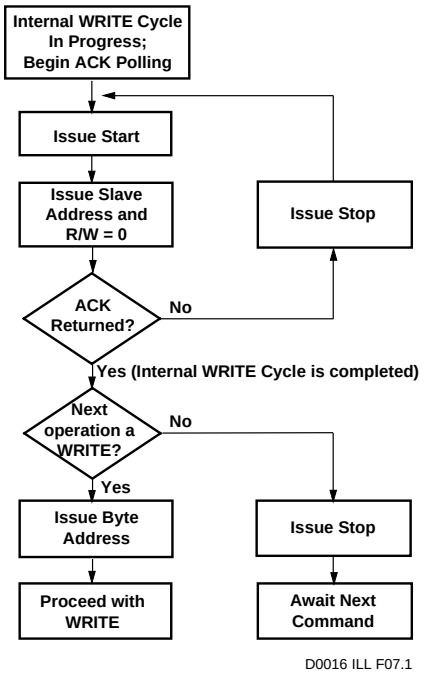


FIGURE 7. ACKNOWLEDGE POLLING

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The XL24C08 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the XL24C08 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the XL24C08 discontinues data transmission. See Figure 8 for the address acknowledge and data transfer sequence.

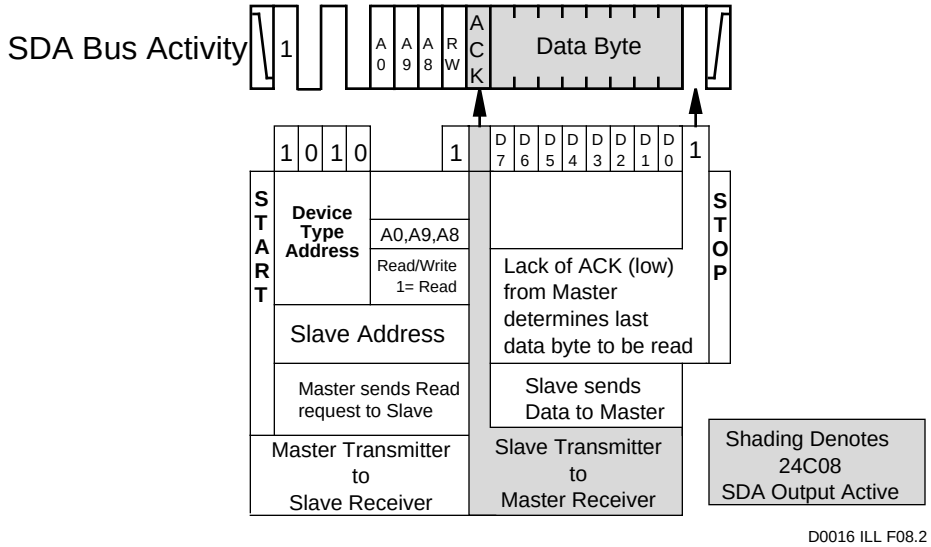


FIGURE 8. CURRENT ADDRESS BYTE READ MODE

Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the XL24C08 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The XL24C08 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The XL24C08 discontinues data transmission and reverts to its standby power mode. See Figure 9 for the address, acknowledge and data transfer sequence.

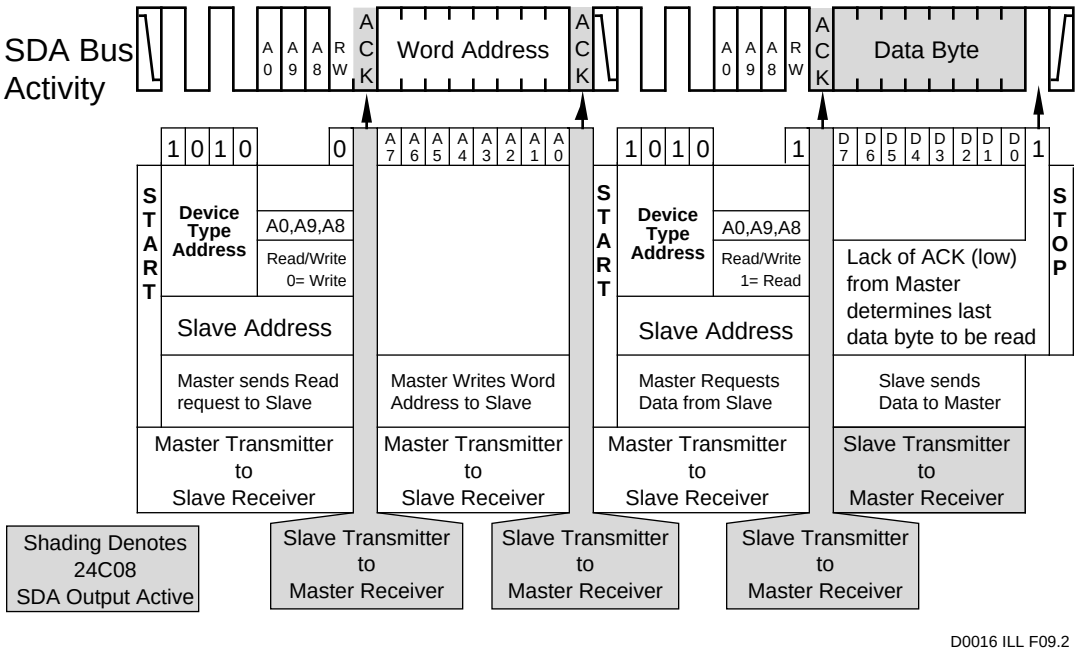


FIGURE 9. RANDOM ADDRESS BYTE READ MODE

Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the XL24C08. The XL24C08 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 10 for the address, acknowledge and data transfer sequence.

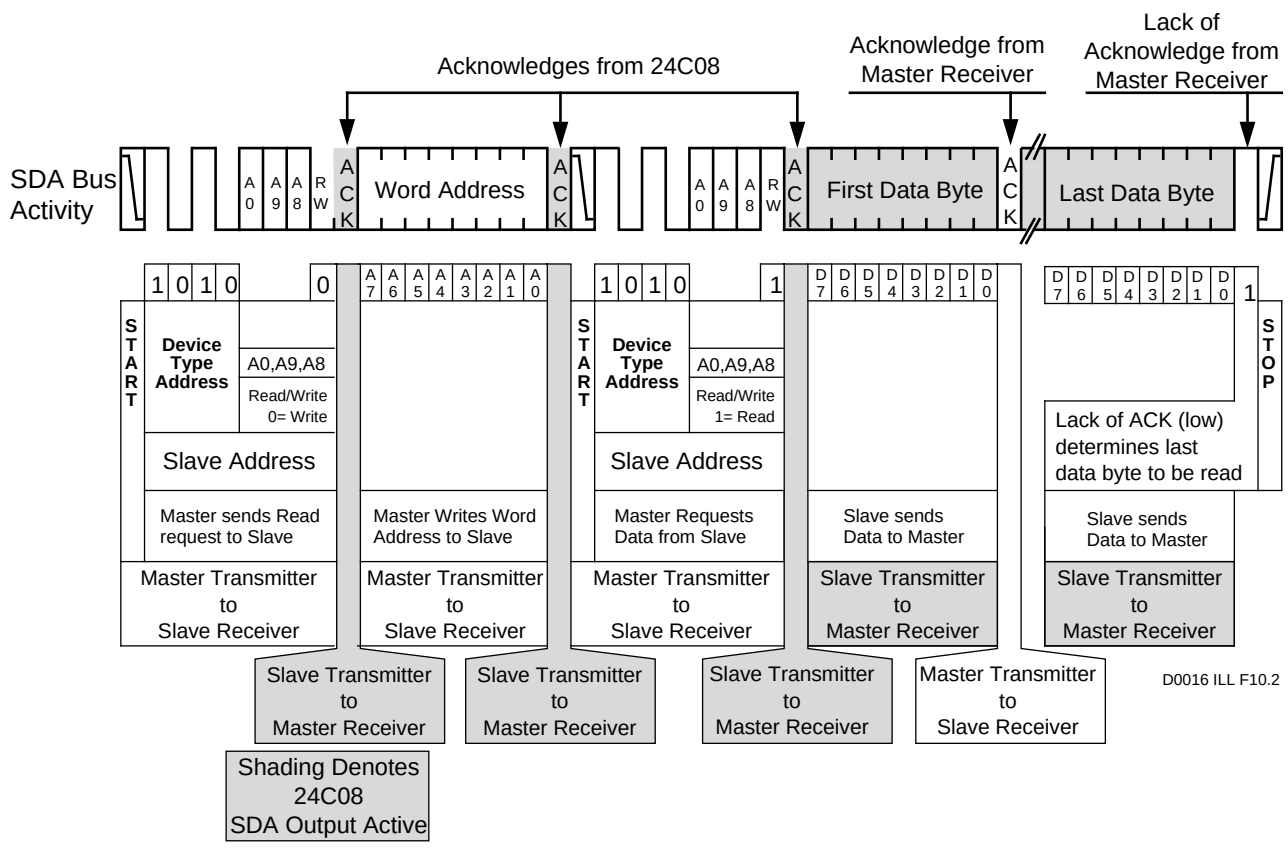


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150˚C
Soldering Temperature (less than 10 seconds) ..... 300˚C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3V to V_{CC}+0.3V
ESD Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{CC} = 1.8V to 5.5V

Symbol	Parameter	Conditions		Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	V_{CC} =5.5V		3	mA
			V_{CC} =1.8V		1	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	V_{CC} =5.5V		5	µA
			V_{CC} =1.8V		2	µA
I_{LI}	Input Leakage	V_{IN} = 0 To V_{CC}			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 To V_{CC}			10	µA
V_{IL}	Input Low Voltage	S0, $\overline{S1}$, S2, SCL, SDA			0.3xV_{CC}	V
V_{IH}	Input High Voltage	S0, $\overline{S1}$, S2, SCL, SDA		0.7xV_{CC}		V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V

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AC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{CC} = 1.8V to 5.5V

			1.8V to 5.5V		4.5V to 5.5V		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		µs
t_{HIGH}	Clock High Period		4.0		0.6		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		µs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

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CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

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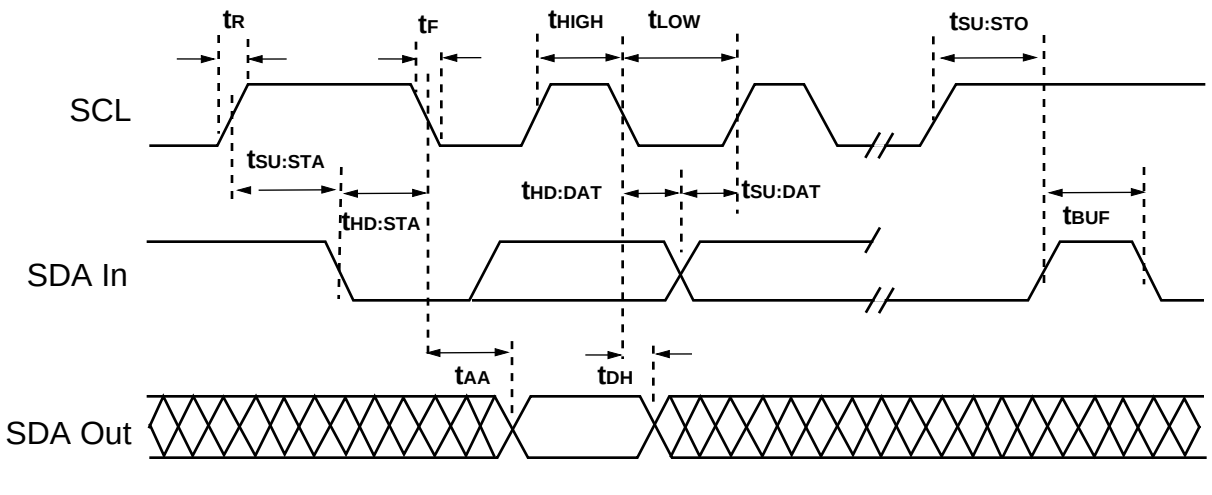

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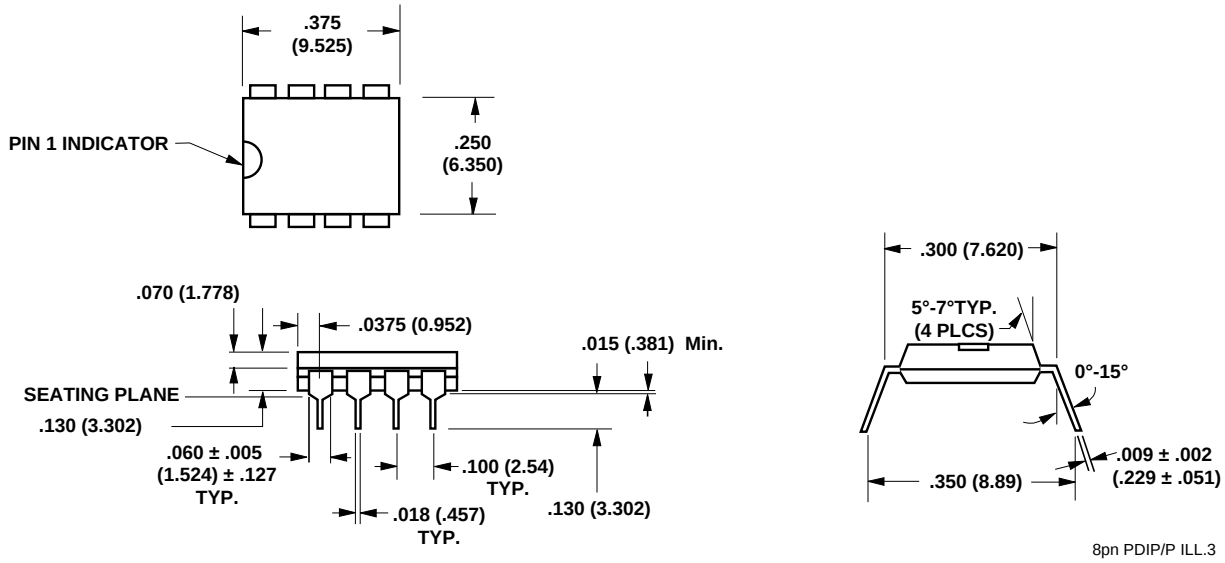
FIGURE 11. BUS TIMING

PACKAGE DIAGRAMS

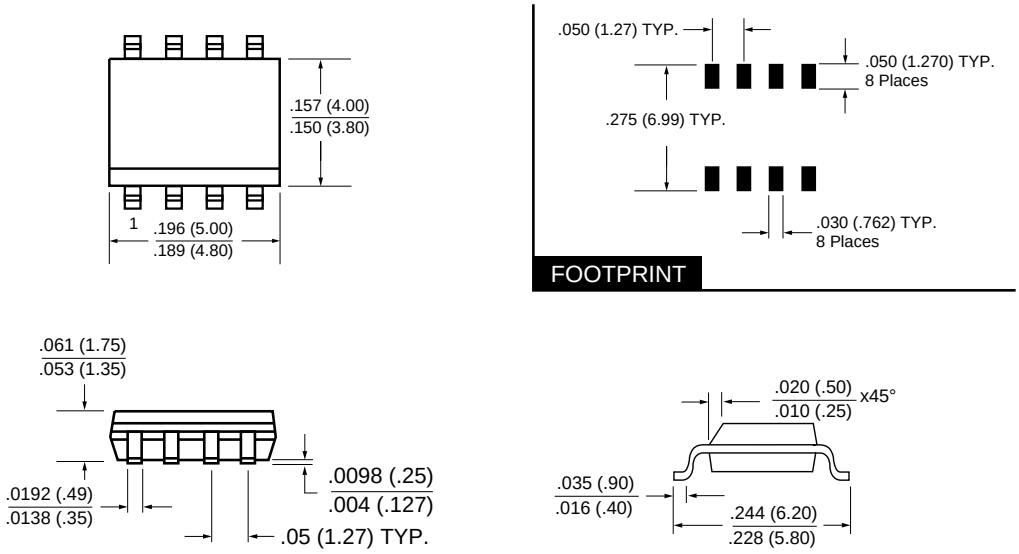
Plastic Dual-in-line (Type "P") Package (PDIP)*



8pn PDIP/P ILL.3

All dimensions in inches (mm).
* See cover page for pinout options.

8 Pin SOIC (Type "Y") Package* (JEDEC 150 mil body width)



8pn JEDEC SOIC ILL.1

All dimensions in inches (mm).
* See cover page for pinout options.

ORDERING INFORMATION

Prefix	Part Number	Package Type
XL	24C08	Y, P

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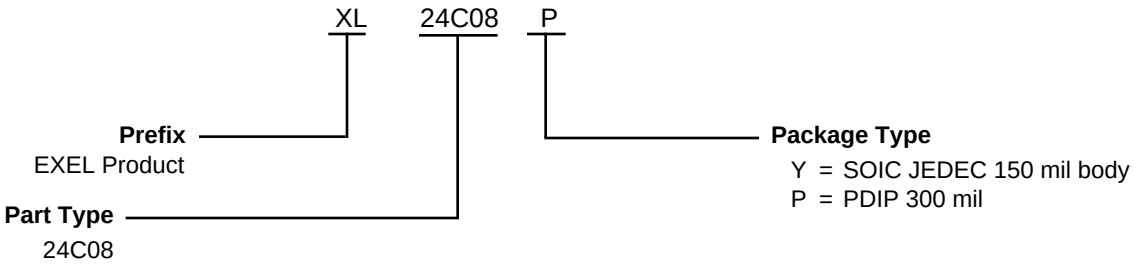
Part Numbers:



MARKING INFORMATION

* See cover page for pinout options.

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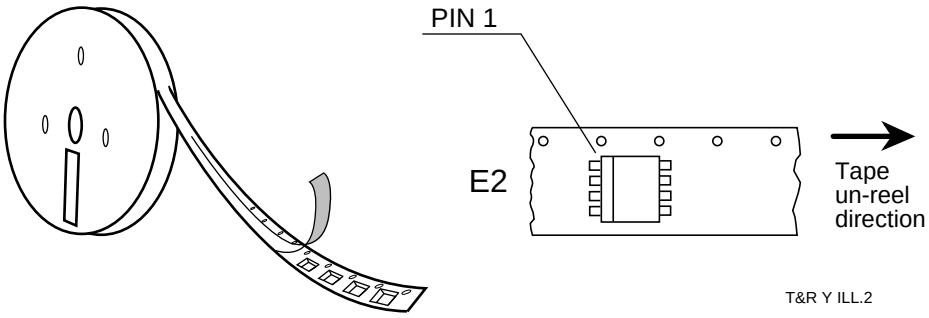
TAPE AND REEL (EMBOSSED) INFORMATION

Surface mount devices, which are normally shipped in antistatic plastic tubes, are also available mounted on embossed tape for customers using automatic placement systems. The following diagram provides general information regarding the direction of the IC's. Tape "E2" shall be designated with PIN 1 at the trail direction.



T&R Y ILL.2

SALES OFFICES

EXEL Corporate
Tel 408-432-0500
Fax 408-432-8710

EXEL Northwest/North Central
Tel 810-684-2959
Fax 810-684-2430

EXEL East
Tel 407-365-8796
Fax 407-977-0449

EXELFax™ Literature Hotline
1-800-853-5886
1-908-935-2774

EXEL Southwest/South Central
Tel 214-881-1205
Fax 214-881-1056